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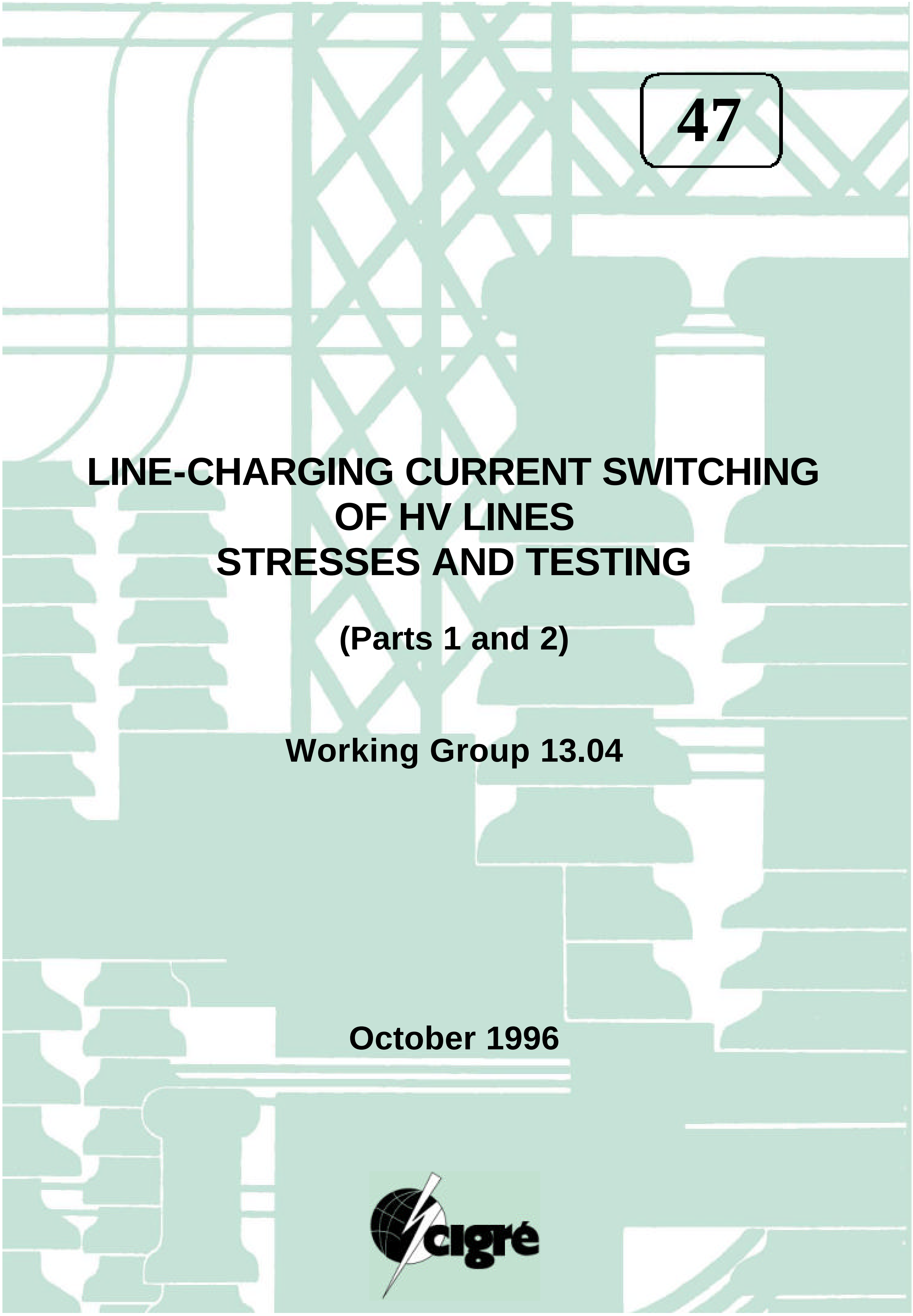
# LINE-CHARGING CURRENT SWITCHING OF HV LINES
# STRESSES AND TESTING

(Parts 1 and 2)

Working Group 13.04

October 1996



# LINE-CHARGING CURRENT SWITCHING OF HV LINES

## STRESSES AND TESTING.

(Part 1)

Working Group 13.04*(Switching Test Methods)

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## 1. - INTRODUCTION.

A first report issued in Electra 155, presented the State of the Art for capacitive current switching. This general paper should be followed by several more detailed studies concerning capacitive current switching : line-charging current switching, capacitor bank switching, etc ... The present paper deals with line-charging current switching for voltages 72.5 kV and above, by circuit-breakers and also switches, provided that they have a limited time spread between pole contact parting.

Switching the capacitive current of an unloaded line is something usual in service on HV networks. This must be done with the confidence that it will not result in any hazard to the system. This is not truly the case, as utilities have reported restrikes of circuit-breakers, although they were assumed to be restrike-free (see section 3.1.3 for the definition).

The working group has sent a questionnaire to many utilities in the world, to have their feedback about the deficiencies of the IEC standard for circuit-breakers (IEC 56). The results of this survey are followed by a theoritical analysis of the switching cases.But the main task of the working group has been to discuss test circuits and test procedures, to make proposals to improve IEC 56.

The existing IEC standard does not require circuit-breakers to be restrike-free, but it does not detail tests for a non restrike-free circuit-breaker. This is a key point. As it is not the work of such a CIGRE working group to decide whether or not a circuit-breaker has to be restrike-free, the working group has decided to consider both cases, that is to say to propose test circuits that can be used in laboratories for restrike-free circuit-breakers or for circuit-breakers which restrike. However, the working group opinion is that a circuit-breaker rated 245 kV and above must be restrike-free.

As mentioned above, this report does not deal with MV line-charging current switching even if the basic phenomena remain the same. The topology of the networks are different, and test circuits are generally 3-phase circuits. Besides, the risk for the network caused by restrike(s) is lower at these lower voltages.

## 2. - QUESTIONNAIRE

### 2.1 The questionnaire

A questionnaire was sent in 1989 to utilities which were assumed to be representative of the various possible cases of no-load line switching encountered in the world. The aims were as follows :

1. To evaluate the degree of satisfaction with the existing international standard IEC 56 for circuit-breakers, as far as capacitive current switching is concerned for voltage levels 72.5 kV and above.
2. To identify if any aspects of capacitive current switching are not covered by IEC, but are taken into account in users' specifications.
3. To make a survey of the existing circuit-breakers : types, prevalence.

35 utilities representing 20 countries have answered this questionnaire. These countries are :

*AUSTRALIA (AU), AUSTRIA (AT), BELGIUM (BE), BRAZIL (BR),CANADA (CA), CHINA (CN), CIS (CIS), FRANCE (FR), GERMANY (DE),GREECE (GR), ITALY (IT), JAPAN (JP), NETHERLAND (NL), SOUTH AFRICA (ZA), SWEDEN (SE), SWITZERLAND (CH), UNITED KINGDOM (UK), UNITED STATES (US),VENEZUELA (VE), ex YUGOSLAVIA (YU).*

### 2.2 Users' points of view on IEC 56

On a total number of 111 answers (all voltage classes and utilities together) :

- 53 (48%) utilities are satisfied with the present IEC 56
- 58 (52%) consider that an improvement of the standard is needed.

It is not easy to find a geographical apportionment of these negative answers. However, countries with short distances between the points of production and consumption, i.e : western European countries in this survey, are all satisfied with IEC with the exception of the testing procedure (DE, FR, CH) in particular the number of tests and the way of choosing them.

For countries with long lines, the testing procedure is also mentioned (BR, AU). But the main points are that they are not satisfied with rated current (line lengths) (BR, AU and also SE) and the test voltage levels (BR, CA) as they are defined in IEC.

### 2.3 Additional requirements in users' specifications

Some utilities ask for additional requirements in their specifications to cover specific needs. As far as switching of unloaded lines is concerned, three main demands have been identified :

1. - the load rejection at one end of the line (at the load side) followed by the opening of the unloaded line by the circuit-breaker at the supply side,
2. - the switching of the two remaining healthy phases of an overhead line subject to a single phase fault,
3. - requirements to cover phenomena associated with the compensation of the line.

The survey results are presented on figure 1 as a function of voltage level.

- Load rejection.

On a total number of 128 answers (all voltage classes and utilities together), 56 (44%) take into account the load rejection, mainly in countries with long lines (AU, BR, CA, US) but also in other countries (DE, JP, SE). The answers are evenly distributed over all voltage levels.

- Healthy phases switching.

On a total number of 128 answers, 82 (64%) take into account the switching of healthy phases. Most of these answers are from countries with long lines (AU, BR, CA, CN, CIS, US, VE), from three countries in Europe (AT, IT, SE) and from Japan. The answers are evenly distributed over all voltage levels.

- Line compensation.

On a total number of 128 answers, 28 (22%) take into account compensation of the line. This is only the case of countries with long lines (AU, BR, CIS, US, VE), mainly for voltages 245 kV and above.

## 2.4. Other elements from the questionnaire.

### 2.4.1 Purchase of restrike-free breakers.

The analysis of the results clearly indicates that the users want to purchase restrike-free circuit-breakers, although there is no requirement in IEC 56. In 1989, only three countries (BR, FR, SE) bought circuit-breakers which might be "non restrike-free". These circuit-breakers are used on networks with voltages up to 245 kV but mostly below.

One can also see from figure 2 that a large number of circuit-breakers for voltages up to 245 kV are oil-breakers and it is doubtful that most of these circuit-breakers could be restrike-free.

### 2.4.2. Lengths of the lines.

Figure 3 indicates the maximum lengths of the lines for a given utility and a given voltage level. These figures are compared to the value derived from the IEC rated capacitive current and voltage values (an extrapolation to 700 A has been chosen as the rated line-charging breaking current for a 765 kV circuit-breaker). The conclusion is globally contrary to what was expected : IEC current values cover most of the needs (92%) above 245 kV, but only 61% in the range 72.5 kV -245 kV.

As for the minimum lengths, most of them are very short, i.e. in the range of 1 km. This means stresses not well covered by IEC tests :

- a voltage wave shape across the circuit-breaker nearly 1-cos, thus without voltage drop after current zero.
- a very low current ( ~ 1 A).

## 2.5. Conclusion.

This questionnaire was sent to many utilities having various network conditions, various practices and hence various specifications for line switching.

Half of them wish a change of the existing IEC, essentially to improve the testing procedure.

This enquiry shows that load rejection and healthy phases switching are often required in the specifications. These network conditions are more severe for the circuit-breaker.

A large majority of the users wants circuit-breakers which will not restrike in their networks. Exceptions are limited to below 245 kV for which the consequences of a restrike are less dangerous because the ratio of the permissible overvoltage to the rated voltage is greater than for higher voltage levels.

■ Load rejection □ Switching of healty phases ◆ line compensation

| | | | |
|---|---|---|---|
| 420 kV | | | |
| AT | | □ | |
| BE | | | |
| CH | | | |
| DE | | | |
| FR | | | |
| GR | | | |
| IT | | □ | |
| NL | | | |
| SE | | □ | |
| UK | | | |
| VE | ■ | □ | ◆ |
| YU | | | |
| ZA | | | |
| 525 kV | | | |
| AU | ■ | □ | ◆ |
| AU | | | |
| BR | ■ | □ | |
| BR | ■ | □ | |
| BR | ■ | □ | ◆ |
| BR | ■ | □ | ◆ |
| BR | ■ | □ | ◆ |
| CIS | | □ | ◆ |
| CN | | □ | |
| JP | ■ | □ | |
| JP | ■ | □ | |
| JP | ■ | □ | |
| JP | ■ | □ | |
| US | | □ | ◆ |
| US | ■ | □ | ◆ |
| >765 kV | | | |
| BR | ■ | □ | ◆ |
| CA | ■ | □ | |
| CIS | | □ | ◆ |
| CIS | | □ | ◆ |
| VE | ■ | □ | ◆ |
| ZA | | | |
| 170 kV | | | |
| BE | | | |
| CA | ■ | □ | |
| GR | | | |
| IT | | □ | |
| JP | ■ | □ | |
| JP | ■ | □ | |
| JP | ■ | □ | |
| JP | ■ | □ | |
| NL | | | |
| 245 kV | | | |
| AT | | □ | |
| AU | ■ | □ | ◆ |
| AU | | | |
| BE | | | |
| BR | | | |
| BR | ■ | □ | |
| BR | | □ | |
| BR | ■ | □ | ◆ |
| BR | ■ | | |
| BR | ■ | □ | ◆ |
| BR | ■ | □ | ◆ |
| BR | ■ | □ | |
| CA | ■ | □ | |
| CH | | | |
| CIS | | □ | ◆ |
| CN | | □ | |
| DE | | | |
| FR | | | |
| IT | | □ | |
| NL | | | |
| SE | ■ | | |
| US | ■ | □ | |
| US | | □ | ◆ |
| YU | | | |
| 300 kV | | | |
| AU | | □ | |
| AU | | | |
| AU | ■ | □ | ◆ |
| JP | ■ | □ | |
| JP | ■ | □ | |
| JP | ■ | □ | |
| JP | ■ | □ | |
| UK | | | |
| ZA | | | |
| 362 kV | | | |
| AU | ■ | □ | ◆ |
| AU | | | |
| BR | ■ | □ | ◆ |
| BR | ■ | □ | |
| CA | ■ | □ | |
| CIS | | □ | ◆ |
| CN | | □ | |
| US | | □ | |
| 72,5 kV | | | |
| AU | | □ | |
| BE | | | |
| BR | | | |
| BR | ■ | □ | |
| BR | ■ | □ | |
| BR | | □ | |
| BR | ■ | □ | ◆ |
| BR | | □ | |
| BR | ■ | □ | |
| CA | | □ | |
| CN | | | |
| FR | | | |
| GR | | | |
| JP | ■ | □ | |
| JP | ■ | □ | |
| JP | ■ | □ | |
| JP | ■ | □ | |
| US | | | ◆ |
| US | | □ | |
| 100 kV | | | |
| FR | | | |
| 123 kV | | | |
| AT | | □ | |
| AU | | □ | |
| CIS | | □ | ◆ |
| CN | | □ | |
| DE | ■ | | |
| NL | | | |
| US | | | ◆ |
| US | ■ | | |
| YU | | | |
| 145 kV | | | |
| AU | | | |
| AU | | □ | |
| BR | | | |
| BR | | □ | |
| BR | ■ | □ | |
| BR | | □ | |
| BR | ■ | □ | |
| BR | ■ | | |
| BR | ■ | □ | ◆ |
| BR | ■ | □ | ◆ |
| CA | ■ | □ | |
| SE | | | |
| SE | ■ | | |
| UK | | | |
| US | | □ | |

Figure 1 : Specific users' needs

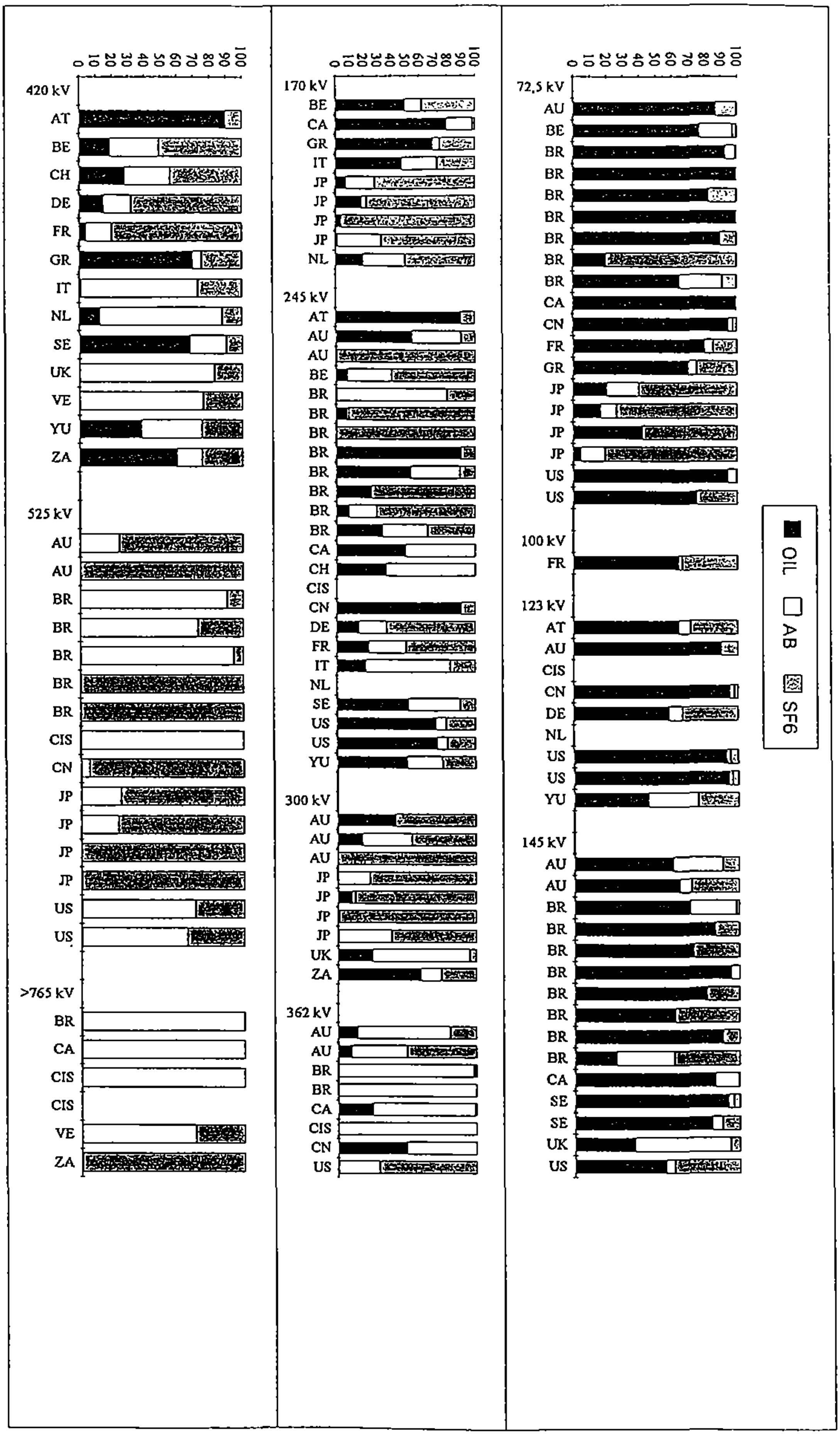


Figure 2 : Circuit-breakers types

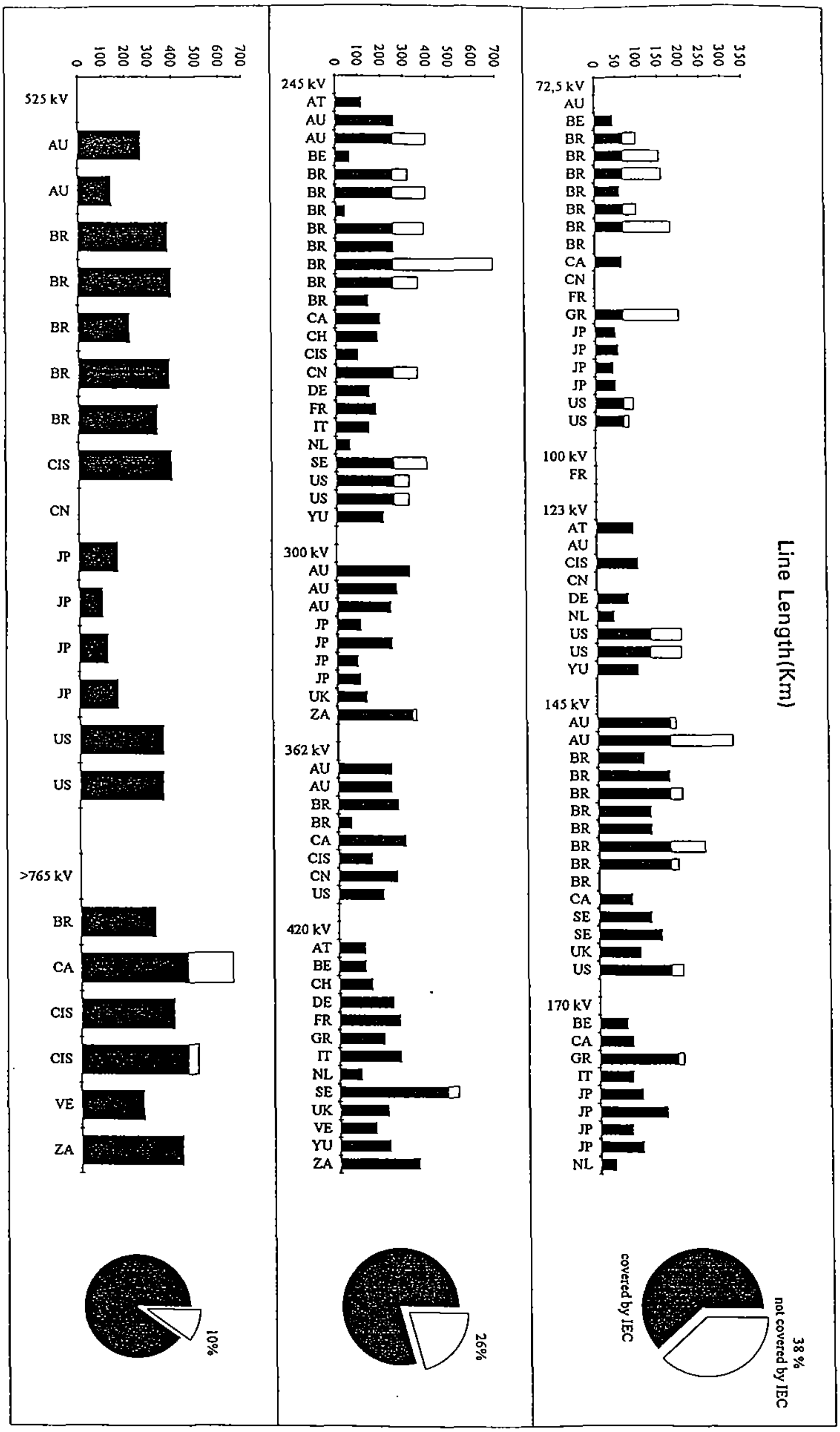


Figure 3 : Length of the longest line

## 3. DESCRIPTION OF THE PHENOMENA

### 3.1. Basic phenomena

### 3.1.1. When the circuit-breaker is closed

- An unloaded overhead line can be generally represented by a capacitance, Fig.4. In the case of short lines (< 200 km) this capacitance can be concentrated, but in the case of long lines it must be distributed. Typical values vary from 9.1 nF/km per phase for single conductor to 14 nF/km per phase for four-conductor bundle.

When the remote end of the line is open, the voltage values $U_1$ and $U_2$ to ground at the circuit-breaker correspond to Eq. (2), i.e. the difference $\Delta U = U_c - U_0$ increases proportionally to the line length a and to the source impedance $L_S$.

(1) $i_c = U_c \omega C_L$.

and

$$U_0 = i_c\left(\frac{1}{wC_L} - wL_S\right)$$

which yields :

(2) $U_1 = U_2 = U_c = U_0/(1-\omega^2 * L_S * C_L)$ e.g. from /1/,

where $U_0 = U/\sqrt{3}$ reference phase-to-ground voltage

$U_1 = U_2 = U_c$ source side voltage at closed breaker, which is greater than $U_0$

$\omega = 2\pi f_p$ ($f_p$..power frequency)

$C_L >> C_1$

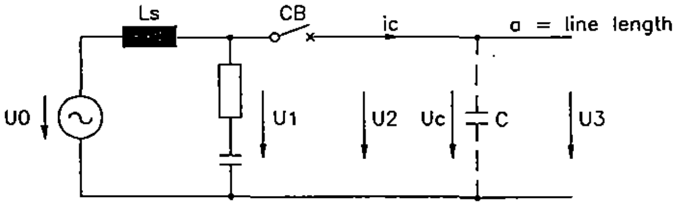


Figure 4 : Schematic circuit for no-load line switching

- Because of the capacitive current drawn through the line reactance, the unloaded line does not have a constant voltage but an increase of the value from the source side ($U_2$) to the open end ($U_3$) of the line. This is the Ferranti effect which can be written :

$U_3/U_2 = 1/\cosh \gamma a$ or :

(3) $U_3 / U_2 = 1 / \cos \gamma a$ e.g. from /2/.

where $\gamma$ = phase constant in rad/km or degrees/km,
a = length of the line,

This relationship is obtainable from the differential equations of the line in sinusoidal steady-state conditions assuming

| | |
|---|---|
| $\bar{z} = r + j\omega l$ | as the longitudinal line impedance per unit length, where r and are the resistance and inductance of the line per unit length and |
| $\bar{y} = g + j\omega c$ | as the transversal line admittance per unit length, where g and c are the admittance and capacitance of the line per unit length and from which the following line parameters are defined: |
| $\bar{Z}_0 = \sqrt{(\bar{z}/\bar{y})}$ | (surge impedance) |
| $\bar{\gamma} = \sqrt{(\bar{z}\bar{y})}$ | (propagation constant [$km^{-1}$]). |

Disregarding the losses of the line, represented by r and g, results in

(4) $\bar{\gamma} = j\gamma = j\omega\sqrt{(lc)}$.

A typical value at 50 Hz, disregarding the line losses, may be $\gamma \cong 10^{-3}$ rad/km, that means the Ferranti effect is 1.03 already assuming a = 250 km :

$U_3 / U_2 = 1 / \cos 0.25 = 1.03.$

As a result, we can define a "long line" as a line longer than 200 km, that is one having an open end voltage increase greater than 2% of the breaker voltage.

### 3.1.2. When the circuit-breaker opens

- After current interruption, the initial voltage jump of the source side (/3/) associated with the voltage difference $U_C - U_0$ is directly related to the total capacitance of the line and/or the source impedance since $U_C - U_0 = U_C\omega^2 L_S C_L$. For very long lines, the initial voltage jump can significantly contribute to extending the arcing time.

- As already mentioned the Ferranti effect causes a higher peak value of the power frequency voltage $U_3$ at the end of the line than at the breaker side $U_2$. Thus after current interruption, the voltage being on the peak value, the line oscillates by means of travelling waves having an amplitude $U_3$-$U_2$.

The velocity of propagation, disregarding the losses, is given by $v_1 \cong 1/\sqrt{(1c)}$ for the direct wave $v_1$ and is approximately the velocity of the light, while the velocity of the zero sequence wave is
$v_0 = 0.6 - 0.7\ v_1$, depending on the resistivity of the soil.

The travelling waves have sinusoidal form and are defined by the wave length $\lambda = 2\pi/\omega\sqrt{(1c)}$ (distance between two successive maxima) and oscillation frequency $\varphi = 2v/a$ determined by the line length a.

The energy losses cannot be accounted for by constant resistance and leakage conductance factors r and g. Indeed, these losses are due to corona, ground resistance and skin effect, none of which are linear functions of voltage or current /4/.

From eq. (3), the most decisive parameter controlling the voltage increase is the line length followed by the capacitance and the inductance per unit length. Other parameters are the influence of the adjacent phases and lines, but also the geometric characteristics of the line such as the three-phase arrangement, the radius of the single conductors, the radius of the bundles arrangement and the effect of the line transposition if any /1,5,6/.

- The recovery voltage across the breaker approximately corresponds to a "1-cosine" shape : a cosine voltage on the source side starting on the voltage maximum (1 pu) and a dc voltage on the line side. However, the transient effects mentioned beforehand at both sides of the breaker cause, particularly with long lines, a significant deviation which usually increases the maximum voltage stress of the breaker : with very long lines up to 2.8 pu in extreme cases.

The combination of long line and high short circuit impedance, which increases both the 1-cos recovery voltage and the voltage value due to the Ferranti effect, increases also the initial rate of rise of the recovery voltage. This and the contribution of the voltage jump can lead to an early reignition.

### 3.1.3. If the circuit-breaker reignites

Where the dielectric strength of the opening contact gap is overstressed by the recovery voltage, the gap collapses and a flashover arc bridges the contacts. This is called a reignition or a restrike. As a result the line voltage will be adapted to the momentary value of the source side by an oscillating current. Frequency and amplitude of this current oscillation depend on line length and impedance conditions at the source side (see figures 5 and 6).

Especially with long lines an almost rectangular current waveshape is obtained due to travelling wave phenomena.

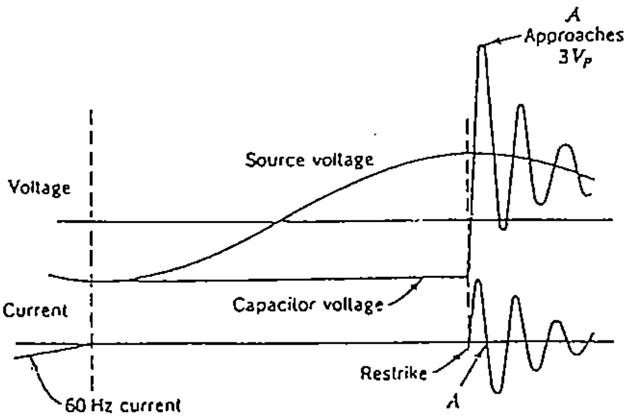


Figure 5 : Capacitance switching with a restrike at peak voltage
(from /6/)

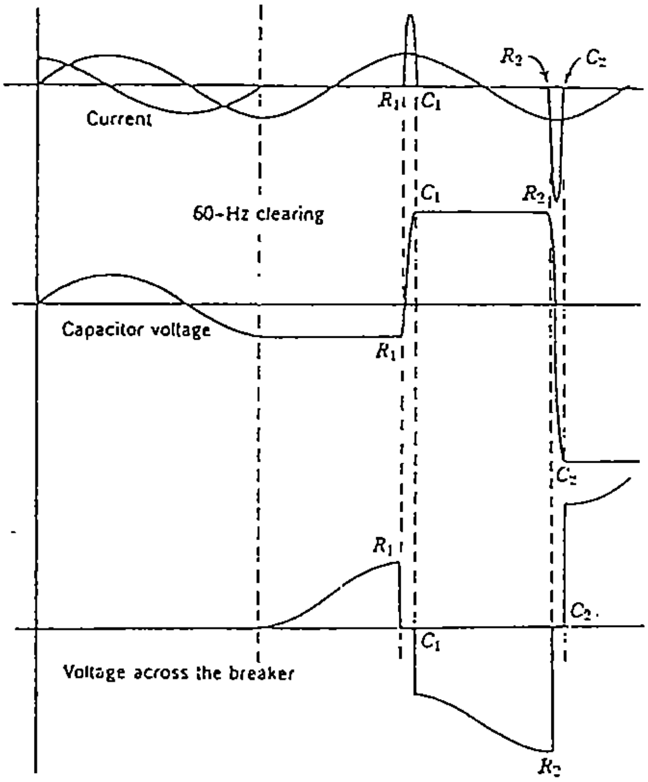


Figure 6 : Capacitance switching with multiple restrikes
(from /6/)

The line voltage may be trapped at 3 pu where the restrike occured close to (or at) the peak of the power frequency source side voltage and the oscillating current was interrupted by the breaker at current zero after the first half cycle (Fig. 6). Also superimposition of voltage wave traveling phenomena occurs (doubling by reflection at the far open end) which may increase the voltage to ground up to 3.7 pu /11/. Even by the use of metaloxide surge arrestors the overvoltage cannot be suppressed below 2.3 pu /11/. Figure 6 shows also a second restrike, with doubled amplitude of the current, on the successive power frequency voltage loop and voltage escalation of the line from +3 pu to -5pu.

However, restrikes occur usually before the maximum of the recovery voltage. Also the oscillating current is not necessarily interrupted after the first half cycle but after the second or even later. Thus the trapped charge voltage at the line usually is significantly less than that given by the theoretical case of voltage escalation shown by figure 6 (a good example is given on figures 2.12 and 2.13 of /3/).

**Because of the potential negative effects that restrikes might have on the network, restrike-free performance is advantageous. But how could a restrike-free switching device be defined ?** It cannot be in absolute terms, because of the statistical nature of the phenomena. The working group suggests to define it through the tests : **the type test is intended to provide the degree of confidence required by the users for a specific application, e.g. line switching taking into account for instance the number of operations in service, the risks linked to the restrike.**

### 3.1.4. When the circuit-breaker closes

During a closing operation of the breaker a preignition across the open contact gap can occur close to the peak value of the power frequency voltage. The load side at this instant can have a dc voltage charge, depending on the previous switching operation, and this could be in the range (0-1.5) $U_0$ of opposite polarity.

In order to prevent the possible high overvoltages it should be closed with a minimum difference voltage. Different methods may be used to ensure this. Two methods are closing resistors and controlled switching. If neither of these methods is used, the line voltage transient, from 1 pu (in the case of trapped charges), may reach in the worst cases 5 pu on the opposite polarity according to /6/.

The working principle for closing resistors is the following. An additional switch inserts the resistance a fixed time before touching of the contacts of the interrupting chamber. During this time, the line voltage is equalised to that of the supply through the resistor and the main contact closes only on relatively small voltage. The resistor and the time have to be adjusted in order to ensure a minimum of potential difference at the moment of contacts touching. Usually resistor values in the range between 0.5 and 2.0 times the line impedance are used. For longer lines the value of the resistor should be closer to the smaller value. The insertion time of the resistor is usually in the range of 8-20 ms and is dependent on the time needed to equalise the voltages.

These principles can be realised either with the resistor in series with the interrupting chamber or with the resistor in parallel to the interrupting chamber. Most of the resistor chambers are directly connected to the circuit-breaker mechanism (this means fixed insertion time). However, resistor chambers driven by an independent drive are known. The working principle is equal from the network point of view, but the resistor chamber itself has to cope with different stresses. In literature there is also mentioned the use of inductances instead of resistors, but it seems that this method is normally not used in practice. Because of voltage coordination and protection, closing resistors are only needed for systems with voltages above 420 kV and for long lines.

For controlled switching a device (mainly electronic) is needed which gives the closing impulse for the switching device so that there is only a minimum voltage difference (in the best case zero) at the moment of contacts touching. This method requires a very precise mechanism. Also the interrupting chamber needs a steep voltage time characteristic in order to allow closing in the vicinity of the zero crossing of the voltage across breaker terminals. To keep the closing at constant small voltage differences it is also necessary to have a precise knowledge about the behaviour of the drive at different conditions, e.g. temperatures. The general problems of controlled switching was a task of a separate CIGRE task force /20/ where these questions were analysed in more detail.

### 3.2. Detailed evaluations of the line side voltage and recovery voltage across the breaker

Considering the voltage on the line side terminal of the breaker after a switching operation ($U_2$ in figure 4), an overvoltage factor can be defined as the ratio of the maximum value of $U_2$ and the line-to-neutral crest voltage of the source. For a given configuration of the line, the dc line voltage of the first cleared phase is increased by the coupling with the not yet switched phases and by the Ferranti effect, in its turn depending on the source impedance.

As an example, in order to allow comparisons among single 420 kV - 50 Hz lines of different length but having the same characteristics and source condition, EMTP computations have been carried out adopting the same phase switching sequence. The supply side model gives 40 kA short circuit current. The recovery voltage for 100% Terminal Fault has a peak value $U_C$ and a rate of rise of the recovery voltage approximately according to IEC 56 (1987). The line parameters are such as to give capacitive currents of 85 A (a=100 km), 270 A (a=300 km) and 476 A (a=500 km).

Peak values of the line side voltages ($U_L$) in pu (1 pu = 420* $2\sqrt{2}/\sqrt{3}$ kV) and of the total recovery voltage have been computed in order to evaluate the contributions (which do not appear at the same instants) of the intercoupling from second and third phase and of the Ferranti effect to the line side voltage. The results are presented in table 1 below.

| Line length (km) | 100 | 300 | 500(*) |
|---|---|---|---|
| Source (a) (pu) | 1 | 1 | 1 |
| Trapped charge (1pu+voltage jump) (b)(pu | ≅ 1 | 1.005 | 1.01 |
| Ferranti effect (c) (pu) | 0.02 | 0.085 | 0.22 |
| Phase coupling effect (d)( | 0.11 | 0.11 | 0.11 |
| Total line side voltage $U_L$ (e=b+c+d) (pu) | 1.13 | 1.20 | 1.34 |
| Recovery voltage across the breaker (f=a+e) (pu) | 2.115 | 2.16 | 2.33 |

(*) Normally for 500 km the line is compensated.

Table 1 : Influences of Ferranti effect, phase coupling and voltage jump during line-charging current breaking operation.

Figure 7 is a typical oscillogram of a 400 kV double circuit line of approximately 60 km being de-energised by an SF6 circuit-breaker. The switched line was Red, Yellow, Blue top to bottom phases whilst the adjacent energised line was Blue, Yellow, Red top to bottom phases.

The traces are source side voltage, line current and line voltage for each phase in turn.

The line current traces are basically sinusoidal up until the current separation point (Datum A) which is approximately 1 ms prior to the Red phase current zero (Datum B). Because the arc duration on Red phase is so short there is no current forcing or distortion as this current approaches zero, whereas on the Yellow and Blue phases, where there are longer time intervals before their current zeros, there is appreciable current forcing and distortion. Note that Yellow (Datum D) and Blue (Datum C) current zeros are not coincidental because of the unearthed component of the line equivalent circuit.

Line side voltages are sinusoidal up until current extinction on that phase, although circuit-breaker arc voltage does introduce a small modification to the waveform. Following current extinction the line side voltage takes a complex form consisting of several stages. The main component of this voltage is the dc trapped charge left on the line. However, whilst current is still flowing in other phases of the switched line, the cleared phase line voltage is further modified by the coupling effect from these other phases. Reference to figure 7 shows that during the period between B and C, the Red phase line voltage continues to increase due to coupling from Yellow and Blue phases, and during the period between C and D, the Red and Blue phase line voltages are modified by coupling from the Yellow phase. This coupling causes a further increase in the Red phase line voltage and a decrease to the Blue phase line voltage.

After Datum D there is no further voltage modification from the switched line because all currents are extinguished but now the voltage coupling from the adjacent energised circuit comes into effect. On this particular configuration it can be seen that the coupling is much stronger on Red phase.

The source side voltage remains at a level of 1 pu. The oscillogram shows the increase of line side voltage on the first phase to clear due to coupling from the other two phases, i.e. Datum D which is 1.21 pu. The additional increase of voltage due to coupling from the adjacent energised line is 1.36 pu at Datum E which coincides with the peak source volts of opposite polarity, and reaches a maximum of 1.39 pu at point F.

Figure 8 is an oscillogram of an earlier test switching the same line as above using an earlier version of the SF6 circuit-breaker, which includes a restrike on Red phase. It clearly shows the amplitude of the restrike current to be many times that of the power frequency current and how complicated the voltage oscillations become after a restrike, and why they are difficult to be correctly represented in the laboratory. It also shows that the restrike occurs before the source side voltage peak and that the restrike current lasts for three loops (see 3.1.3.).

Another example of a field test (at 60 Hz) is given in Figure 9 and in its expansion shown in Figure 10. The line side voltage of the first cleared phase, because of the coupling with the two other phases, of the presence of a second circuit and also of the physical configuration of the line with phases composed of multiple conductors, rises up to 1.5 pu. Here also are clearly visible the Ferranti effect, that gives a modest contribution to the peak line voltage, and the power frequency oscillation due to the other circuit. Therefore the recovery voltage across the first pole to clear is 2.5 pu as shown in Fig. 11.

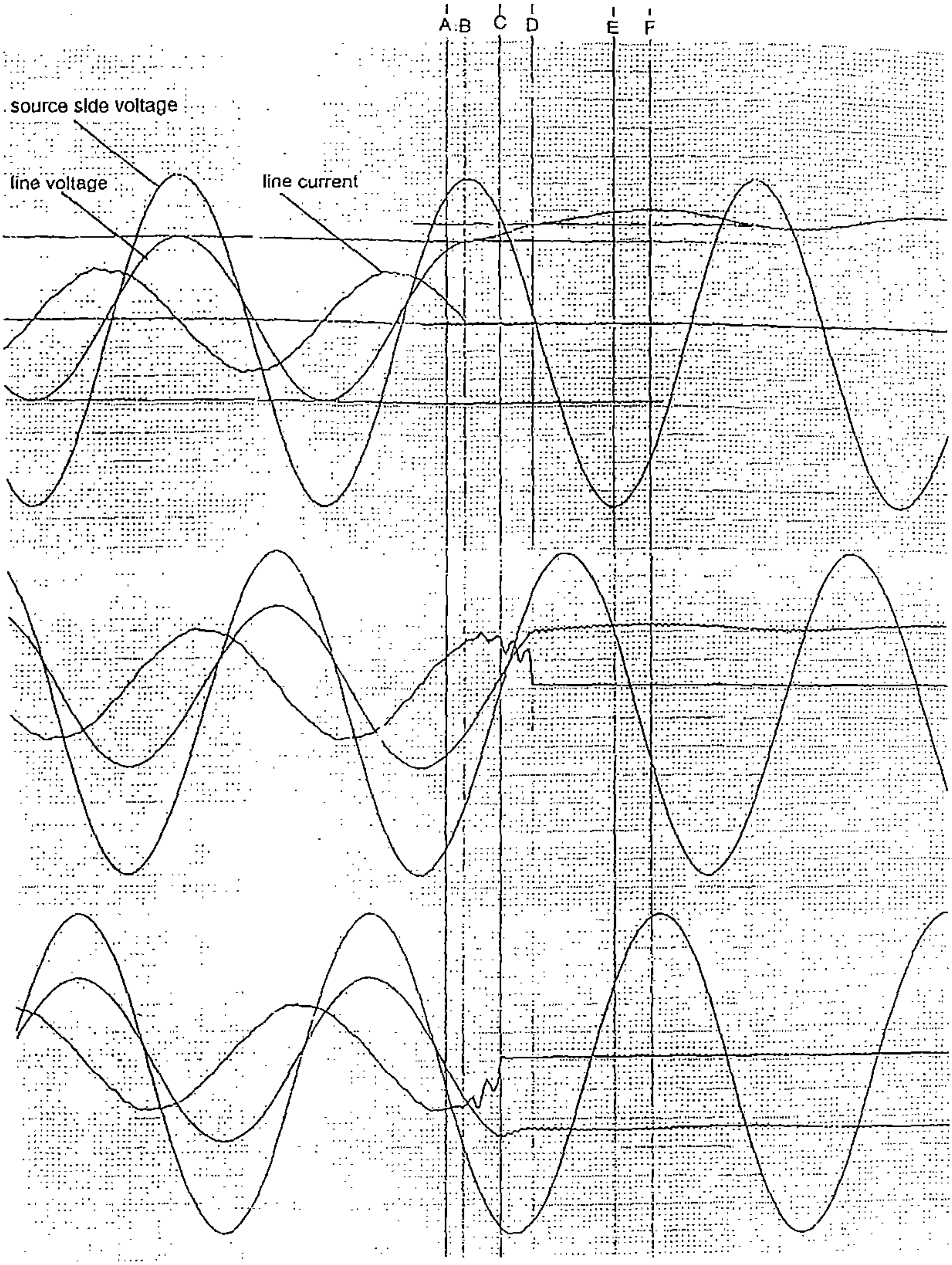


Figure : 7 (1) current; (2) line voltage; (3) source voltage - opening operation without restrike

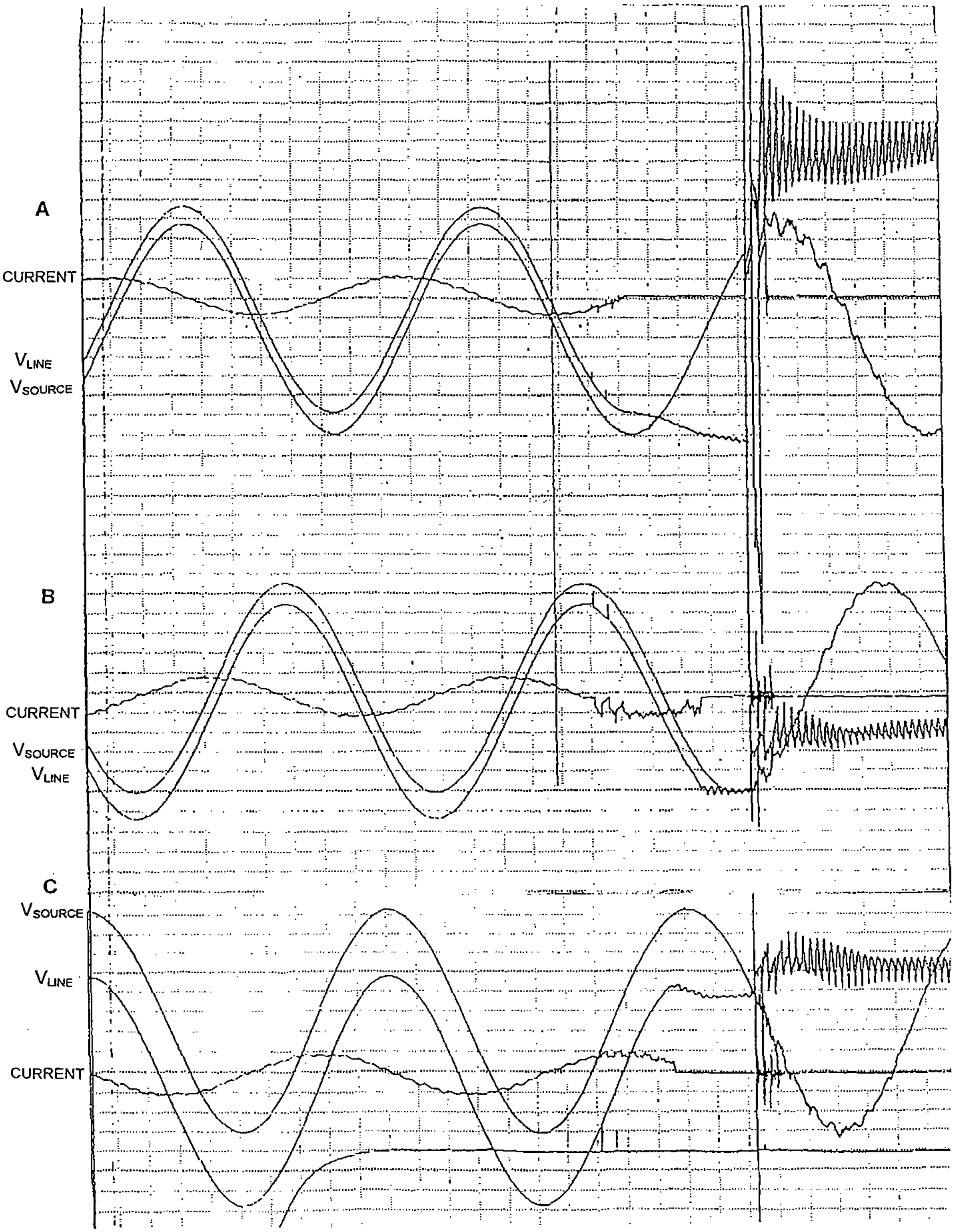


Figure : 8 current, line voltage and source voltage for an opening operation with restrike

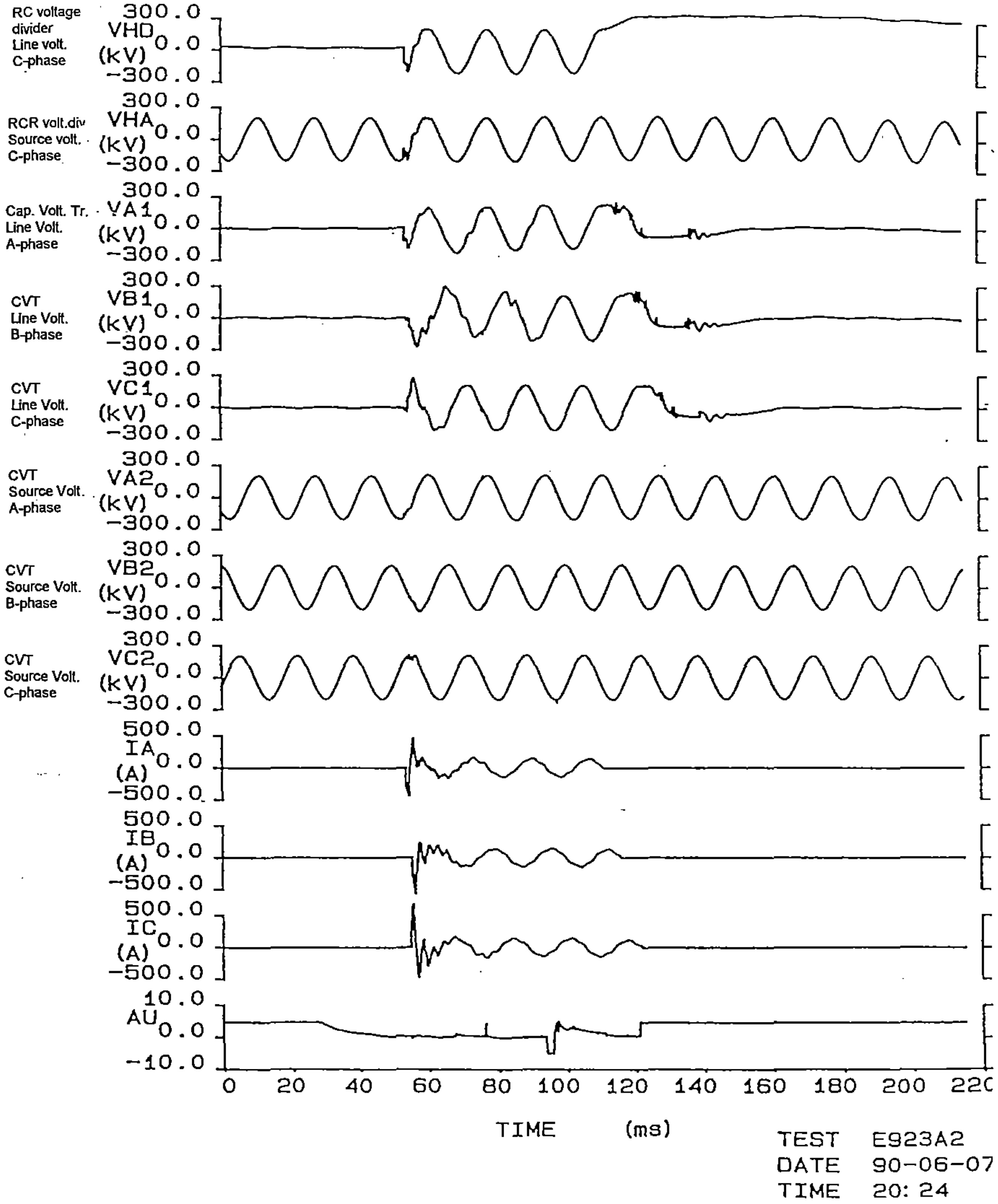


Figure 9 : opening operation without restrike

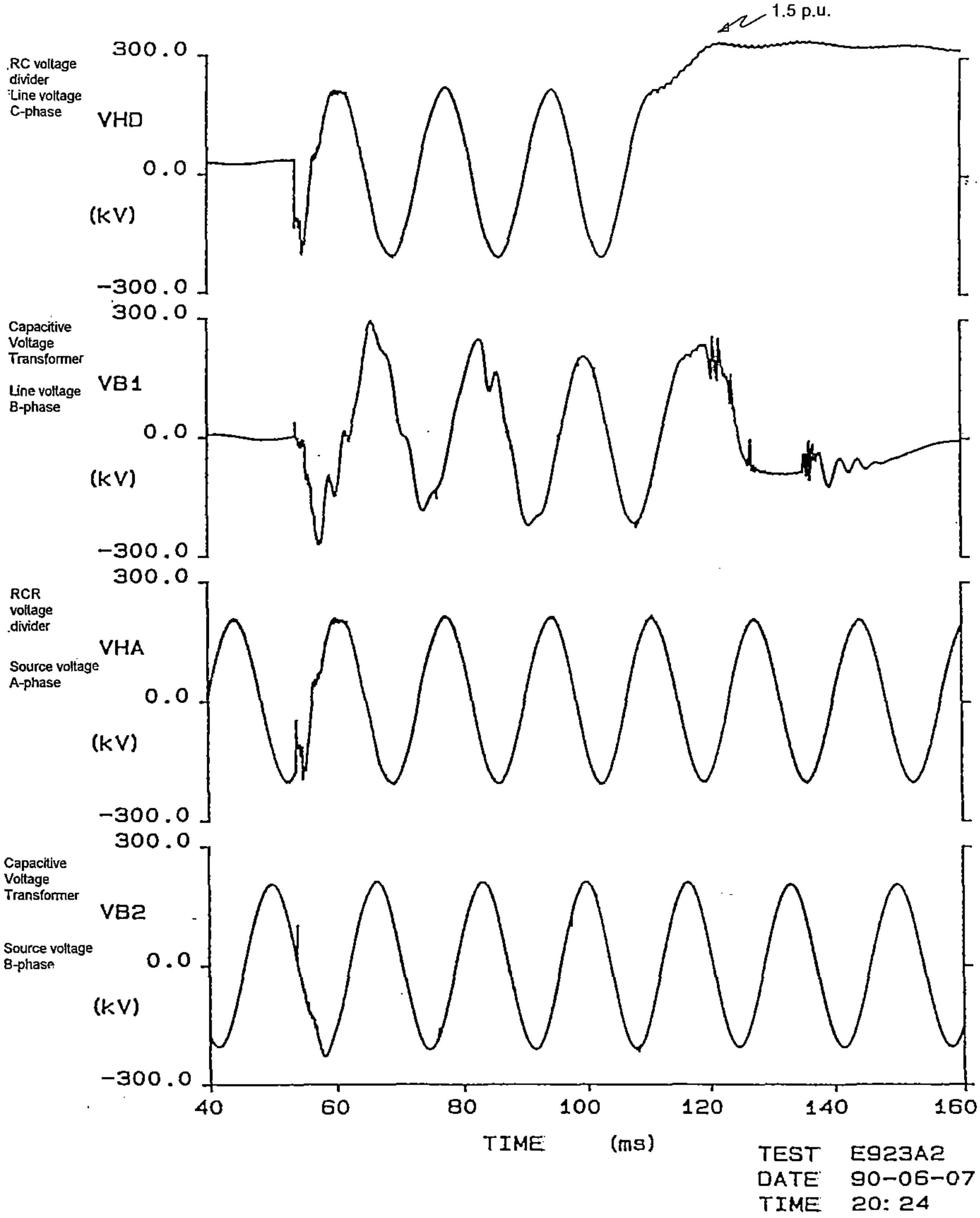


Figure 10 : opening operation without restrike

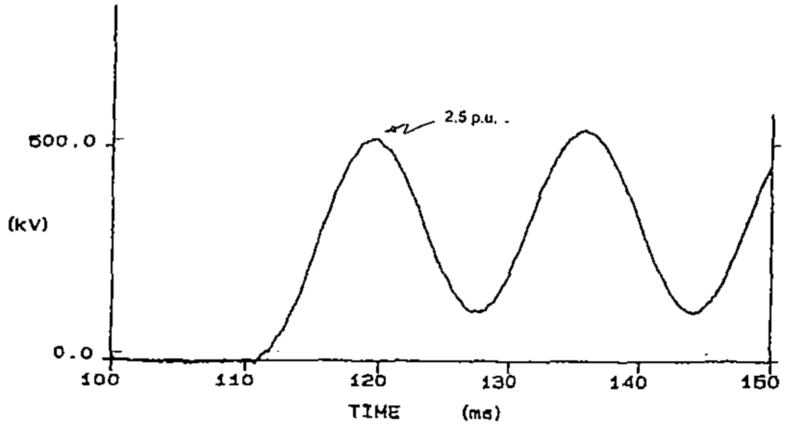


Figure 11 : recovery voltage across the circuit-breaker

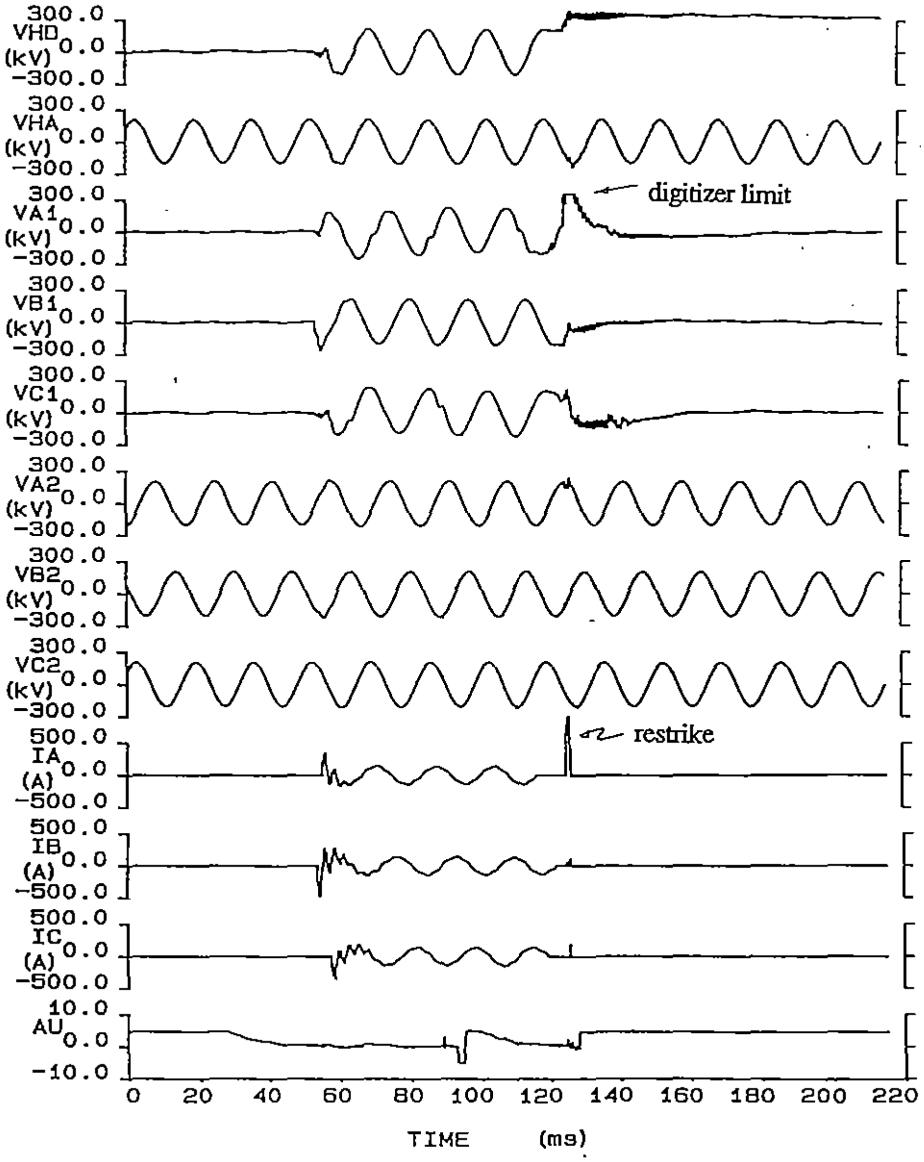


Figure 12 : opening operation with restrike

Figure 12 shows an energization of the same line followed by its tripping by a protection after 4 cycles. A restrike occurs on A-phase 8.3 ms after the current interruption. The transient of the line side voltage after restrike is not correctly reproduced, due to the limits of voltage measurement but a peak voltage between 2.5 and 3.0 pu is realistic.

As far as current wave shape is concerned, a typical distortion is visible on figures 9 and 12. The current harmonic content is higher than the voltage harmonic content, as $i(f) = C2\pi f\ U(f)$ (see /3/ and 4.1.2).

One can conclude that **the maximum stress after half a period across an opening circuit-breaker usually reaches 2.2 - 2.3 pu for single-circuit lines**, and thus is covered by IEC which indirectly asks for 2.3 - 2.4 pu in case of a grounded neutral source. However, **this voltage is higher - 2.4 pu - 2.5 pu - when the line has several circuits and increases with line length.**

## 3.3. Compensated lines

### 3.3.1 Compensation by shunt reactor

The term is generally understood to mean the use of shunt reactors to compensate a portion of the line charging MVAr. They are used for steady-state voltage control but are also effective in reducing switching surges to a considerable degree.

Without shunt reactors, the trapped charge may be considered almost constant; in practice discharge will occur via magnetic potential transformers and due to the presence of corona or pollution. With shunt reactors, the main frequency of the oscillation, determined by the equivalent inductance of the shunt reactors and the capacitance of the line, will be close to the power frequency while discharge via the magnetic potential transformers is low. Thus only line and reactor losses are effective in line discharging, producing a voltage decay.

If the line is fully transposed, there are two main natural frequencies in the oscillation of the phase-to-ground line voltages; the dominant frequency has an amplitude approximating to the source phase-to-ground peak voltage while the other main frequency, determined by the zero sequence equivalent capacitance of the line oscillating with the reactances, has a lower amplitude. For the untransposed line, more frequencies are involved; for instance in the horizontal configuration more frequencies have been noted on the two outer phases where beats between them can cause overvoltages up to 1.7 pu on one of these phases.

The recovery voltage waveform across the breaker is thus determined by the source voltage, which is sinusoidal of constant amplitude at rated frequency, and the line voltage which is of complex form but will have a main component, which is oscillatory with a frequency close to the source rated frequency, amplitude modulated due to energy exchange between phases, and decaying. The result of these various effects is that, in general, the breaker recovery voltage waveform is a beating oscillatory waveform starting from a low level immediately after interruption, with maxima approximately two times the peak of the source voltage. Under certain conditions, this figure could be exceeded but those maxima occur when the breaker is fully open due to the time required for the beat oscillation to build up to the maximum and, hence, **the switching of compensated lines should not present difficulties for the breaker**.

For circuit-breakers fitted with shunt opening resistors, these are effective in reducing the trapped charge on an uncompensated line and, hence, they ease the duty on the circuit-breaker; for highly compensated lines, their effect is negligible.

The power frequency overvoltage of a compensated no-load line, when the line is still connected to the network, decreases with the increase of the compensation factor /8/. A simplified analysis of such overvoltage takes into account the line phase coupling $C_0/C_1$ and the reactor arrangement $L_0/L_1$ /9/. The ratio between the zero and the direct sequence line capacitance is dependent on line bundle, distance between phases and conductor height. The value of the ratio between the zero and the direct sequence shunt reactor inductance is chosen during the line project in order to satisfy not only the overvoltage requirements during line disconnections but also taking into account the impact of the specification of the eventual fourth leg of the reactor on the total cost of the reactor bank and also its interaction with other transient effects. The conclusion is that if $L_0/L_1 \geq C_0/C_1$ the overvoltage can be equal or even lower than the one obtained for the same line but without the compensation.

Figure 13 presents the voltage waveform that results from the disconnection of a line with and without compensation in a 500 kV system diagram by EMTP simulation. In this case the voltage peaks are of the same order of magnitude, the uncompensated case being 6% higher than the compensated one. As can be observed in Figure 13 c), the recovery voltage incorporates a low frequency component originated by the interaction between the shunt reactances and the line capacitance.

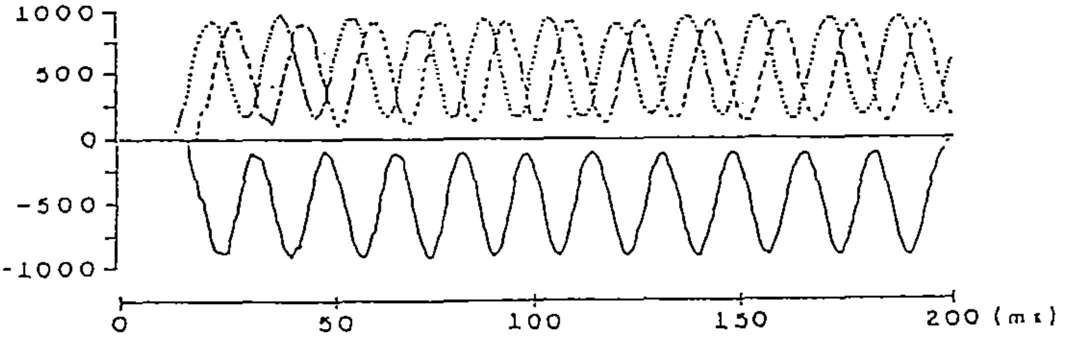


Fig.13a): Uncompensated line disconnection; recovery voltage across the circuit-breaker

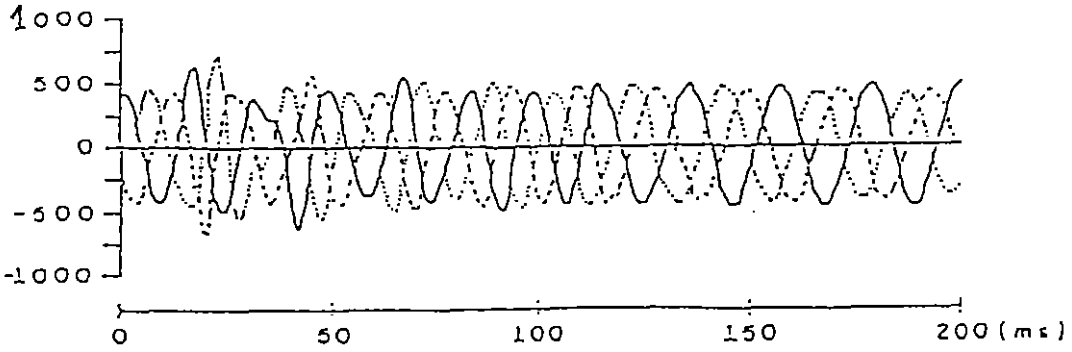


Fig.13b): Compensated line disconnection; line side phase voltages

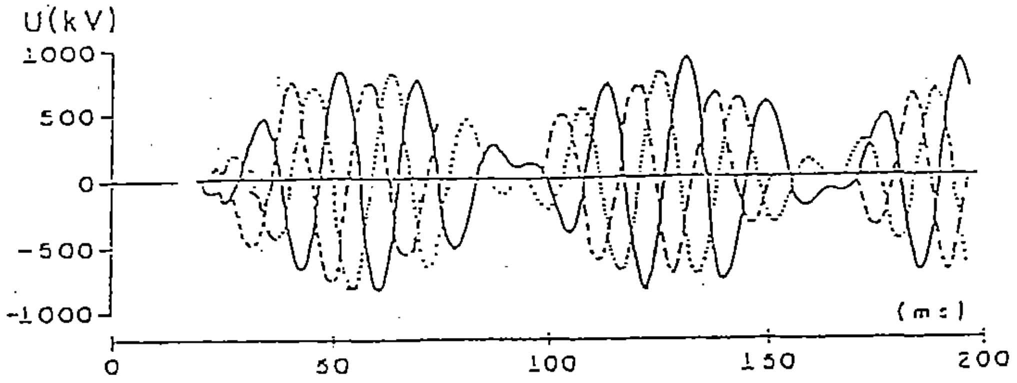


Fig.13c): Compensated line disconnection; recovery voltage across the circuit-breaker

The beating of the trapped charge at the receiving end, equipped with reactor, of a 220 km - 750 kV - 60 Hz line is also shown on the field test oscillograms of Fig. 14. The oscillation frequency after the line switching is around 40 Hz.

Note that the closing operation of the circuit-breaker equipped with closing resistors causes peak values of the phase voltages around 1.1 pu.

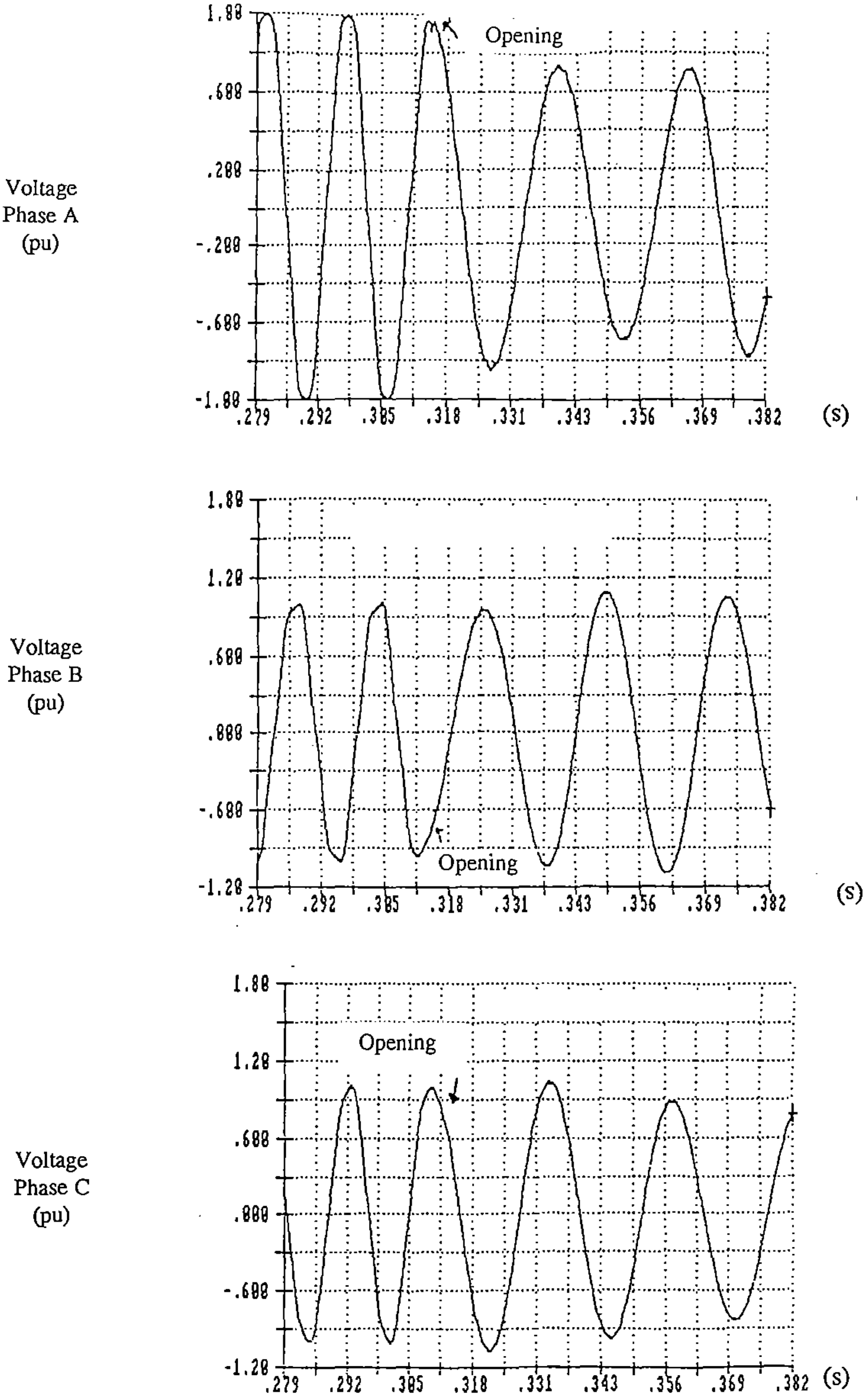


Fig. 14a): Phase voltages after opening operation at the end of a line compensated with shunt reactors

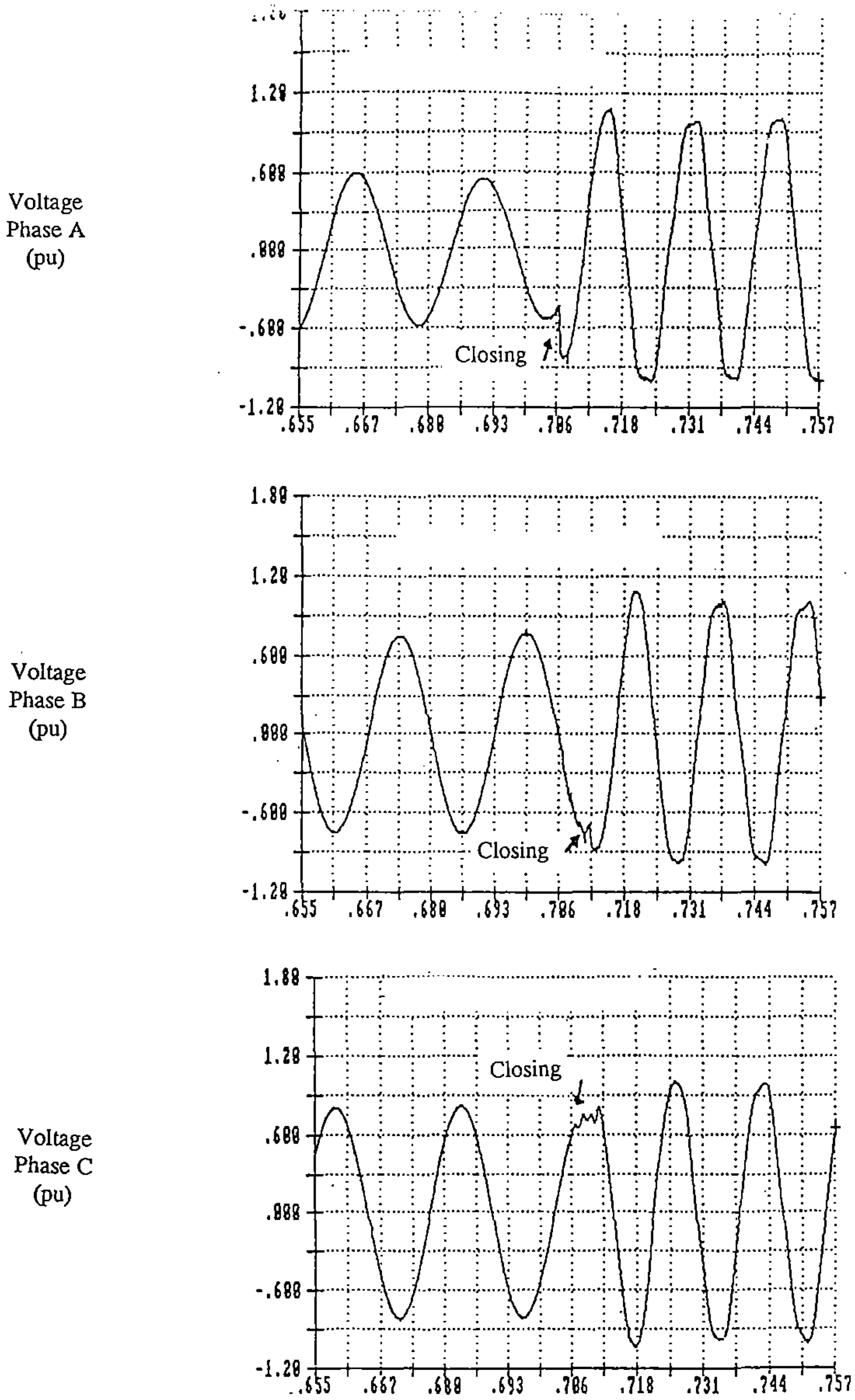


Fig. 14b): Phase voltages after closing operation at the end of a line compensated with shunt reactors

### 3.3.2. Series compensation

Series capacitors, installed at the middle or at one end of the line, allow increased transmission capability by decreasing the voltage difference between the supply and the open end of the line.

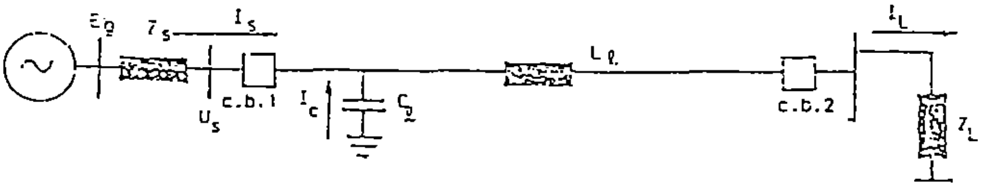
Therefore, after switching off the no-load line, the recovery voltage across the breaker is less modified by the superimposed travelling waves (caused by the Ferranti effect) than without compensation and its peak after half a period is reduced.

### 3.4. Load rejection

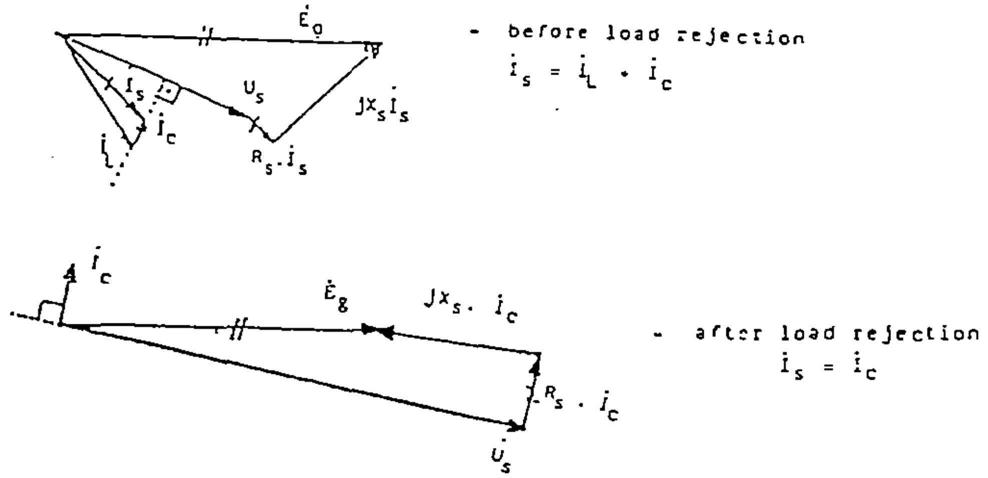
Fault clearing and protection malfunctioning are generally the main reasons leading to load rejection. Shortly after the remote circuit-breaker has disconnected the load, the circuit-breaker at the source side bus may be asked to switch off the no-load line.

A demonstration of the load rejection effects and the main parameters influencing it is given in Figure 15. Due to the normal inductive characteristic of the loads and also considering that the reactive power injected in the network by the transmission lines is kept below adequate values by means of compensation, the generators normally operate overexcited. Hence, the internal voltage $E_g$ is kept higher than the terminal voltage $U_S$, as shown by the phasorial diagram in Figure 15-b (before load rejection).

If, for any reason, the circuit-breaker 2 is opened, the voltage $U_S$ at the sending end of the line jumps to a higher level, due to the sudden change of the voltage drop in the source impedance $Z_S$. The interruption of the load current $I_L$ reduces $I_S$ to its line charging component $I_C$, increasing the terminal voltage $U_S$, as shown in Figure 15-b (after load rejection). Consequently, the reactive power generated by the line also increases, aggravating the over-excitation condition, which leads again to a further rise of $U_S$.



(a) - Simplified network



(b) - Phasorial diagram

Fig.15: Representation of the voltage rise due to a load rejection

The load rejection overvoltage waveshape may be generally classified in three different time domains, as shown in Figure 16. The transitory period is subsequent to the load loss and lasts less than two cycles. The temporary overvoltage is originated by the sudden voltage change at the generator terminal, due to its internal voltage. The influence of the voltage and velocity controls only appears by the end of this period. The harmonics generated by transformers and reactors may increase the severity of the overvoltages. Besides that, the interaction between the line capacitances and the inductive reactance of the saturated elements may lead to the development of ferro-resonance. Finally, the voltage tends to return to its normal level as a consequence of the control system actuation. However, should the generator excitation not be able to absorb the reactive power of the system, the voltage will tend to increase further due to the self-excitation phenomena.

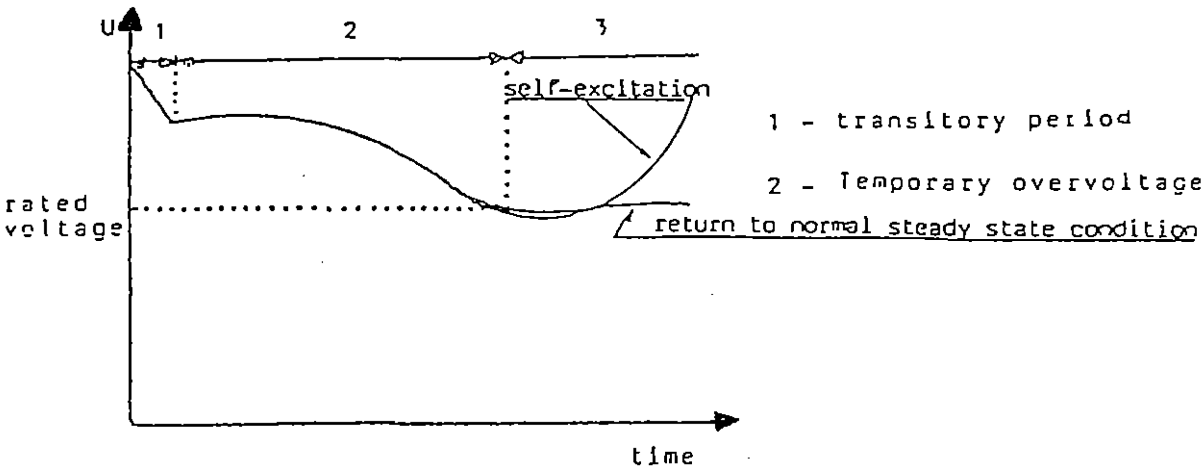


Fig.16: Generalized envelope shape of the load rejection overvoltage, characterized by three distinct domains /10/.

On weak systems, whose topology is rather radial, the temporary overvoltage may reach 1.4 pu /9,11,12,13/. Considering the protection times and the circuit-breaker interruption time, it appears that the line is normally disconnected during the temporary overvoltage period and a maximum line peak voltage of 1.4*1.2 pu can occur resulting in a recovery voltage across the first pole to clear of 3 pu or even higher in the case of double circuit lines. However, on meshed networks with strong generation and not very long lines, the temporary overvoltage is normally lower than 1.1 pu.

In some specific system conditions, the ferro-resonance or some voltage oscillations during the temporary overvoltages period may significantly influence the initial part of the recovery voltage. However, the consequences of it on the switching behavior of the circuit-breaker will depend on specific characteristics of the circuit-breaker and on the initial recovery voltage shape. Generally, no problems are foreseen for modern $SF_6$ circuit-breakers during the above mentioned regime.

### 3.5. Healthy phases switching

Healthy-phases switching is one of the most common fault switching conditions in the circuit-breakers daily life. It can be described taking into consideration the diagram of Figure 17.

When there is a fault in a transmission line, the circuit-breakers are called to isolate it from the network. The first circuit-breaker to open (CB1) has to interrupt a short-circuit in one (or two) phase(s) and the load current in the remaining phase(s). In the same way, the last circuit breaker to open (CB2), must interrupt a short circuit current in one (or two) phase(s) and the line charging current in the other one(s). The latter condition is the so called healthy phases switching.

The main stresses imposed on the circuit-breaker during a healthy-phases switching are the rather high recovery voltages. They result from the combination of the system voltage increase in the healthy phase, due to the presence of a short circuit on one (or two) phase(s): this process gives a voltage shift of the neutral point and thus modifies the phase-to-ground voltages on the healthy phase(s).

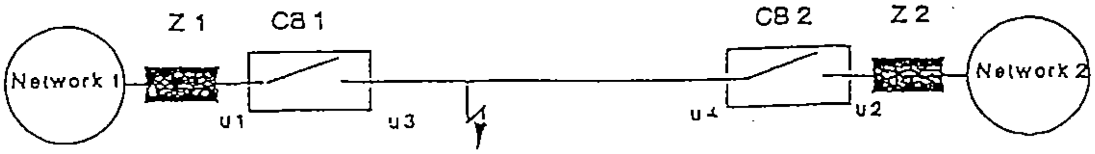


Figure 17 : Transmission circuit : u1, u2 voltages on the busbar side;
u3, u4 voltages on the end of the line; z1, z2 impedances of the system;
CB1 breaker opens first; CB2 second opened breaker.

When a fault occurs on the line, both circuit-breakers get a trip signal to clear the fault. CB1 opens first disconnecting two different networks with a fault current in one phase and a nearly normal current in the two other phases. This gives a stress on CB1 which is covered in existing IEC by the short-circuit test duties.

CB2 has then to clear a fault current in one phase and a capacitive current, with a higher voltage depending on the grounding factor of the network, in the other two phases. Earlier CIGRE studies (WG 13-05) have shown that the highest voltage occurs on the unfaulted phase which interrupts prior to the faulted phase and the highest capacitive current occurs on the last phase to interrupt when the faulted phase is the first to interrupt. In addition, they have established that:

- The main influence on the transient recovery voltage across the circuit-breaker in an earthed neutral system is given by the length of the line, the fault level and the ratio between the zero and the positive sequence reactance ($X_0/X_1$).

- For solidly earthed systems ($X_0/X_1 = 1$) with high fault level (about 50 - 100%) and short transmission lines with lengths up to 200 km, the peak recovery voltage across the circuit-breaker is in the region of 2.4 pu.

- For systems approaching the upper limit of solid earthing ($X_0/X_1 = 3$), with high fault levels and line lengths up to 300 km, the peak recovery voltage across the circuit-breaker is in the range of about 2.8 to 3.0 pu.

- For earthed neutral systems with low fault levels, the peak recovery voltage across the circuit-breaker may be higher. Different influences are interlinked in a very complex way and therefore it is not possible to give general rules. For instance, the saturation of a transformer may decrease or increase the peak recovery voltage.

The phase-to-ground voltage on the line side of CB2 is given by three different effects /10/ and can be expressed by the product of 3 coefficients:

$k_1$ = due to the grounding condition : ≤ 1.4 for earthed neutral systems which are the most common on HV systems and 1.7 for isolated neutral systems.
$k_2$ = associated with the level of the pre-fault load (usually <1.1 see sub-clause 3.4)
$k_3$ = due to coupling between phases and other lines (<1.3 see sub-clause 3.2)

Measurements have shown that the combination of **overvoltage factors in earthed neutral systems do not usually exceed an overvoltage factor 1.4 which means a maximum recovery voltage 2.8 pu.**

However, if the protection system operates in a way to give the tripping impulse at the same time to the circuit-breakers on both ends of the line, than the CB2 may open during the oscillation of the line before the steady state condition is achieved. Attention must be paid to the resulting stresses. In this case the current and voltage waveshapes depend very strongly on the exact line parameters and also on the time delay between the circuit-breakers. A computation of the possible overvoltage and current stresses for breakers and system is necessary. In practice, this situation should be rare.

Healthy phases switching can also be encountered in simple cases involving only one circuit-breaker clearing a faulted open line. The oscillogram in Figure 18 shows the line side phase voltages of an open line and the capacitive current in C-phase of the line which is leading the voltage by practically 90 electrical degrees. A short circuit occurs after two periods. The circuit-breaker is opened and the healthy phases A and B are cleared before the faulted C-phase. The influence of the still energized phases and the Ferranti effect increases the peak recovery voltage of B-phase to nearly 1.4 pu. The interruption of the fault current in C-phase causes a damped sinusoidal oscillation of the corresponding voltage. It is interesting to note this sinusoidal oscillation influences the dc value of the line voltages in the healthy phases and, when it is in phase with the Ferranti effect, it increases the voltages of A-phase and B-phase to nearly 1.3 pu. This case clearly shows that the voltage stress is not necessarily increased on the healthy phases, as compared to the three-phase normal situation, because it depends on how the single phase-circuit affects the neutral point voltage shifting.

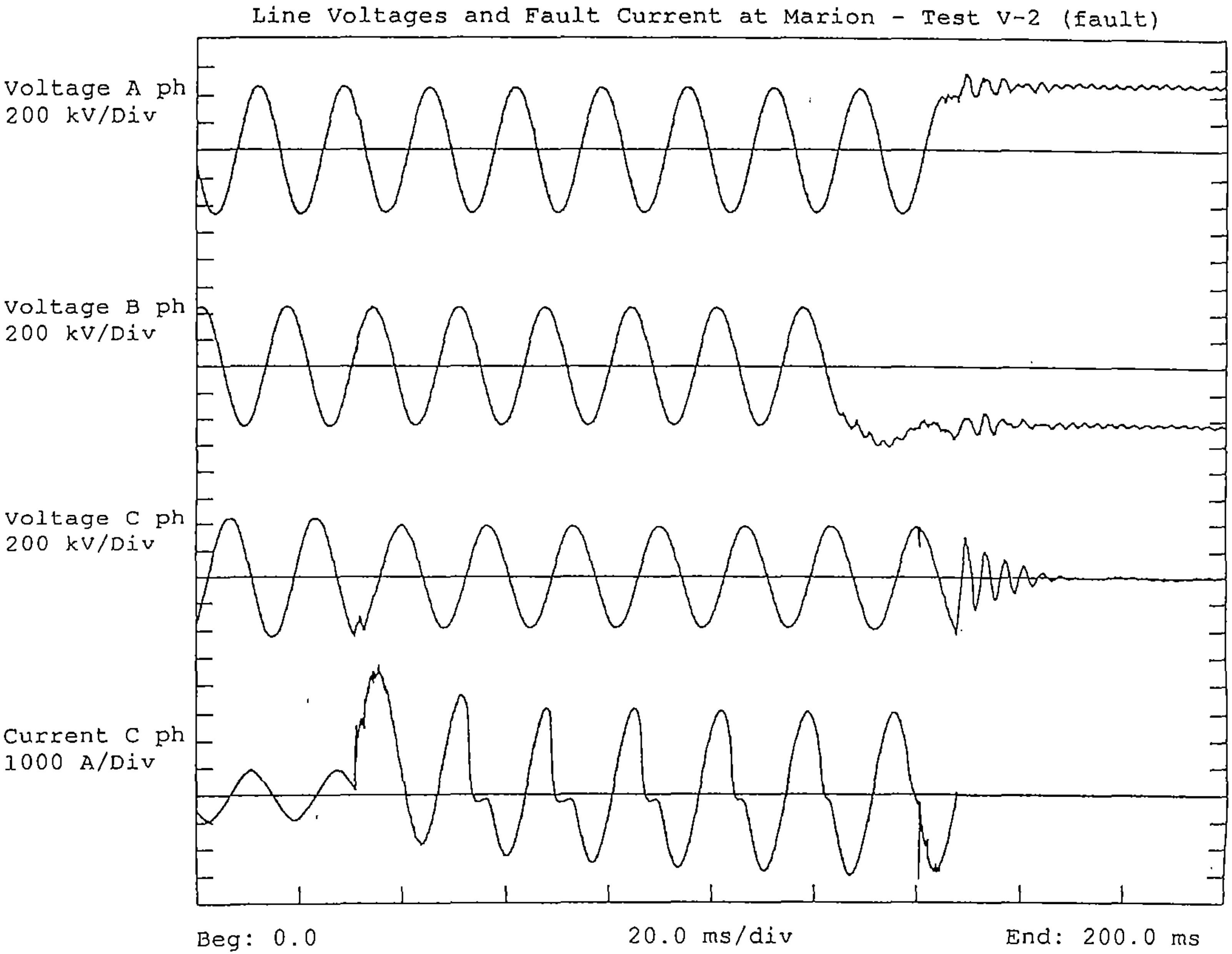


Fig. 18: Short-circuit on C-phase and switching of healthy phases

Another example of healthy phases switching is given by the oscillograms of Figures 19 and 20. They compare switching of a 550 kV unloaded line, equipped without or with compensation reactors, in the presence of a single phase-to-ground fault in B-phase. The line is 315 km long and the fault is situated 200 km from the source. The phase interruption sequence is C-B-A and the short-circuit is initiated one minute after the line energization.

The oscillograms in the case of an open line (without reactors) show the B-phase short-circuit current. After the interruption in C-phase, a reignition occurs in B-phase, while an early interruption of A-phase can be observed, therefore the influence of the change of charge on C-phase may be attributed for the most part to B-phase. The highest recovery voltage peak on C-phase across the circuit-breaker appears about 8 ms after interruption and is 2.73 pu. This value has been increased by the reignition.

The oscillogram of Figure 20 refers to the same line with shunt reactors at the remote end (note that the time scale is about doubled in comparison with Figure 19). The interruption sequence is again C-B-A without reignition. After 3.5 periods the B-phase short-circuit is cleared and, while the B-phase recovery voltage waveshape becomes quickly sinusoidal, the A- and C-phase recovery voltages show a double sinusoidal trend resulting from the beating of the power frequency source side voltage and of the line side oscillation between the inductance of the shunt reactor and the line capacitance (as explained in sub-clause 3.3). The peak recovery voltage in C-phase (2.53 pu) is not reduced much in comparison with the case without reactors, but occurs about 40 ms after the interruption causing no difficulty for the circuit-breaker.

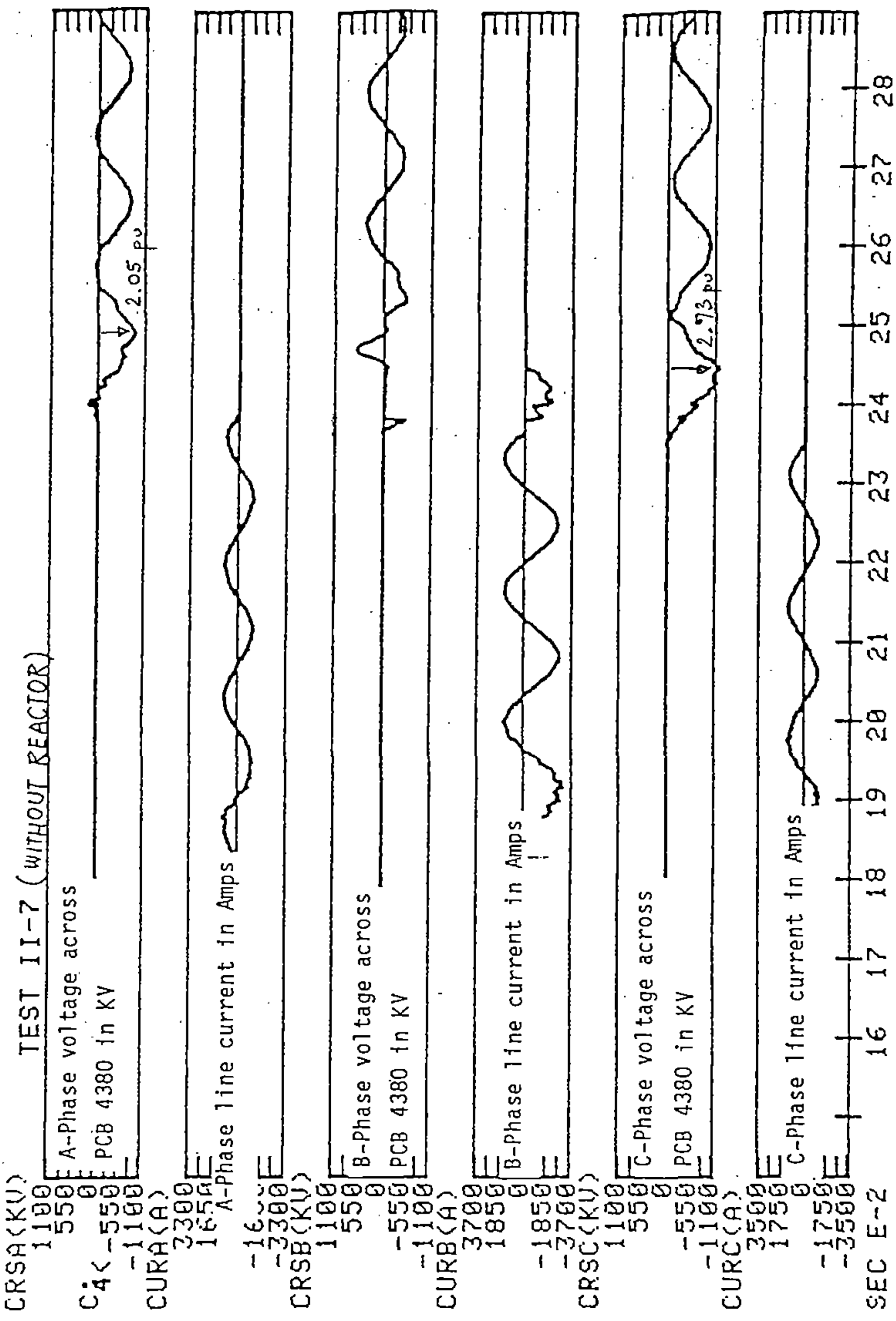


Fig. 19: Short-circuit on B-phase and switching of healthy phases without reactor

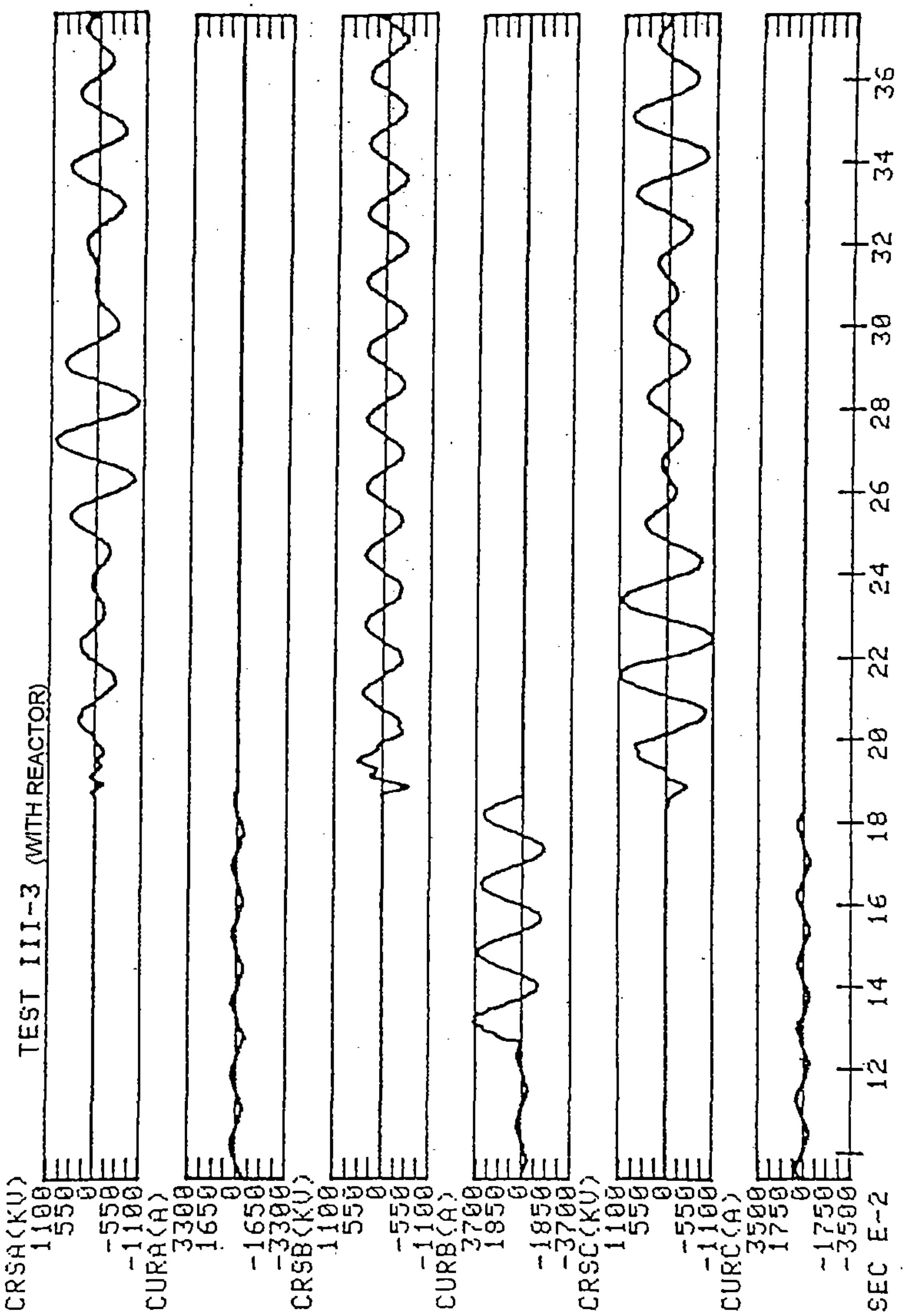


Fig. 20: Short-circuit on B-phase and switching of healthy phases with reactor at end line

### 3.6. Practical consequences

- The physical phenomena such as the different voltages of the source and line sides, the coupled voltages due to the other phases or to a parallel energized line on the first cleared phase and the travelling waves superimposed on the recovery voltage can result in an increased voltage during switching.

- The initial voltage jump and the rate of rise of the first wave due to the Ferranti effect can cause an early reignition, thus, reducing the probability of restrike of the circuit-breaker.

- The series compensation limits the voltage increase at the end of the line and the amplitude of the travelling waves will be lower than in the corresponding uncompensated case.

- The shunt compensation, reducing the line current, also limits the amplitude of the travelling waves. The line oscillates at a frequency close to the rated frequency reducing the recovery voltage across the circuit-breaker during the first half cycle.

# LINE-CHARGING CURRENT SWITCHING OF HV LINES

## STRESSES AND TESTING.

(Part 2)

Working Group 13.04*(Switching Test Methods)

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## Part 2

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## 4. - TEST CIRCUITS

### 4.1. Line-charging current switching tests are not easily performed.

### 4.1.1. Introduction and IEC limitations.

In testing, two aspects are generally considered : test circuits and test procedures. This second issue is covered in Section 5.

As far as capacitive current switching tests are concerned, four type-test duties are asked by IEC 56/14/. They need two source powers and two values for load currents. The line currents generally have low values (100 A - 500 A) compared with the values usually used in High Power Laboratories for short-circuit tests. One could then erroneously conclude that a capacitive current test circuit, for instance valid for the line switching, does not require large facilities. The two sub-clauses below examine the various difficulties, from the laboratory view point.

The main deficiency of the existing IEC 56, when considering test circuits, is that it does not clearly say that a circuit-breaker has to be restrike-free. Otherwise, the IEC alternative solution is to carry out a three-phase test with a real line of appropriate voltage and current. Due to several factors, among them the connection of the laboratory to a network (having the correct voltage rating), the availability of long lines and the cost, this solution is almost never used.

Restrikes generate overvoltages which may be onerous for the network. The working group opinion is thus to advise the use of restrike-free circuit-breakers on networks at 245 kV and above. However, new and more sophisticated line model circuits which could enable laboratories to test restriking circuit-breakers can be envisaged, and are presented later in this chapter.

*Note* :

No specific work has been done by the WG to examine the particular stresses applied to three-phase GIS circuit-breakers when breaking the capacitive current of a line. However, this case must be handled with care to take into account the possible interactions between phases. An IEC guide for GIS circuit-breaker giving some guidance in this respect, for example about fault interruption, will be shortly issued.

### 4.1.2. Difficulties in obtaining a correct source circuit

As this paper is limited to HV and UHV systems, the associated laboratory line-charging switching tests are in practice performed single-phase. The source voltage is chosen as k . U/√3 where :

U is the rated voltage of the breaker,

k is a coefficient taking into account the various system conditions detailed in clause 3 ($1,2 \leq k \leq 1,7$).

IEC 56 requires two supply circuits, which should be very different :

- one giving a small short-circuit current, thus with a large short-circuit inductance. The source side voltage variation when switching (and thus the initial jump) is high, but limited to 10% of the test voltage by IEC.

- the other one giving a large short-circuit current so that the source side voltage variation when switching is as small as possible and at least below 5% of the test voltage. In practice, as the short-circuit power (Psc) used in High Power Laboratories for these tests is limited to 1000-3000 MVA, The source side voltage variation (ratio (U1 - Uo)/U1; see Figure 4) is often in the range of 2 - 4% as can be seen in table 2.

| Voltage variation<br>$\frac{U1-Uo}{U1}$<br>(%) | | Psc (MVA) | | | |
|---|---|---|---|---|---|
| | | 500 | 1000 | 2000 | 3000 |
| Rated (*) voltage U (and current) | 245 kV (125 A) | 3.9 | 2.0 | 1.0 | 0.7 |
| | 300 kV (200 A) | 7.2 | 3.8 | 2.0 | 1.3 |
| | 420 kV (400 A) | 16.3 | 9.5 | 5.2 | 3.6 |

(*) Test voltage = 1.2 U/√3

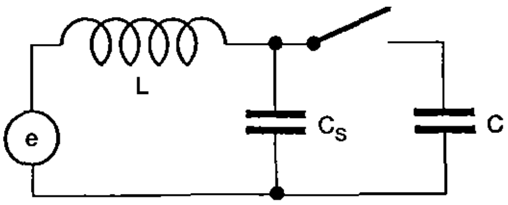
Table 2 : Source side voltage variation as a function of the short-circuit power of the source.

This means that these two supply circuits are not as different as it may appear at first glance : as the ratio between their voltage variations is quite often 2 - 3, their short-circuit power is also in the same ratio 2 - 3. It should therefore be sufficient to **only use one supply circuit, giving a limited voltage variation (< 5%).**

- Attention to the current wave shape has also to be paid when connecting the source side circuit to the load circuit in order not to have additional current zeros which modify the arcing time and the voltage applied across the breaker. This stray current superimposed to the power frequency current has two origins :

- It is generated by the source voltage harmonics, and amplified by the capacitive circuit : 2% of the 5th voltage harmonic means 10% of the current value.

- The resonance frequency of the circuit (see figure 21) must be chosen to be as remote as possible from the voltage harmonics of the source, which are odd values 3, 5, 7, 9 .... Adjusting the source power to obtain a resonance frequency which is an even harmonic of the power frequency is the convenient solution.



$$f = \frac{1}{2\pi\sqrt{L}\,(C + C_S)}$$

Figure 21: Influence of the resonance of the circuit.

- Besides these difficulties, the laboratories may also be limited by the available capacitance, which has to be designed to withstand the test voltage and also possible overvoltages associated with restrikes (for instance 3 pu). In practice, the biggest facilities in High Power Laboratories are limited to the test of a full pole of a 420 kV circuit-breaker (test voltage = 291 kV) breaking a line current of 400 A.

To overcome this limitation, unit testing is possible, which means that only a part of a multi-unit pole of a circuit-breaker is tested. This technique is often the only solution for UHV circuit-breakers. Due to the lack of information on the equivalence of the tests with actual situations, they have to be performed on the maximum number of units in series. However, it is often considered that unit testing is more severe : the voltage distribution is worse on a total pole at short arcing times due to mechanical spread of the units, this increases the probability of reignitions and decreases the probability of restrikes. Another possible solution is to use capacitive synthetic tests instead of direct tests (see 4.2).

### 4.1.3. Several line models are possible

#### 4.1.3.1. Representation of a line at power frequency.

The simplest representation of a line is a capacitor giving the proper current value at power frequency. Such a circuit is only valid to represent low frequencies phenomena (i.e : 0-100 Hz) occuring during switching operations, the circuit is not adequate to represent restrikes.

Nevertheless, this circuit or variations on this circuit such as resistor/capacitor or inductor/capacitor series connected circuits are almost always used in laboratories.

#### 4.1.3.2. Representation of a line for higher frequencies.

When there is a restrike, IEC 56 states that only three-phase tests performed on a real line of appropriate length are valid. As already said, the standard does not suggest a practical solution to test a non-restrike free breaker, as almost no High Power Laboratory or utility is ready to accept the very restricting solution of using a real line.

To overcome this difficulty, i.e to be in position to also test restriking circuit-breakers with components available in test laboratories, laboratories are looking for the simplest circuits able to represent the high frequency phenomena as accurately as possible.

Figure 22 shows the response of four circuits expressed by their impedance, as a function of the frequency :

1 : Basic circuit, composed of a capacitor.
2 : RC circuit.
3 : Four-branch model of a line, according to Figure 23.
4 : Real line.

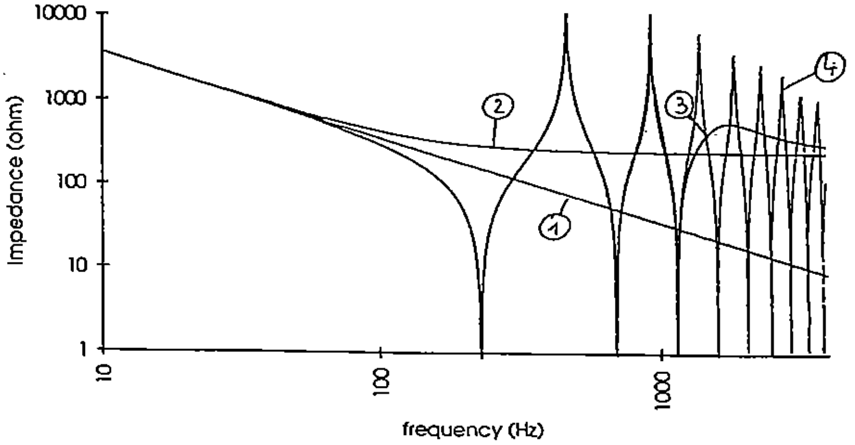
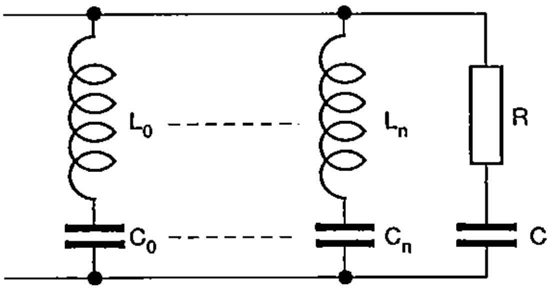


Figure 22 - Impedances of 420 kV - 400 A line models versus frequency.

Various representations of unloaded lines exist in the technical literature /17,18/. Figure 23 gives an example, in use for 10 years.



with

$L_i = \mathscr{L}/2$

$C_i = \dfrac{8\mathscr{C}}{\pi^2 (2i+1)^2}$

$R = \mathscr{Z}c$

$C = \mathscr{C} - \sum_0^n C_i$

$\mathscr{L}, \mathscr{C}$ total inductance and capacitance of the line

Figure 23 : Les Renardières line circuit.

One can conclude from figure 22 that a good representation of a line can be reasonably achieved with a limited number of circuit branches. The line has to be accurately modeled for frequencies up to one to some kHz. This is also useful if the voltage transients at closing or if the Ferranti effect of the line have to be represented.

### 4.2. Testing a restrike-free circuit-breaker.

#### 4.2.1. A capacitor is sufficient to represent a line.

When the aim of the tests is to check that the circuit-breaker does not restrike, a capacitor bank is sufficient to represent the line. This is the simple and usual case.

This circuit will not give the appropriate so-called inrush current at making. Derived circuits (resistor-capacitor, inductor-capacitor) are often used to limit the peak current. However, these circuits have one or even two drawbacks : firstly, they induce modifications of the overvoltage levels at closing, and secondly, the phase shift between voltage and current may be significantly modified in the case of the resistor-capacitor association, which should be prohibited.

#### 4.2.2. Synthetic tests.

Synthetic tests are possible when the method is limited to testing restrike-free circuit-breakers since a synthetic circuit is neither able to provide the energy dissipated in a restrike, nor represent the phenomena following a restrike.

Capacitive synthetic tests are now allowed by (amendment 1 of) IEC 56, which defines the voltage stress across the terminals of the circuit-breaker as TRV parameters.

A survey of the possible synthetic circuits, in use in the high power laboratories, was done by CIGRE /19/ and has been published in IEC 427 /16/. No new work has been started by WG 13-04, as it was not deemed to be necessary.

#### 4.2.3. Long lines switching.

Switching of long lines generally occurs at higher voltage levels for which the permissible overvoltages are limited. Thus, the circuit-breaker must be restrike-free to limit the stresses on the network. It can be tested with a simple line circuit such as a capacitor.

The test voltage is very high, compared to the single-phase voltage of the network because the user often asks for requirements (load rejection, breaking of healthy phases in the presence of a single-phase fault on the third phase, compensation of the line) exceeding the standard values. This reflects the strategic role of the line in the network.

While most of these requirements can be easily taken into account by an increase of the test voltage, they cannot in the case of a shunt compensated line. The voltage maximum may be obtained later than half a cycle, for instance after 40 to 80 ms because of the compensation of the line. This has a positive effect on the breaking capability of the breaker. A test circuit, called a balanced oscillating current injection circuit, as in figure 24, allows the circuit-breaker to be correctly stressed.

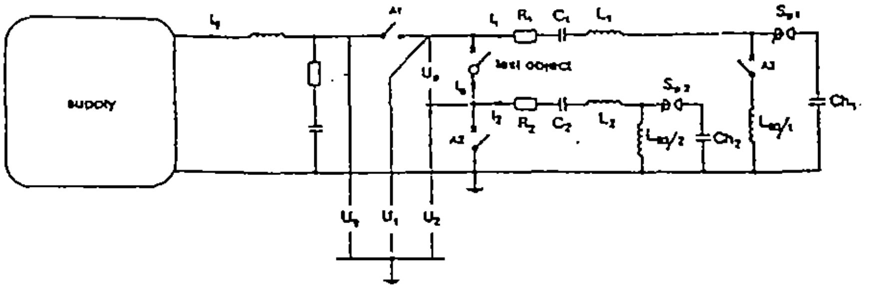


Figure 24 : Circuit for long line switching

It is composed of :

- a current circuit supplying the power frequency test current $I_g$ (for example 1000 A as in oscillogram Figure 25),
- the current injection voltage circuit 1 supplying the recovery voltage $U_1$ at time t1,
- the current injection voltage circuit 2 required to attain the $U_c$ value at time $t_m$.

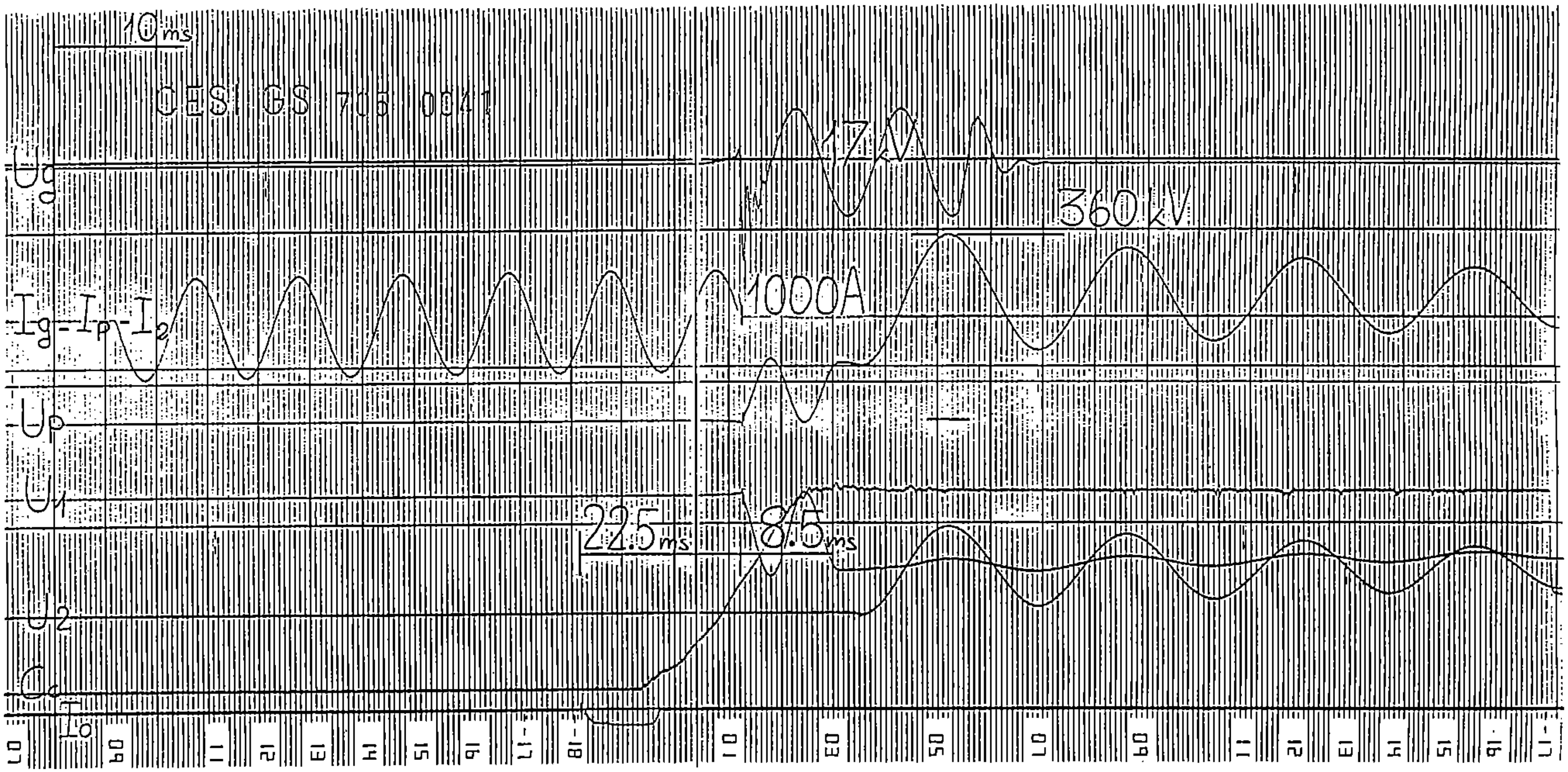


Fig. 25: Oscillogram of a capacitive test on a compensated line

Before the sequence of the operations, the auxiliary circuit-breakers A1, A2, A3 and the test circuit-breaker are closed.

The firing of the spark-gap $Sp_1$ at the predetermined power frequency current zero discharges the capacitance $Ch_1$ and $I_1$ starts to flow. $A_1$ breaks at the power frequency current zero, the test breaker clears the total current ($I_g$ + $I_1$) and the recovery voltage U1 is applied to its corresponding terminal.

The firing of the spark gap $Sp_2$ after a suitable time interval discharges the capacitance Ch2 and the current $I_2$ flows through the auxiliary breaker $A_2$.

The oscillating circuit 1 is switched by A3 on the second recovery voltage peak so that the rated voltage $U_1$ is applied across the test breaker.

Finally, A2 switches the current $I_2$ and the recovery voltage $U_2$ is applied to the other terminal of the tested circuit-breaker that withstands the total recovery voltage Up, composed of the direct value $U_1$ and the sinusoidal oscillation $U_2$.

### 4.3. Testing a non restrike-free circuit-breaker with a laboratory circuit

Let us consider the four circuits of figure 22 (case of a 420 kV circuit-breaker, breaking 400 A under 291 kV at 50 Hz), with a restrike after half a cycle. Figures 26 and 27 give the voltage and current transients computed during the first few milliseconds following the restrike.

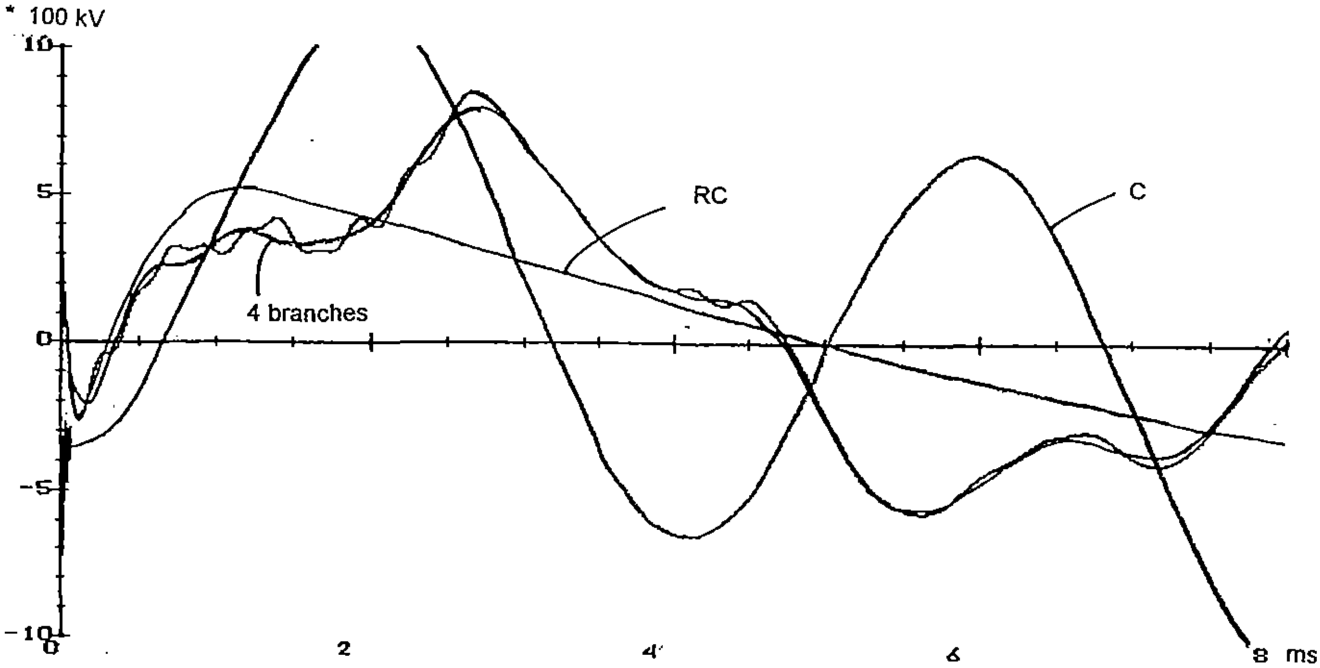


Figure 26 : Voltages after a restrike.

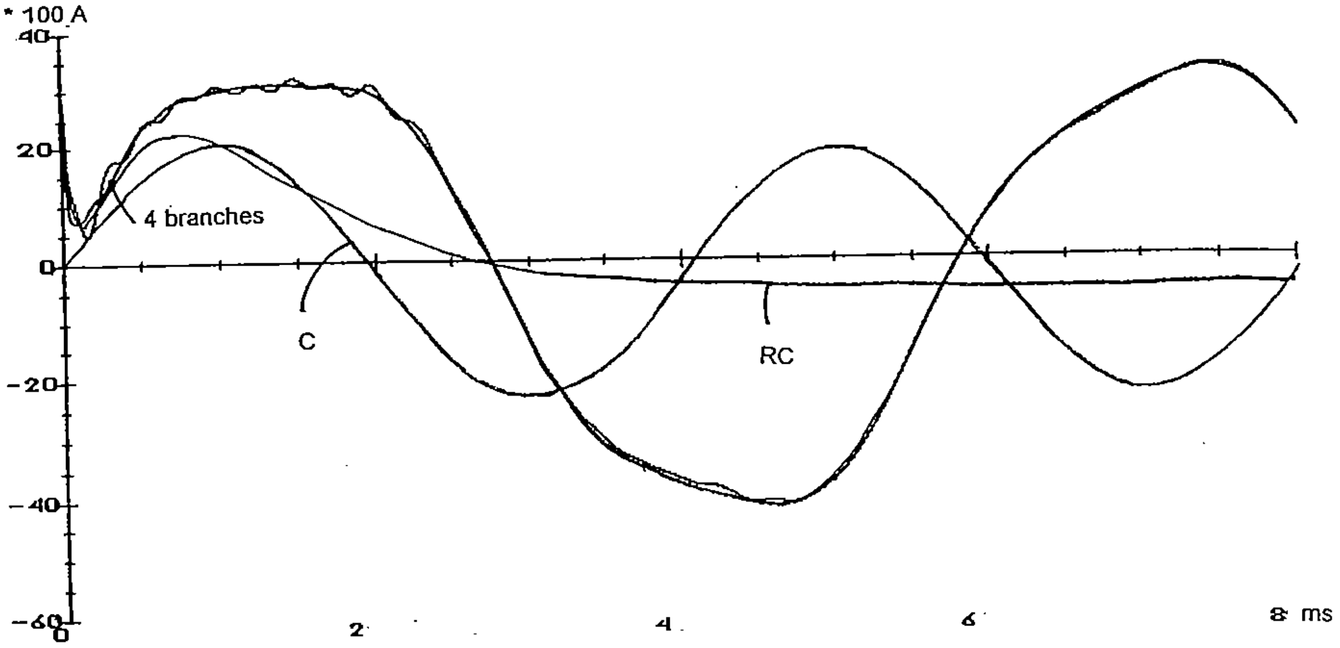


Figure 27 : Currents after a restrike.

These two figures confirm that a single capacitor is not sufficient to give the complex current and voltage wave shapes. The association of a resistor and capacitor in series is the worst solution : the free oscillation following a restrike is completely modified.

They also show that a reasonably simple line model is sufficient to generate the current and voltage transients : frequencies, current shape at current zeros and wave shapes. In addition, and because of the good representation of the impedance as a function of the frequency, the circuit reproduces the voltage stresses (TRV) when/if the circuit-breaker clears on one of the current zeros following the restrike.

Figures 28 and 29 are two test oscillograms, comparing the results of a 3-branch circuit and a real 85 km long line in case of restrikes : the voltages are comparable, including the transients after clearing a "high frequency" current.

One can then conclude that the voltages and current during and after a restrike can now be correctly represented in a single phase scheme by a circuit of reasonable complexity.

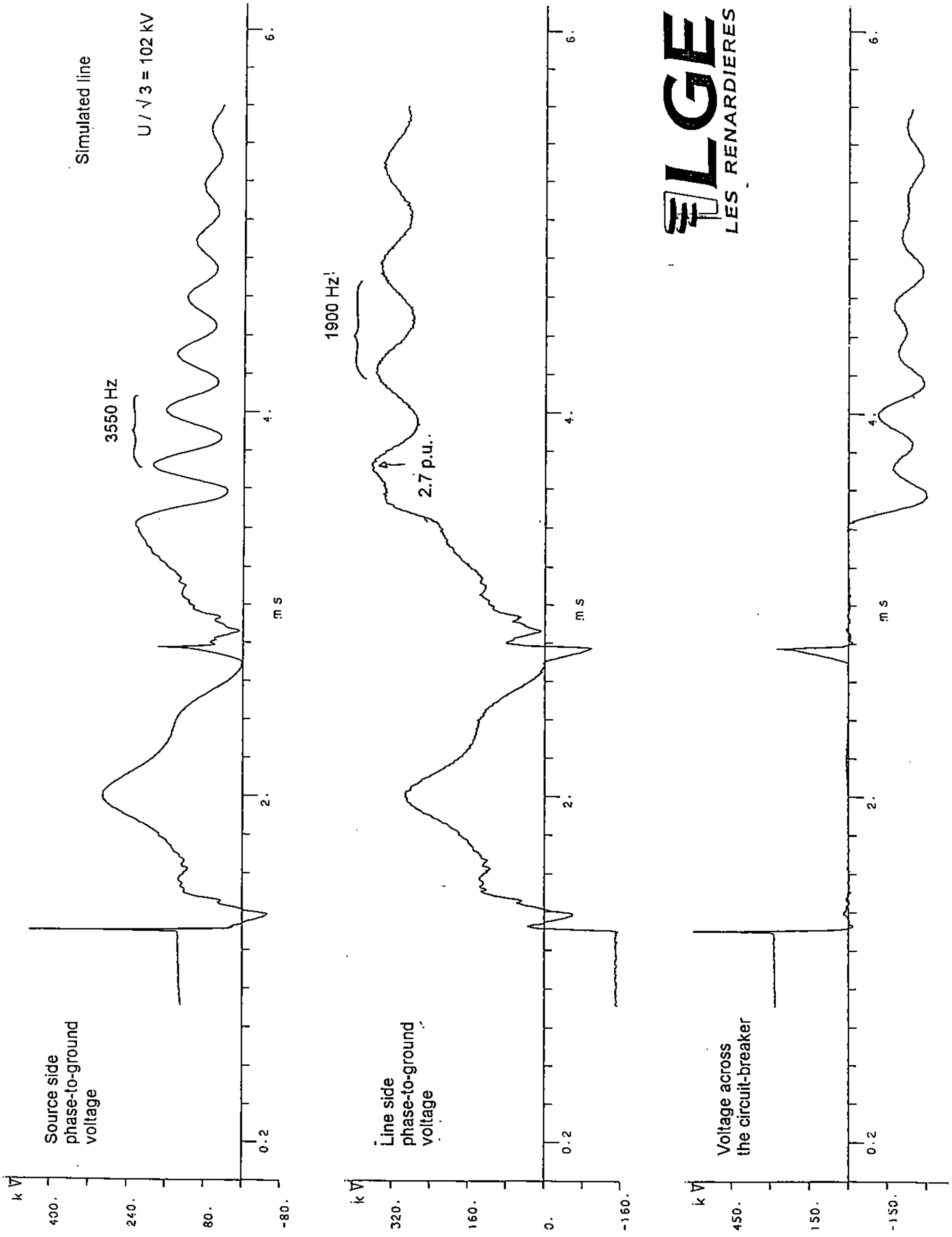


Figure 28: Test with a model of the line

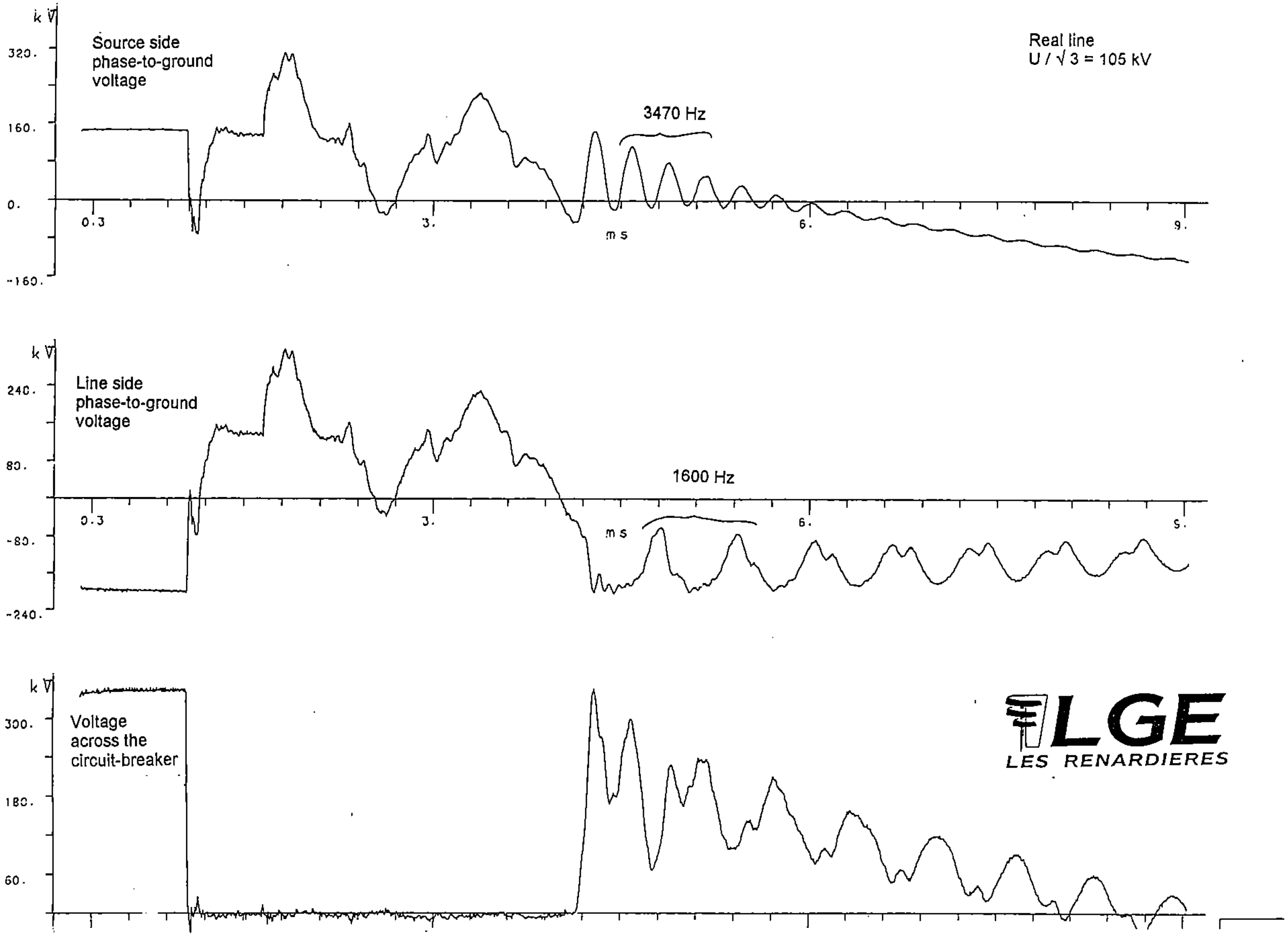


Figure 29: Test with real line

## 5. - LINE SWITCHING : TEST PROCEDURES

### 5.1. The existing IEC and ANSI procedures

Transmission lines can be of any length and are used over a wide voltage range.

The aim would be to perform a series of tests in such a way that the results would be applicable to almost all service requirements.

With this aim in mind bodies such as IEC and ANSI have developed test procedures, which manufacturers and test laboratories have followed, to allow type testing to be performed in a uniform manner.

The existing type test procedures in IEC 56 for instance involve a recognition of the influence on behaviour of several factors (source conditions, the line length, the line characteristics including earthing) and features of the circuit breaker such as **arc duration.**

The procedure for conducting line switching tests to IEC 56 can be summarised as four test duties, with the number of tests for each test duty stated to be :

- 10 tests for three-phase tests,
- 12 tests for single-phase tests with the contact separation distributed at intervals of approximately 30 electrical degrees.

It is worth examining the reasoning behind the choice of the number of tests for each test duty. A line switching operation is normally a planned operation where the energisation of the operating coils of the circuit breaker is not synchronised to the system, therefore, contacts can make or break at any point on the voltage wave. The operation would also normally involve all three poles and in practice there is likely to be small differences in closing times and opening times of the three poles. Therefore, any procedure must try and cover all the possible combinations of arc durations and phase closing and opening sequences.

When performing 10 three phase tests with random point-on-wave switching, the first phase to clear will be distributed between the three poles in a random way. Because a current zero occurs every 60 electrical degrees - 3.3 ms at 50 Hz - and assuming all three poles have their contacts parting at the same instant, the maximum arc duration ($t_a$) for the first phase to clear cannot exceed ($t_a$ min + 3.3) ms. **So when performing three phase tests, results are obtained for first phase to clear arc durations ranging from $t_a$ min to ($t_a$ min + 3.3) ms on all 10 tests per test duty.**

**When performing 12 single phase tests with controlled point-on-wave switching,** the voltage is chosen to represent first phase to clear conditions. The 30 electrical degree change between tests - equivalent to 1.65 ms - means that **four of the tests will have arc durations within the range ($t_a$ min + 3.3) ms to ($t_a$ min) ms.** The remaining eight tests will have longer arc durations, covering the performance of second and third phases to clear on the equivalent three phase test.

At this stage it is worth examining the ANSI C37.09.1979 procedure, because although it is very similar with regards to source voltage, load voltage and load current, it differs considerably when considering the number of tests. For three-phase tests and single phase tests it has only two duties but calls for 24 tests on each duty. The 24 tests are made up of two interruptions over the current loop at 0°, 30°, 60°, 90°, 120° and 150°, six interruptions with contact separation at the point-on-wave, ± 7.5°, which gave the shortest arc duration during the first 12 tests (on the first phase to clear for three phase tests); and six interruptions with contacts separation at the point-on-wave, ± 7.5°, which gave the longest arc duration during the first 12 tests (on the first phase to clear for three phase tests).

### 5.2. New tests procedures are necessary for modern circuit-breakers testing

Modern circuit-breakers, particularly high voltage circuit breakers, use $SF_6$ as the interrupting medium. This type of circuit breaker when used for transmission line switching has a very small minimum arc duration, even 0 ms in some cases. Therefore, test procedures which do not allow such short arc durations must be carefully assessed.

As stated earlier the IEC 56 tests result in 10 first phase to clear arc duration in the range ($t_a$ min) ms to ($t_a$ min + 3.3) ms for three phase tests per test duty, but only 4 arc durations in the same range for single phase tests per test duty. Also none of these are necessarily true minimum arc duration because of the coarse adjustments between tests. ANSI goes some way to improving this situation by calling for additional tests in the minimum arc duration region.

Since the **most vulnerable condition for the modern circuit breaker is when contacts part just before a current zero**, hence, applying the recovery voltage to the smallest gap, it is essential that the test procedure not only allows clearance with very short arc durations, but that the majority of the tests are performed in the minimum arc duration range.

The number of tests for a test duty should reflect the fact that the circuit breaker contacts can part at any point on the current wave, that there is a critical zone where the arc duration is very short, and should relate to the expected number of service operations. An attempt has been made to assess the number of switching operations for line breakers by approaching a number of utilities. The general consensus was that a realistic figure would be approximately 10 such operations per year, particularly if the circuit breaker has to clear the currents in the healthy phases with a fault on the third one. However if only one pole is tripped in case of single phase fault, this value could be 2-3 times lower.

The working group proposal is to apply the following procedure during the two tests duties using the same source circuit (as suggested in 4.1.2) :

- 12 tests regularly spread over a period, ie, 30° intervals (as in the existing test procedure),
- 18 tests at the minimum arcing time with a given polarity,
- 18 tests at the minimum arcing times with the other polarity.

The phrase "at the minimum arcing time" has to take into account the practical variation in opening time (although this might be small) which results in an arc duration within the minimum arcing time zone. Some additional tests in the maximum arcing time zone are thus also needed.

In the field application, the breaker is assumed to contact part randomly with respect to the voltage wave. If critical contact parting is defined as one which results in an arcing time no more than 0.5 ms greater than the minimum arcing time, there are six (two per phase) 0.5 ms critical time periods per cycle of 50 Hz or 60 Hz. Therefore, single phase testing with critical contact parting provides a test which is approximately 6.7 times (for 50 Hz) to 5.6 times (for 60 Hz) more effective in provoking restrikes than the three phase field application.

Knowing that, the probability of a series of n non-restriking operations occuring, each one of which has a probability $P_{restrike}$ of restriking, is $(1 - P_{restrike})^n$. If the probability of accepting a marginal design is made to be low, eg, 2% then $(1 - P_{restrike})^n = 2\%$.

Allowing n to be the proposed 72 tests (18 at each polarity in two test duties) then $P_{restrike} =$ 5.3% during the test, but is 6.7 times (for 50 Hz) to 5.6 times (for 60 Hz) less in the field application, or 0.8% (for 50 Hz) and 1% (for 60 Hz). **This statistical approach has allowed the working group to quantify the number of tests (at minimum arcing time) to cope with the realistic objective of having a 1% probability of restrike in service.**

### 5.3. Closing tests generate some ageing in the circuit-breaker

There are as many closing operations in the network as openings of unloaded lines. Most of these operations are not performed in sequence, as a CO for instance, except where a circuit-breaker has to clear a capacitive current on the healthy phases when there is a single phase fault on the line.

This explains why IEC 56 only requests 2 CO at the rated line-charging current for both source circuits, and also why "no appreciable charge shall remain on the capacitive circuits before the making operations" as an overhead line discharge is typically 10% in 3s even with dry conditions (except in case of capacitive voltage dividers). However, for reclosing during healthy phases switching, it is likely that there will be trapped charges on the line.

But these closing tests are not aimed at the evaluation of the overvoltages at closing because these overvoltages only depend on the network parameters and on the closing instant. They are normally not dangerous for the network and if necessary, in the case of UHV networks mainly, they can be computed or simulated, in order to design a device (see 3.1.4.) which will damp the overvoltages.

Closing operations may be significant for the two following reasons :

1. The effect of a closing operation on the subsequent opening operation (if done in sequence) : depending on the circuit-breaker technology, there may be a reduction of the dielectric properties of the circuit-breaker due for instance to a reduction of the SF6 pressure (SF6 puffer-breakers) or a reduction of the opening speed. This justifies some CO operations being required by the standard. They should be performed with openings around the minimum arcing time to be really meaningful.

2. Repeated breakdowns in the breaking unit(s) from closing operations may deteriorate insulating parts (nozzles for instance) and affect the dielectric withstand of the circuit-breaker. **The working group suggests to introduce at least separate closing tests that will generate some ageing of the circuit-breaker. This will contribute to increase the confidence in the equipment, which is actually stressed on the network at the same level as the one checked by type tests.** This is already the ANSI practice /15/, as 100% rated line switching current are close-open tests and with 30% of rated current, they are open-close tests for circuit-breakers rated for instantaneous reclosing.

## 6. - CONCLUSION

The main conclusions of this work focused on HV line switching are the following :

1. - Contrary to what is often said, most of the lengths of the UHV lines are covered by the rated line-charging current defined by the standard. But this is not the case for the lower voltages, for which the rated current should be increased.

2. - The opinion of the working group is that the circuit-breakers have been designed for years to be restrike-free. This is not a mandatory clause in IEC, but should be at least for voltages from 245 kV and above due to the potentially serious consequences of restrikes occurring on UHV lines.

3. - Very high stresses may exist on circuit-breakers in certain specific circumstances. This is for instance the case for long lines in non-interconnected networks. During testing it is possible to take into account the physical phenomena occuring during breaking (i.e. coupling with other phases, Ferranti effect, load rejection, presence of a single-phase fault) by an increase of the test voltage.

4. - Shunt compensation usually eases the breaking process because of the beating of the source power frequency with the line-side frequency.

5. - The two source circuits used for type testing according to IEC 56 are not so different as far as the initial jump is concerned. This could lead to a simplification of the standard, with one source circuit, as in ANSI, instead of the two.

6. - The smaller the initial jump, the more severe the stress on the circuit-breaker.

7. - Test circuits exist to test either restrike-free circuit-breakers or non restrike-free circuit-breakers in high power laboratories. In the first case, the circuit is simple and widely used. In the latter case, the topology of the circuit is more complex but achievable for single-phase tests and has been already used for years in one laboratory.

8. - The test procedure as it is now in IEC is not adequate to prove that a circuit-breaker is restrike-free. The working group suggests to double the total number of tests (48 for single-phase tests in four test duties for the time being), and to use them differently. Because it is of first importance to increase the number of tests with a very short arcing time ( nearly 0 ms ).

9. - It is also suggested to generate some ageing in the unit(s), which is what exists in service when switching lines. This can be done by introducing as many closing operations as breaking operations.

## 7. - REFERENCES

/1/ E.Slamecka, Prüfung von Hochspannungs-Leistungsschaltern. Springer-Verlag 1966.

/2/ J.Zaborszky,J.W.Rittenhouse, Electric Power Transmission, Rensselaer Bookstore, Troy N.Y. 1969

/3/ CIGRE WG 13.04, Capacitive current switching - State of the art, Electra No. 155 Aug. 1994

/4/ L.V.Bewley, Traveling waves on transmission systems, John Wiley & Sons, Inc. 1951.

/5/ C.Portela, Analysis of main aspects that influence recovery voltage in no load line switching off. COPPE/UFRJ - c89-RT-ID001

/6/ EPRI, Transmission line reference book - 345 kV and above. 1987.

/7/ C.H.Flurscheim, Power Circuit Breaker - theory and design, IEE Monograph Series 17

/8/ E.Ruoss, Overvoltages when energizing HV lines. Brown Boveri Review, 4-79, vol.66 pp.262-279, April 1979.

/9/ W.Diesendorf, Insulation coordination in high voltage Electric Power Systems. Butterworth & Co (Publishers) Ltd, London, 1974.

/10/ R.Eriksson,V.S.Raskes, Three Phase Interruption of Single and Two-phase Faults: Breaking Stresses in the Healthy Phases. Electra ,No. 67, pp. 77-92, 1979.

/11/ A. Greenwood, Electrical Transients in Power Systems, Wiley - a Wiley-Interscience publication , New York, 1971.

/12/ L.P.S.Silva,M.Drummond,M.Lacorte, Capacitive current switching - no-load lines. II Latin-American Regional Meeting of CIGRE, Puerto Iguaçu, Argentina, June 1987.

/13/ G.Saint-Jean, Y.Latour, M.Landry, J.Bélanger, H.Huynh, P.Czech, Solution to the problem of separation of the Hydro-Quebec 735kV system by switchable metal-oxide surge arresters. CIGRE Session, Paper 33-01, Paris, 1986.

/14/ IEC 56, High-voltage alternating-current circuit-breakers - Fourth edition 1987.

/15/ ANSI/IEEE C37.012-1979, Application Guide for Capacitance Current Switching for AC High-Voltage Circuit Breakers Rated on a symmetrical Current Basis

/16/ IEC 427, Synthetic testing of high-voltage alternating-current circuit-breakers - Second edition, 1989.

/17/ H. Nasko , Beitrag zur Untersuchung der Vorgänge beim Abschalten leerlaufender homogener Leitungen in Hochspannungsnetzen , ETZ-A83, 1962 ,pp. 39-45.

/18/ R. Planche, Artificial unloaded lines for testing high voltage circuit-breakers, IEEE Vol PAS-103, n° 9, September 1984.

/19/ CIGRE WG 13-04, Requirements for capacitive current switching tests employing synthetic test circuits for circuit-breakers without shunt resistors - Electra n° 87, 1983, pp. 25-39.

/20/ CIGRE TF 13-00-1 ,Controlled switching - A state-of-the-art survey ,Electra Nos. 162 Oct 1995 and 163 Dec 1995.