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ON VOLTAGE AND POWER STABILITY IN AC/DC SYSTEMS

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Working Group 14.05

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To the memory of Clarence V. Thio

Contents

[1]This section is identical with section 1.2, but since it is essential for the subsequent discussion in this chapter it is repeated in full here.

Preface

This report is the result of work done in Cigre WG14.05 over the years 1996 - 1999. By various reasons all the various contributions have not been put together in a single document until now. When this work started, it was not clear to the convenor, nor to the working group members, the amount of work required to cover the topic in a systematic way. To do this substantial additional work would be needed. Still, the report contains significant new results, e.g. concerning the definitions of voltage and power stability an AC/DC systems, section 1.5. This definition is adopted to comply with the definitions introduced in power systems without any HVDC systems. But also other chapters contain new material.

As agreed at the SC14 meeting in Paris 2000, the material available has been put together without any excessive editing. Therefore, it might occur repetitions and the coherency might not be complete. Despite this, the report contains a lot of material that is deemed to be useful for the power industry.

Since the work started in 1996 new types of converters have been introduced for high power application, i.e voltage source converters, which not are discussed or analyzed in this report. Only line commutated current source converters and capacitor commutated converters are covered. However, the analysis methods and tools in the report could also be applied to systems using voltage source converters or other types of converters.

The main contributors of the chapters in this report are:

Chapter 1: G. Andersson

Chapter 2: H.A.D. Lee

Chapter 3: A. Golé

Chapter 4: J. Reeve

Chapter 5: H.A.D. Lee

Chapter 6: C.V. Thio and J.B. Davies

During the course of this work the working group suffered a significant loss when Clarence Thio passed away. Clarence was one of the most active members of the working group and his contributions were essential for the progress of the work documented in this report. His insights and experience together with his sincere interest to understand the problems dealt with inspired all members of the working group and had a decisive influence of the work pursued here. We will all remember Clarence as a prominent engineer and a great friend.

The members of WG14.05 who participated in the work were:

T. Adhikari

G. Andersson (Convenor)

J.B. Davies

M.A. Eitzmann

A. Golé

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As convenor I want to thank all the members of the working group for their work and contributions, which formed the basis for this report.

Göran Andersson
Convenor WG14.05

Summary

Voltage and power instability has been a limiting factor for many HVDC projects during the last decades. Pioneering and systematic work to understand and analyse the interactions leading to this instability started in the early eighties, and joint Cigré and IEEE working group presented the first comprehensive overview of the topic in the early nineties, ref. [4] of this report. After that report was published substantial work has been done, both in the academia and the industry, to further develop analytical and simulation tools in order to improve the understanding and the computational tools. These later developments are reported in this report. A brief overview of the report is given below.

In the late eighties and early nineties extensive work was done within Cigré and IEEE to better understand and analyse voltage stability in (pure) AC systems. Among other things definitions regarding voltage stability were formulated. These definitions are reviewed in chapter 1 and definitions applicable for AC/DC systems that are consistent with those of AC systems are formulated.

The concepts of Maximum Power Curves (MPCs) and Voltage Sensitivity Factors (VSFs) were early introduced for the analysis of simple AC/DC systems. In chapter 2 the theoretical foundations of these tools are further developed and extensions to more complex systems are carried through. Systems with loads, parallel AC lines, and multi-infeed HVDC systems are included. In chapter 5 further considerations for multi-infeed systems are discussed.

The methods dealt with in chapter 2 are based on quasi steady-state considerations. The virtue is that very powerful computational tools can be developed, which enable very fast analysis of different system conditions as well as analysis of the influence of different design and system parameters. However, the dynamics of the system is not explicitly modelled and the analysis based on quasi steady-state methods must be extended with time simulations for a complete analysis of system. In chapter 3 comparisons between the static analytical methods and full detailed time simulations are given. The conclusion is that static methods, i.e. the ones based on MPC and VSF, can be used for determining the limits of voltage/power stability, but for determining the dynamic properties a full dynamic model of the system is required.

In chapter 4 the influence of loads, parallel AC lines, etc, on the stability limits is studied. It is also demonstrated that the stability limits of the Capacitor Commutated Converters (CCCs) are significantly higher as compared with those of the standard line commutated converters. (VSC converters were not included in this analysis, see below.)

In chapter 6 a discussion how the developed tools can be applied to real planning and design problems is given. Particularly, the interplay between the use of the static and dynamic analysis tools are exemplified. The Nelson River HVDC scheme is the system mostly considered in this chapter.

The analysis methods described in this report can be used for all converter types. However, in this report the methods have only been applied to the conventional line commutated converters, and Capacitor Commutated Converters (CCCs), but not to systems with Voltage Source Converters (VSCs). The extension to this latter kind of HVDC systems should be straightforward.

1
Basic Theory and Definitions

1.1 Introduction

Modern power systems are becoming increasingly complex and large. To be able to predict the behaviour of these systems under different operating conditions engineers are more and more dependent on sophisticated software. Since the models of the power system and the software used in analyses are getting more and more complex the requirements on the engineers involved in these studies get higher. Even if the analytical tools are much more powerful today, it is still of utmost importance that the engineers have a thorough understanding of the basic physical processes and interactions in the system. Without this knowledge it is not possible to understand phenomena in complex systems, and to design appropriate control and protection systems that can alleviate possible adverse interactions.

Another important prerequisite for the establishment of a good understanding of a phenomenon is that commonly accepted and appropriate definitions exist. This will facilitate the discussion between experts and contribute to the development of the knowledge and understanding. It is not uncommon that disagreements between experts on an issue are due to lack of accepted definitions. The importance of clear definitions, that are commonly accepted, should be obvious.

In this chapter a basic explanation of the power and voltage instability phenomena is given. This is done by introducing a simple model of an AC/DC system, which exhibits the basic interactions that are dominating also in real size power systems. Definitions of power and voltage stability are also given. These definitions are based on definitions of voltage stability for AC systems.

The chapter is organised as follows. First a brief physical explanation of the power and voltage instability in AC/DC systems is given. Then the definitions of voltage stability in AC systems are reviewed and discussed. A simple AC/DC system model is then introduced and definitions of voltage and power stability in AC/DC systems are proposed.

1.2 Simplified Explanation of Power/Voltage Instability Phenomenon

A power/voltage instability in a conventional line-commutated HVDC system can basically arise out of an inter-relationship between the AC voltage, DC controls and the DC current. It manifests itself in "weak" AC systems because it depends almost entirely on the "stiffness" of the AC voltage. In simple terms, the basic mechanism of the instability occurs as follows.

Suppose the AC voltage drops just a small amount; then the DC voltage at the inverter drops proportionately (they are directly related). But the main

function of the DC controls in many DC schemes is to hold constant power order ($P_d = U_d \cdot I_d$). If the DC voltage (U_d) goes down, the only way the controls can maintain constant power is to increase the DC current (I_d). However, as soon as it does this, the reactive power consumption of the DC increases because this is directly related to the DC current. Unless this additional reactive power is immediately available, the AC voltage will dip further and start the cycle all over again. In other words, an unstable cycle will be started and perpetuated, which unless it is stopped in some way can lead to a runaway condition and a total collapse of the entire AC/DC

1.3 Definitions of Voltage Stability in AC Power Systems

During the late eighties substantial work was done within the power industry to develop methods and tools to analyse and predict voltage stability in power systems. A number of working groups within CIGRE and IEEE produced a large number of documents on the topic, and some of the work done is summarised in refs. [1] and [2]. These references contain the definitions that are generally accepted in the industry today. It is of interest to note that the definitions in these two reports are not identical. These definitions are reviewed below.

1.3.1 Definitions According to CIGRE

In ref. [1] the following definitions are given:

- A power system at a given operating point is *small-disturbance voltage stable* if, following any small disturbance, voltages near loads are identical or close to the pre-disturbance values.
- A power system at a given operating state and subject to a given disturbance is *voltage stable* if voltages near loads approach post-disturbance equilibrium values. The disturbed state is within the region of attraction of the stable post-disturbance equilibrium.
- A power system undergoes voltage collapse if the post-disturbance equilibrium voltages are below acceptable limits.

As seen these definitions are quite general and refer to how power system voltages react to disturbances in the system.

1.3.2 Definitions According to IEEE

Another set of definitions is given in ref. [2]:

- *Voltage stability* is the ability of a system to maintain voltage so that when load admittance is increased, load power will increase, and so that both power and voltage are controllable.
- *Voltage collapse* is the process by which voltage instability leads to a loss of voltage in a significant part of the system.

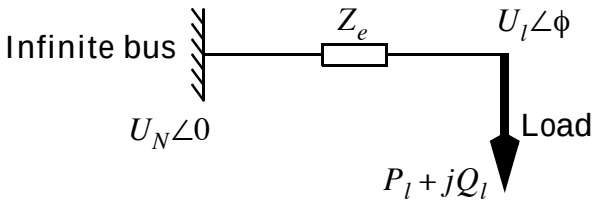

Figure 1.1. Simple AC power system for analysis of voltage stability.

- *Voltage security* is the ability of a system, not only to operate stably, but also to remain stable (as far as the maintenance of system voltage is concerned) following any reasonable credible contingency or adverse system change.

- A system enters *voltage instability* when a disturbance, increase in load, or system change causes voltage to drop quickly or drift downward, and operators and automatic system controls fail to halt the decay. The voltage decay may take just a few seconds or ten to twenty minutes. If the decay continues unabated, steady state angular instability or *voltage collapse* will occur.

This set of definitions are obviously more restrictive than those of the previous subsection. This will be illustrated in subsection 1.3.4.

1.3.3 Other Definitions

In the literature there exist many more definitions, most of them just variations of the ones given above. It will not be elaborated on those here, but it might be worthwhile to mention another concept that has been used, i.e. the concept of regularity. In ref. [3] regularity is defined as:

- A power system is said to be *voltage regular* at a given operating point if an injection of reactive power into a bus does not result in a decrease of voltage magnitudes in the system.

The rationale for this definition is obvious since voltage control is mostly accomplished by controlling reactive power from controllable sources, such as synchronous machines, reactive shunt elements, SVCs, etc. The authors of ref. [3] suggest that in addition to the requirements given in the above definition, the system needs also to be voltage regular in order to be voltage stable.

1.3.4 Discussion of CIGRE and IEEE Definitions

The Nose Curve of a Simple Test System

A simple system often used in voltage stability studies is the one Figure 1.1. It is assumed that the system quantities could be adequately modelled by phasors for the analysis done here.

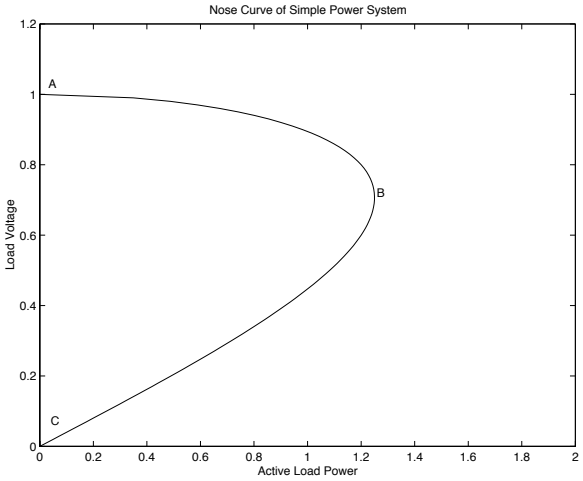

Figure 1.2. Nose curve of simple AC power system. Power factor of load =1. Impedance of line = 0.4 p.u., impedance angle = 90°. Voltage of infinite bus = 1.0 p.u.

If the voltage of the infinite bus is kept constant, both magnitude and phase, and the active load demand P_l is varied, the so-called nose curve is obtained. This curve shows how the load voltage U_l varies as P_l is changed. It is assumed that for a given active load there corresponds a unique reactive load, for instance by assuming a constant power factor. A typical example of a nose curve is shown in Figure 1.2.

The curve in Figure 1.2 shows that for each load power level below the power corresponding to the point B, there exist two solutions: One with "high" voltage and one with "low" voltage. At the point B these two solutions coalesce, and above this power level no solutions exist with the given data of the system. The point corresponding to B is often referred to as the *Point of Maximum Loadability* (PML).

Physically the curve in Figure 1.2 can be constructed in the following way. At the load bus a shunt admittance (impedance) is connected, and the value of this admittance is increased from zero, corresponding to point A, to infinity, corresponding to point C. The ratio between the active and reactive parts of the admittance should be kept constant to a value determined by the power factor of the load. For any given value of the load admittance, the load voltage can be calculated and the load power determined, which means that to any given value of the admittance there exists a unique point on the nose curve.

Definitions Applied to Simple Test System

The definitions given above will now be applied to the system in Figure 1.1. It is clear that with the definition of IEEE, subsection 1.3.2, operation on the nose curve between points B and C will be unstable by definition, since in this region load power will decrease when load admittance is increased as explained above. Thus only operation on the upper part of the nose curve can be stable according to the definition of IEEE.

k_p	U_{stab}
≥ 1	0
0.75	0.45
0.5	0.58
0	0.71 ("B")

Table 1.1. Regions of voltage regularity for different active load voltage dependencies, k_p Operating points on the nose curve of Figure 1.2 with voltages greater than U_{stab} are voltage regular, i.e. $VSF > 0$, those with voltages less than U_{stab} are not voltage regular. The transition point for constant power loads, i.e. loads with $k_p = 0$ corresponds to the point B in Figure 1.2.

If the definitions according to Cigré, subsection 1.3.1, are to be applied, a few considerations have to be made. The voltage control of all power systems is based on the assumption that injection of reactive power increases the voltage magnitude at the injection bus and the adjacent buses. Injection of reactive power could be done by connection of shunt capacitors, disconnection of shunt reactors, raising the excitation of synchronous machines, etc. This principle could be expressed as that the quantity called the *Voltage Sensitivity Factor* (VSF) is positive, or mathematically

$$VSF = \frac{\Delta U}{\Delta Q} > 0 \tag{1.1}$$

As seen this means that the system is voltage regular according to the definition of ref. [3], and a necessary condition for stability is thus voltage regularity. It is straightforward to calculate the *VSF* for the simple system above. To simplify the calculations it is assumed that the load is purely active and it has voltage dependence according to

$$P = P_0 \Big(\frac{U}{U_0} \Big)^{k_p} \tag{1.2}$$

With these assumptions it can be shown that regions of the nose curve where *VSF* is positive depends on the exponent k_p. It turns out that the nose curve is divided into two regions, one where *VSF* is positive and one where *VSF* is negative. At the transition point *VSF* goes to infinity. If it is assumed that the line impedance Z_e is lossless and that the voltage of the infinite bus is kept at 1 p.u., the stability regions for some exponents k_p are given in Table 1.1 can be summarized as:

For constant power loads, i.e. $k_p = 0$, only operating points on the upper part of the nose curve are voltage regular and the transition takes place at the point B of the nose curve. If the voltage dependence is as constant current load or with a higher exponent, i.e. $k_p \geq 1$, all points on the nose curve are voltage regular. For values of k_p in between, the border between voltage regularity and irregularity lies on the lower part of the nose curve as indicated in Table 1.1. Negative values of k_p are deemed unphysical and not considered.

It should be noted that in principle a voltage control strategy based on that reactive power injection decreases the voltage could be used in the regions found voltage irregular above. However, such a voltage control scheme had to detect

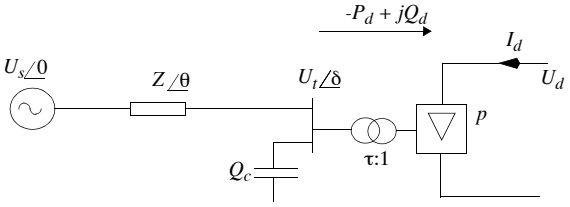

Figure 1.3. Simple AC/DC system for analysis of voltage/power stability. The quantity p in the figure includes all parameters that are needed to specify the HVDC system, e.g. commutation reactance, commutation margin, etc.

the sign of *VSF* before acting, and such a controller is deemed to be highly hypothetical and not to be considered in a practical power system.

Furthermore, one could here imagine that the load characteristics are such that the initial voltage dependence ensures stability, but slower control actions are such that the operating point moves away from the initial one, leading to either too high voltages in the system or to a voltage collapse. Therefore, operation on the lower part of the nose curve might be tolerable for short period of times, but to guarantee stability, normal (steady state) operation must be on the upper part of the nose curve.

Conclusions

Two main conclusions can be drawn from the simple example analysed above:

- According to the IEEE definition, operation on the lower part of the nose curve is unstable.
- According to the definition of Cigré the stability depends on the voltage characteristics of the load and for certain disturbances operation might be stable on the lower part of the nose curve. However, for secure stable operation the system must be on the upper part of the nose curve.

These two conclusions will be very important when we discuss stability for AC/DC systems in the next section.

1.4 Analysis of AC/DC Systems

For analysis of the voltage/power stability[1] of an AC/DC system a test system similar to the one in Figure 1.1 has been introduced, see e.g. ref. [4]. This system is depicted in Figure 1.3.

The system in Figure 1.3 is believed to be a good model of a real AC/DC system in the time frame where the DC current controls of the HVDC link have had time to respond, but the controls of the AC system have not yet responded. It is thus assumed that no "fast" voltage controls such as SVCs are present in the AC system, but the voltage control is basically carried out by the AVRs of

[1] A definition will be proposed in the next section.

the synchronous machines. It is further assumed that loads could be modelled by impedances. These assumptions are discussed more in detail in ref. [4], where a description on how to model synchronous machines also is included. In the subsequent chapters the influences of these assumptions are further analyzed and discussed. From Figure 1.3 a few basic definitions are recalled:

- *Short Circuit Ratio*, *SCR*, is the per unit admittance of the impedance $Z\angle\theta$ in Figure 1.3. The per unit value is based on the nominal MW rating of the HVDC converters and the nominal AC voltage of the converter AC bus.

- *Effective Short Circuit Ratio*, *ESCR*, is $SCR + Y_c$, where Y_c is the per unit value of the admittance of the shunt reactive power compensation Q_c in Figure 1.3.

From the definitions of SCR and $ESCR$ it is clear the these quantities are complex numbers. However, in most cases the angle θ is close to 90°. Furthermore, as shown in ref. [4], system performance is rather insensitive to the angle θ as long as its value is close to 90°. Therefore, if not explicitly stated, it is assumed that $\theta = 90°$, and only the magnitude of SCR is given. In this case $ESCR$ can be written as $ESCR = SCR - Q_c$.

The discussion in the following will be based on the model system of Figure 1.3, and the assumptions briefly reviewed above are adopted.

1.4.1 Maximum Power Curves

A very central concept in analysis of the behaviour of AC/DC systems in the time scale indicated above is the *Maximum Power Curve* (MPC). This curve shows many similarities with the nose curve of the simple AC system of Figure 1.1, and in fact the MPC can be converted into a nose curve with the load being an HVDC converter, as will be shown later. A fairly detailed description of how an MPC for an HVDC inverter is derived will be given below.

Firstly, define a pre-disturbance steady state operation point of the system. This could in principle be any operating point within the rating of the equipment and operating limits of the system, but for simplicity it is assumed that the pre-disturbance operating point corresponds to nominal conditions, i.e. U_t = 1.0 p.u., I_d = 1.0 p.u., P_d = 1.0 p.u. Other conditions of the HVDC, e.g. γ (commutation margin) and U_d, are also at nominal values, and the reactive compensation Q_c is also at a given (nominal) value. By solving the load flow and HVDC equations, this would uniquely determine the values of the transformer tap ration, τ, magnitude of the source voltage, U_s, and the phase angle of the converter bus voltage, δ[2]. All these values determine then the initial steady state operating point of the system.

The MPC of an inverter in constant commutation margin, γ, operation[3] is now derived as follows. The values of U_s, τ, Q_c, and γ are kept constant,

[2]We have here set the phase angle of the source voltage to zero, which means that this voltage phasor is the phase angle reference of the system.

[3]One could in principle allow other modes of operation as well. The only requirement being that when the DC current is varied that the controls uniquely determine the states of the system so that the load flow equations could be solved. Other control modes that are conceivable are constant firing angle control, constant DC voltage control, etc. see section 1.6

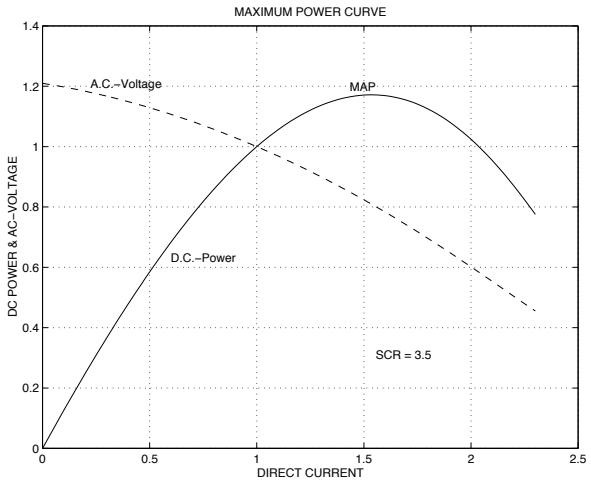

Figure 1.4. Maximum Power Curve (MPC) of the system in Figure 1.3. $SCR = 3.5$, $\gamma = 17°$. Initial operating point: $I_d = 1$ p.u. and $U_t = 1$ p.u.

"frozen", while the DC current, I_d, is varied. The variation of I_d is assumed to be so "slow" that the new state of the system could be determined by solving the resulting load flow equations of the system in Figure 1.3. The active and reactive power of the DC system are determined by the steady state equations of the converter. By varying I_d the magnitude of AC voltage of the converter bus, U_t, the phase angle of this voltage, δ, the active and reactive power of the HVDC system, P_d and Q_d, will vary. A typical example of how the DC power and terminal voltage will vary with the variations of the DC current with the assumptions above is given in Figure 1.4.

The solid curve in Figure 1.4, i.e. the MPC, has similarities with the nose curve of Figure 1.2. The *Maximum Available Power* (MAP) is defined as the maximum point of MPC, and this points indicates thus the theoretically maximum DC power that can be injected into the system by keeping all "controllable" quantities in Figure 1.3 constant, varying the DC current only. The corresponding DC current is called I_{MAP}. (The variables U_t and δ will of course vary as a consequence of the variation of I_d, but these are not controllable as e.g. U_s and τ.) MAP corresponds thus to PML of the nose curve in the AC system case. In a real system, MAP may not be feasible since the corresponding DC current might be too large, or the corresponding low AC voltage might cause e.g. protections to act.

The shape of the MPC depends very much of the SCR, i.e. of Z, of Figure 1.3. If the SCR now is lowered to 1.5 an MPC according to Figure 1.5 is obtained. An interesting finding in Figure 1.5 is that the MAP is to the left of the initial operating point. Consequently, an increase in DC current at the nominal operating point implies a decrease in the DC power, and vice versa. This is contrary to the objective of DC power control, and therefore this operating situation should be avoided if normal power scheduling should prevail. Otherwise, an increase of DC current order, as an attempt to increase DC power will be unsuccessful.

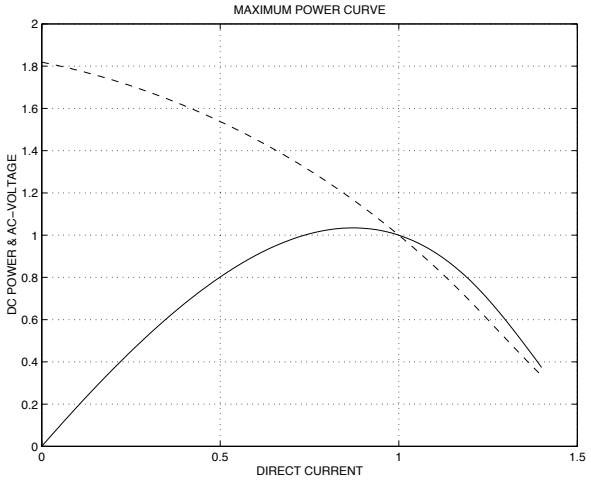

Figure 1.5. Maximum Power Curve (MPC) of the system in Figure 1.3. $SCR = 1.5$, $\gamma = 17°$. Initial operating point: $I_d = 1$ p.u. and $U_t = 1$ p.u.

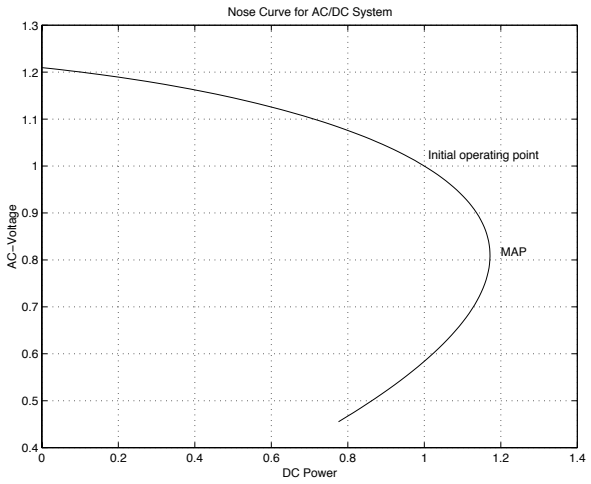

Figure 1.6. Nose curve for the AC/DC system in Figure 1.3, $SCR = 3.5$.

As indicated above the nose curves of the pure AC system and the MPCs exhibit great similarities. To verify this, curves showing the variation of AC voltage as function of the DC power are plotted in Figure 1.6 and Figure 1.7 for the MPCs in Figure 1.4 and Figure 1.5, respectively.

1.4.2 Voltage Sensitivity Factors

The VSF could also be calculated in the nominal operating points of Figure 1.4 and Figure 1.5. When doing this the MPC *per se* can only give limited information. The MPC depicts the behaviour when only the DC current is varied,

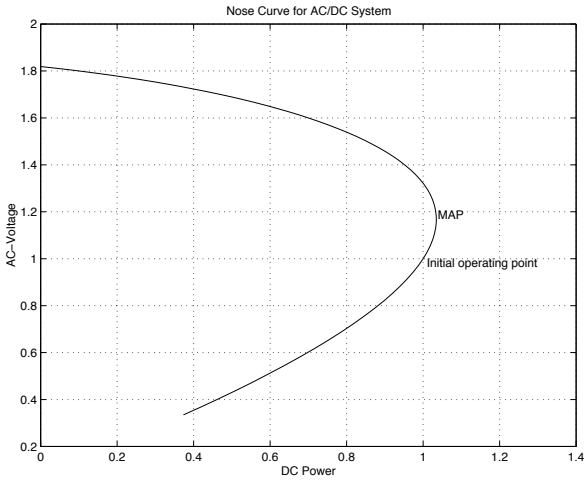

Figure 1.7. Nose curve for the AC/DC system in Figure 1.3, $SCR = 1.5$.

SCR	Control Mode	VSF
3.5	C.C.	+
3.5	C.P.	+
1.5	C.C.	+
1.5	C.P.	-

Table 1.2. Sign of Voltage Sensitivity Factors of the systems in Figure 1.4 and Figure 1.5 at the nominal operating point. C.C. = Constant DC Current Control. C.P. = Constant DC Power Control.

but when calculating the VSF other quantities than the DC current could be varied. When calculating VSF, the control mode of the HVDC is crucial to the result. For the systems of Figures 1.4 and 1.5 the control modes constant power control and constant DC current control will be considered. Other control modes can also be analysed, but for the discussion here it is sufficient to consider these two modes. A simple analysis gives the results of Table 1.2.

As seen from Table 1.2 all cases are voltage regular except the last one, which corresponds to constant DC power control in the weak AC system case. It is thus seen that for the weak system ($SCR = 1.5$), constant power control implies a negative VSF, while constant DC current control implies positive VSF.

1.5 Definitions for AC/DC Systems

When comparing the analyses of the nose curve and the MPC one can conclude that DC current plays the same role for the AC/DC system, Figure1.3, as load admittance does in the pure AC system, Figure1.1, see subsection 1.3.2. The roles of load characteristics in the AC case and control mode of the HVDC in the DC case are also similar. Therefore it is motivated that the definitions of voltage stability given in section 1.3 be modified accordingly to cover AC/DC

systems. From the discussion above the following two definitions are proposed for an AC/DC system:

Definition of Power Stability:

Power Stability of an AC/DC system is the ability, for a given operating condition and DC control mode, to increase DC power by an incremental increase in DC current.

Definition of Small-Disturbance Voltage Stability:

An AC/DC system at a given operating state and DC control mode, and subject to a small disturbance, is said to be *small-disturbance voltage stable* if AC voltage settles to equilibrium close to pre-disturbance value.

Definition of Voltage Stability:

An AC/DC system at a given operating state and DC control mode, and subject to a given disturbance, is said to be *voltage stable* for this particular DC control mode and disturbance, if AC voltage and other system states settle to values that are viable for system operation.

1.6 Discussion

It is clear that operation to the left of MAP is stable according to the definitions above.

From the proposed definitions it is obvious that operation to the right of the MAP will not be power stable. When it comes to voltage stability it is clear that in constant DC power control operation to the right of MAP is unstable[4]. A control action to increase the voltage magnitude, e.g. by connecting a shunt capacitor, will result in a decrease in voltage, see Table 1.2. (It is here assumed that the constant power control loop can control the DC power to the desired value.) This will in a real system lead to an unstable situation.

In constant DC current control and to the right of MAP, the system is initially voltage stable since the VSF is positive. However, the system will not transmit the desired amount of power and any attempt to adjust the DC current with a standard DC power controller will lead to unstable conditions. Therefore, the system can operate transiently to the right of MAP, but in order to use the HVDC link for power control it must be brought back to the left side of the MAP.

The definition of voltage stability involves arbitrary disturbances, such as earth faults and trippings of lines. For such cases analyses based on MPCs are not sufficient, since the large signal dynamics of the system plays an important role. The restart strategies of the HVDC after faults are very important when analysing (large disturbance) stability of the interconnected AC/DC system.

In the examples above it has been assumed that the inverter is in constant γ control. However, as indicated above MPCs can be computed for other types of HVDC controls such as constant DC voltage control or other types of γ

[4]It is here assumed that the DC power controller has a positive gain in its main loop, i.e. a decrease in DC power will result in an increase in the DC current order.

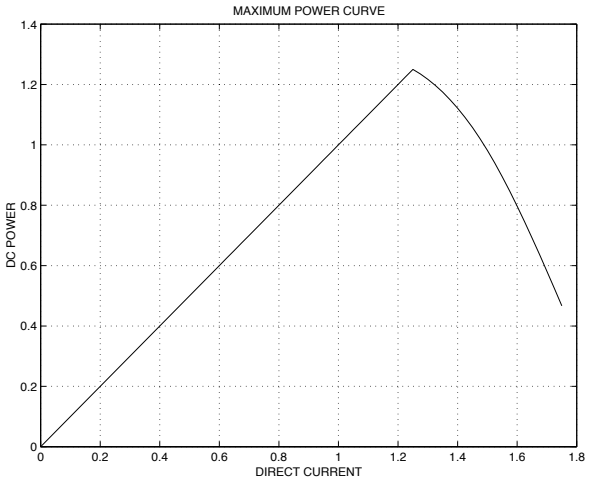

Figure 1.8. MPC for an AC/DC system with constant DC voltage control.

control. The MPC for such a control mode will look different, but there will be a MAP point for such modes also. The MAP will occur for the point where γ has reached its minimum permissible value, γ_{min}. The MPC to the right of this point would coincide with an MPC with constant $\gamma = \gamma_{min}$. The same reasoning for these types of control as for the constant γ control applies, which means that only steady state operation to the left of MAP is stable in a practical system. An example of an MPC with constant DC voltage control is given in Figure 1.8.

To distinguish between MPCs plotted for different control modes, an index indicating which DC controls that are used when calculating can be used. The standard MPC with constant γ control should thus be denoted MPC_γ and the MPC in Figure 1.8 should be MPC_{U_d}.

2
Analytical Tools and Methods

2.1 Introduction

The basic concepts of power/voltage instability associated with weak AC/DC interconnections have been discussed in the previous chapter. A number of analytical tools based on these concepts, in the form of system indices, have been proposed to facilitate qualitative appraisal of power/voltage stability [4], [5],[6],[7],[8]. These are the *Maximum Available Power* (MAP), *Voltage Sensitivity Factor* (VSF), and *Control Sensitivity Index* (CSI). Essentially these indices are all sensitivities of system states to incremental changes in controlling system quantities. In this chapter, the basic formulation and application of these analytical tools are treated.

These indices have invariably been derived based on a simplified AC/DC system configuration as shown in Figure 2.1, commonly known as a single-infeed configuration. However, recently emerging AC/DC system configurations around the world have necessiated other appropriate simplified system models that would adequately represent these new situations. In particular are system configurations with multiple HVDC links terminating in close proximity and point-to-point HVDC links having parallel AC lines, commonly referred to as multi-infeed and single-infeed with parallel AC line configuration, respectively. In this chapter, the analytical tools developed with respect to the classical single-infeed configuration would be extended to these higher-order system models as shown in Figure 2.8 and Figure 2.9. Further, the simplified system model of Figure 2.1 would also be enhanced by incorporation of local system components such as loads, compensators, etc., and the basic equations derived. With the analytical methods applied to the various system models, there exists a relationship among them. This chapter also establishes this overall relationship among the power and voltage stability methods for the various system models.

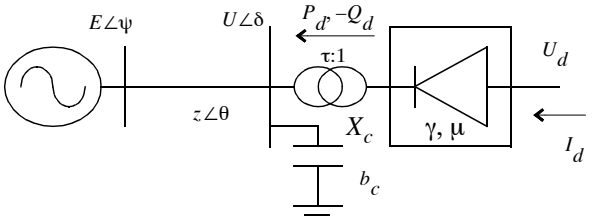

Figure 2.1. Simplified single-infeed HVDC configuration.

2.2 Power Stability

2.2.1 Maximum Available Power

The concept of *Maximum Available Power* (MAP) was first introduced in [5] and [6] to the system model of Figure 2.1 with the converter operating in *Constant Extinction Angle* (CEA) control mode. This maximum available power is defined as the maximum of the *Maximum Power Curve* (MPC) which is the converter DC power P_d as a function of the direct current I_d. Mathematically, this operating point corresponds to the condition that

$$\frac{dP_d}{dI_d} = 0 \tag{2.1}$$

Equation (2.1) is known as the MAP condition. When this condition occurs, the prevailing DC power is the maximum the converter can deliver to the AC system at the corresponding direct current I_{MAP}. Beyond I_{MAP}, the DC power delivered actually decreases with further increase in direct current. This is due to the larger percentage decrease in the converter AC bus voltage as compared with the increase in direct current, resulting in a net decrease in the DC power. Such a phenomenon corresponds with unstable system behaviour, thus the MAP condition determines the power stability limit of the AC/DC interconnection. The index dP_d/dI_d is the gradient of the MPC and can be derived from the power flow equations for the converter AC and DC buses in Figure 2.1. By linearizing these equations with respect to the system states I_d, U, δ, and eliminating U, δ, dP_d/dI_d may be derived as

$$\frac{dP_d}{dI_d} = \frac{rU\cos(\gamma+\mu)\big[U^4 ESCR^2 + b\big(U^2 ESCR + Q_d\big) - Q_d^2 - P_d^2\big]}{\det J_I} \tag{2.2}$$

where

$$ESCR = \frac{1}{z} - b_c$$

$$r = \frac{2U_d}{\cos\gamma + \cos(\gamma+\mu)} \qquad b = 2\big[Q_d - P_d\tan(\gamma+\mu)\big]$$

$$\det J_I = U^4 ESCR^2 - Q_d^2 + U\frac{\partial Q_d}{\partial U}\bigg|_{I_d}\big(U^2 ESCR + Q_d\big) - P_d\bigg(P_d - U\frac{\partial P_d}{\partial U}\bigg|_{I_d}\bigg)$$

and $\partial P_d/\partial U_I|_{I_d}$ and $\partial Q_d/\partial U|_{I_d}$ are the voltage dependence of the converter active and reactive power, respectively, for the constant current control mode (see eq. (2.9)). From eq. (2.2), the MAP condition thus occurs when

$$U^4 ESCR^2 + b\big(U^2 ESCR + Q_d\big) - Q_d^2 - P_d^2 = 0 \tag{2.3}$$

If the system operating point corresponds with the MAP condition under nominal conditions, then the prevailing $ESCR$ is said to be critical, $CESCR$. Eq. (2.3) then solves to

$$CESCR = \frac{1}{U^2}\bigg[-\frac{b}{2} + \sqrt{\big(\frac{b}{2} - Q_d\big)^2 + P_d^2}\ \bigg] \tag{2.4}$$

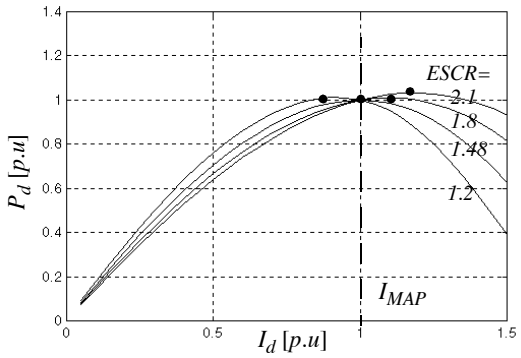

Figure 2.2. Maximum Power Curves.

This reduces further to

$$CESCR = \frac{1}{U^2}\Big[- Q_d + P_d \cot\big(\frac{\pi}{4} + \frac{\gamma + \mu}{2}\big)\Big] \tag{2.5}$$

In eqs. (2.2) - (2.5) the Thevenin impedance is assumed to be purely reactive so as to simplify the analysis, though this is not mandatory. The form of eq. (2.5) with the Thevenin impedance having a resistive component can be found in [4].

2.2.2 Maximum Power Curve

The MPC is practically derived by computing the converter DC power P_d numerically as a function of the direct current I_d. This is done by first solving the power flow equations with the system operating under nominal conditions, i.e. U, U_d, I_d as 1 p.u. etc. Subsequently the Thevenin AC voltage magnitude is held fixed, when the power flow equations are solved to compute P_d for every value of I_d.

Example 1 Consider the single-infeed configuration of Figure 2.1 with the following system parameters; $\gamma = 17°$, $d_x = 0.08$ p.u., $b_c = 0.54$ p.u., $|z| = 0.576$, 0.496, 0.428, 0.379 ($ESCR = 1.2, 1.478, 1.8, 2.1$, respectively). $\theta = 90°$. The corresponding MPC's and converter AC bus voltages are shown in Figures 2.2 and 2.3, respectively.

For the given parameter values, it is seen from Figures 2.2 and 2.3 that the MAP condition occurs under nominal conditions (I_{MAP}, U, P_d are 1 p.u.) for a $CESCR$ of 1.4775. For $ESCR$ values less than this, the system operates on the right-side of the MPC maxima which implies unstable operation, e.g. the MPC for an $ESCR = 1.2$ in Figure 2.2. For $ESCR$ values greater than the $CESCR$, the system will operate on the left-side of the MPC maxima which implies stable operation, e.g. the MPC for an $ESCR = 1.8$ or 2.1 in Figure 2.2. The relationship between the MPC and eq. (2.2) is illustrated in Figure 2.4. In Figure 2.4, the zero of dP_d/dI_d as given by eq. (2.2) coincides with the maxima of the MPCs.

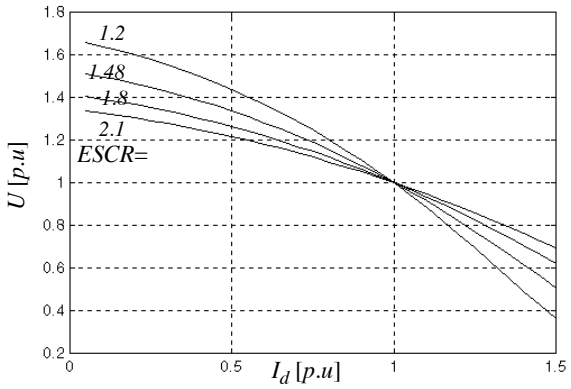

Figure 2.3. Converter AC bus voltage.

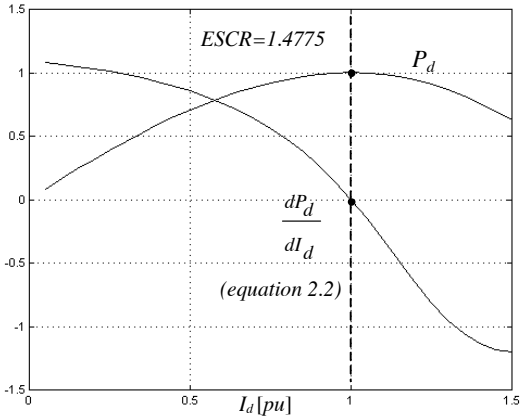

Figure 2.4. Relationship between eq. (2.2) and MPC.

2.3 Voltage Stability

2.3.1 Voltage Sensitivity

The *Voltage Sensitivity Factor* (VSF) was first introduced in [7] for the single-infeed configuration of Figure 2.1[1]. This is defined as the ratio of the incremental change in the voltage ΔU and reactive power ΔQ at the converter AC bus, given by

$$VSF = \frac{\Delta U}{\Delta Q} \tag{2.6}$$

The VSF is essentially the converter AC voltage sensitivity to the reactive power incremental change at the converter AC bus, and is used as a stability index. When the VSF is small and positive, a small change of reactive power

[1] In [7] the quantity was called *Voltage Stability Factor*, but we will use the more general term *Voltage Sensitivity Factor*.

induces a small and same directional change in the converter AC bus voltage. This characteristic is consistent with stable system behaviour. An increasing VSF corresponds to a decreasing voltage stability margin and when the VSF becomes infinite, the transition to an unstable system occurs. When the VSF is negative, a small change of the reactive power induces an opposite change in the converter AC bus voltage. This characteristic corresponds with unstable system behaviour.

The VSF can be derived mathematically from the same power flow equations used to formulate the gradient of the MPC in eq. (2.2). By the same linearization of these equations with respect to U and δ, and eliminating δ, the VSF is given by

$$VSF = \frac{\Delta U/U}{\Delta Q} = \frac{U^2 ESCR + Q_d}{U^4 ESCR^2 - Q_d^2 + U\frac{\partial Q_d}{\partial U}\Big(U^2 ESCR + Q_d\Big) + P_d\Big(P_d - U\frac{\partial P_d}{\partial U}\Big)} \tag{2.7}$$

where $\partial P_d/\partial U$ and $\partial Q_d/\partial U$ are the voltage dependence of the converter active and reactive power, respectively, and are given by the control mode as follows

CEA/Constant Power Control

$$\frac{\partial P_d}{\partial U} = 0\ ; \qquad \frac{\partial Q_d}{\partial U} = \frac{2}{U}\Big[Q_d - P_d \tan[\gamma + \mu)\Big] \tag{2.8}$$

CEA/Constant Current Control

$$\frac{\partial P_d}{\partial U} = \frac{2}{U}\big[\frac{P_d \cos\gamma}{\cos\gamma + \cos(\gamma+\mu)}\big]\ ; \qquad \frac{\partial Q_d}{\partial U} = \frac{2}{U}\big[Q_d - \frac{P_d \sin(\gamma+\mu)}{\cos\gamma + \cos(\gamma+\mu)}\big] \tag{2.9}$$

Constant DC Voltage/Constant Power Control

$$\frac{\partial P_d}{\partial U} = 0; \qquad \frac{\partial Q_d}{\partial U} = \frac{2}{U}\big[Q_d + P_d \cot(2\gamma+\mu)\big] \tag{2.10}$$

Example 2 Using the same parameter values as in Example 1 for the single-infeed configuration of Figure 2.1, the VSF as a function of $ESCR$ for different HVDC control modes are shown in Figure 2.5. It is seen that HVDC systems with constant DC voltage control have small VSF even for low $ESCR$, implying that this control mode is inherently stable. In contrast, constant power control is inherently unstable at low $ESCR$ as shown by the negative VSF below the $CESCR$.

2.4 Control Stability

2.4.1 Control Sensitivity Index

The concept of control sensitivity was introduced in [8], based on the single-infeed configuration of Figure 2.1. This is defined as the rate of change of a

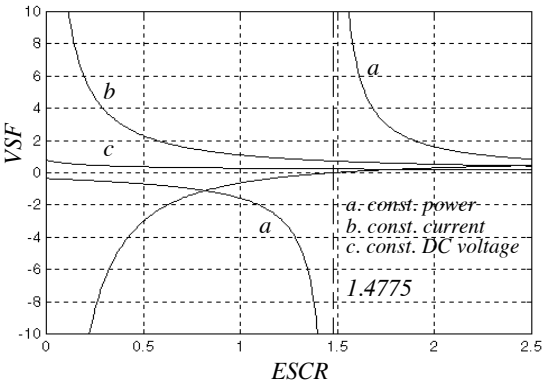

Figure 2.5. VSF for various control modes.

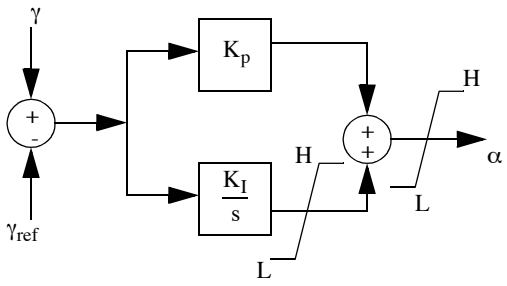

Figure 2.6. Inverter Constant Extinction Angle controller.

controlled parameter with respect to the controlling parameter. To illustrate, consider an example of the inverter CEA controller shown in Figure 2.6. The extinction angle γ (controlled parameter) is required to be controlled to specified value by directly varying the inverter firing angle α (controlling parameter). A suitable ratio $d\gamma/d\alpha$ may then be defined as a stability index for the controller. Stable controller action requires that an increase in α causes the system to respond with a decrease in γ, i.e. $d\gamma/d\alpha < 0$. Thus a negative $d\gamma/d\alpha$ indicates stable system characteristics with respect to the controller action, and vice versa. For other control strategies, similar ratios may be defined. In general, a *Control Sensitivity Index* (CSI) [8] commensurating with the control principle may be defined as the stability index, those for typical controllers are as given in Table 2.1.

2.4.2 CSI Computation

The CSI may be computed from the power flow Jacobian at the steady-state operating point under investigation. To this end, the system steady-state operating point is first obtained by a Newton-Raphson power flow solution. The Jacobian which is derived from linearization of the power flow equations with respect to the operating state vector, is then computed at this operating point.

Rectifier	Inverter	CSI
const. current	CEA	$d\gamma/d\alpha$
const. power	CEA	dP_d/dI_d
const. current	cons. voltage	$dU/d\alpha$

Table 2.1. Common CSI definitions.

The power flow equations comprise AC power balance equations at the converter AC bus, and converter steady-state DC power, current, and voltage equations. This set of six equations can be found in [8].

The operating state vector comprises system states which will vary during dynamic operation of the system. Its composition depends on the control mode under consideration but includes the controlled and controlling system states. For the system model of Figure 2.1, the operating state vector v_{xy} is $(\alpha, \phi, \delta, U_t, U_d, I_d, P_d)$ for constant power (constant γ), $(\alpha, \gamma, \phi, \delta, U_t, U_d, P_d)$ for CEA (constant current) and constant DC voltage (constant current), control. α and ϕ are the inverter firing angle and power factor at inverter AC bus, respectively, and other symbols are self-explanatory from Figure 2.1.

Thus the Jacobian, say J_{xy}, computed at the operating point (power flow solution) is given by

$$J_{xy} \cdot \Delta v_{xy} = 0 \tag{2.11}$$

Rewriting eq. (2.11) gives

$$J_x \Delta v_x + J_y \Delta v_y = 0 \tag{2.12}$$

where $v_{xy} = (v_x, v_y)$, J_x is a 6x6 square matrix comprising columns of J_{xy} related to the v_x system states and J_y is a single column of J_{xy} corresponding to the single controlling system state v_y. Thus from eq. (2.12)

$$\frac{\Delta v_x}{\Delta v_y} = -J_x^{-1} J_y \tag{2.13}$$

One of the elements of the vector in eq. (2.13) then defines the CSI as according to Table 2.1, for the control mode under consideration. For example for the CEA control mode, the first element of $\Delta v_x/\Delta v_y$ defines the CSI, i.e. $d\gamma/d\alpha$.

Example 3 Consider the single-infeed configuration of Figure 2.1 with the following system parameter values taken from [8]; $X_c = 0.18$ p.u., $SCR = 1.01$, $b_c = 0.567$ p.u., $\gamma_{min} = 15°$, $\alpha = 164.7°$ $(= 180° - \gamma_{min} - \mu)$. The computed CSI for the constant power control modes as in Table 2.1 is shown in Figure 2.7.

2.5 Extension to Higher-Order Models

Recent works have extended the concepts of maximum power and voltage sensitivity to multi-infeed and single-infeed with parallel AC line configurations as shown in Figure 2.8 and Figure 2.9, see refs. [9], [12], [14]. In this section the basic power and voltage stability analysis methods incorporating these concepts are developed for these two system configurations.

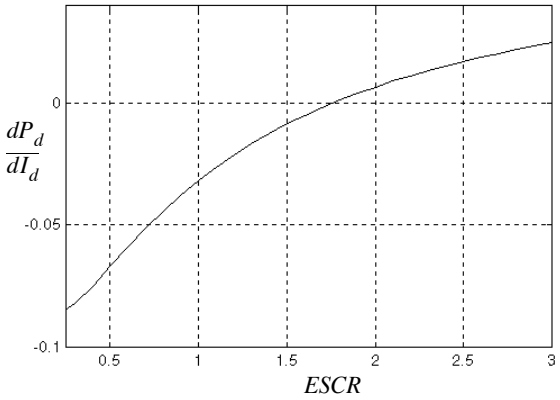

Figure 2.7. Control Sensitivity Indices.

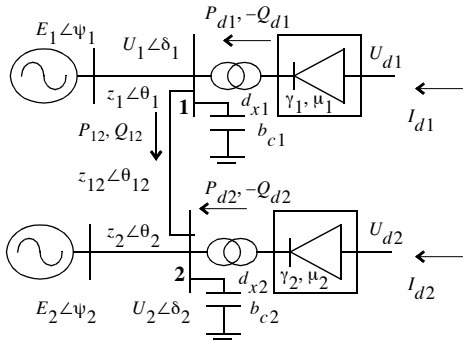

Figure 2.8. Simplified multi-infeed HVDC configuration.

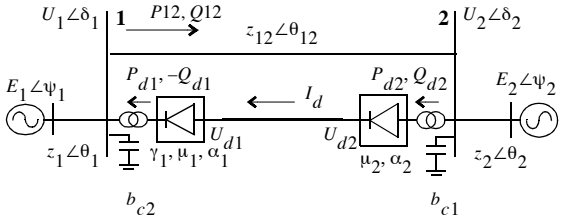

Figure 2.9. Single-infeed with parallel AC line configuration.

2.5.1 Maximum Power

Similar to the single-infeed case, the power stability methods for these higher-order system configurations are derived from their linearized power flow equations. These equations also assume constant Thevenin voltages, thus the source

buses are eliminated in the power flow solution model, given by

$$\begin{pmatrix} \Delta P_d \\ \Delta P_{ac} \\ \Delta Q_{ac} \end{pmatrix} = \begin{pmatrix} J_{dI} & 0 & J_{dU} \\ J_{PI} & J_{P\delta} & J_{PU} \\ J_{QI} & J_{Q\delta} & J_{QU} \end{pmatrix} \begin{pmatrix} \Delta I_d \\ \Delta \delta \\ \Delta U/U \end{pmatrix} \tag{2.14}$$

where;

ΔP_d is a vector of incremental DC power at the converter DC buses.

ΔP_{ac} is vector of incremental AC active power at the converter AC buses.

ΔQ_{ac} is a vector of incremental AC reactive power at the converter AC buses.

ΔI_d, $\Delta \delta$, and $\Delta U/U$ are vectors of incremental change in the system states comprising the DC current, converter AC bus voltage angle and relative magnitude, respectively.

The Jacobian submatrices are the partial derivatives of the power flow equations with respect to the system states. The subscript labels d, ac denote the quantities related to the DC power, AC active and reactive power, respectively. Note that I_d is additionally chosen as a system state so that the Jacobian is an extended form of the well known Newton-Raphson model. The expressions for these Jacobian submatrices are given in [17].

For no active or reactive power injections at the converter AC buses, ΔP_{ac} ,ΔQ_{ac} may be assumed to be zero. Thus eq. (2.14) may be reduced to

$$\Delta P_d = J_{MPC} \Delta I_d \tag{2.15}$$

where

$$J_{MPC} = J_{dI} - J_{dU} J_{R1}^{-1} J_{R2}, \qquad J_{R1} = J_{QU} - J_{Q\delta} J_{P\delta}^{-1} J_{PU}$$

and

$$J_{R2} = J_{QI} - J_{Q\delta} J_{P\delta}^{-1} J_{PI}$$

Standard MPC (SMPC) approach

In eq. (2.15), the diagonal and off-diagonal elements of J_{MPC} give the intra and inter $\Delta P_d - \Delta I_d$ relationship, respectively, of the constituent converters in Figures 2.8 and 2.9. The maximum power concept for the single-infeed case is directly extended to a referenced constituent converter by using only its intra $\Delta P_d - \Delta I_d$ relationship and constraining the other non-referenced constituent converters to be invariant. From eq. (2.15), this is equivalently given by

$$\left. \frac{\Delta P_{d_i}}{\Delta I_{d_i}} \right|_{\Delta I_{d_j}=0} = J_{MPC_{ii}} \qquad i = 1, 2 \quad j \neq i \tag{2.16}$$

where $J_{MPC_{ii}}$ is the i-th diagonal element of J_{MPC}. When $J_{MPC_{ii}}$ vanishes, eq. (2.16) is akin to eq. (2.1) for the single-infeed case. Thus $J_{MPC_{ii}}$ is used to determine the MAP condition for these higher- order configurations. Similar to the single-infeed MPC, the SMPC for the higher-order configurations may also be derived. This is done practically by numerically computing the DC

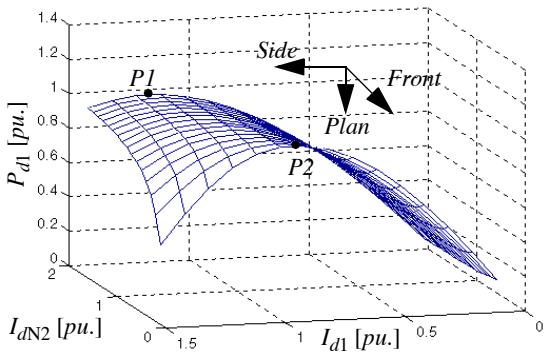

Figure 2.10. Three dimensional view of the SMPC surface.

power of a referenced constituent converter as a function of its DC current while constraining the DC current of the other non-referenced constituent converters as constant parameters, in accordance with eq. (2.16). All voltage magnitudes of Thevenin AC voltage sources are also assumed to be fixed at values determined for nominal conditions, i.e. I_{d_1}, I_{d_2}, U_{d_1}, U_{d_2}, U_1, U_2 as 1 p.u.

Example 4 To illustrate the derivation of the SMPC, consider the multi-infeed configuration of Figure 2.8 with the following system parameters: $ESCR1 = 1$, $ESCR2 = 3$, $z_{12} = 0.6$ p.u., I_{d_1} is a variable and I_{d_2} is a constant parameter taking values from 0.1 to 1.6 p.u. Figure 2.10 shows the resulting three dimensional SMPC surface which is twisted-saddle shaped. The surface is a composite of many MPC's, each of which is the MPC of the referenced converter with respect to I_{d_1} for a given value of I_{d_2}. This is clearly shown in Figure 2.11 which is the front projection of the SMPC surface of Figure 2.10. Thus, the MAP and I_{MAP} for every MPC may be determined as the operating point corresponding to eq. (2.1) for each given value of I_{d_2}. Figure 2.12 shows the plan projection of the SMPC surface. The curve corresponds to the ridge of the SMPC surface, i.e. the loci of the MAP of every MPC of the composite surface. This curve is thus defined as the SMPC power stability boundary.

Modal MPC (MMPC) approach

The SMPC approach gives only a system-specific or local assessment of power stability, by virtue of allowing only a single degree of freedom for DC current variation. Another approach to investigate system power stability is to apply an eigenvalue decomposition technique to J_{MPC}. This is expected to give a more system-wide or global assessment of system power stability since this technique treats J_{MPC} in its entirety and no constraints on the degrees of freedom for DC current variation are imposed. Thus decomposing J_{MPC} into its eigenvalue equivalent, assuming this is always possible, gives

$$J_{MPC} = \Psi \Lambda_{MPC} \eta \tag{2.17}$$

where

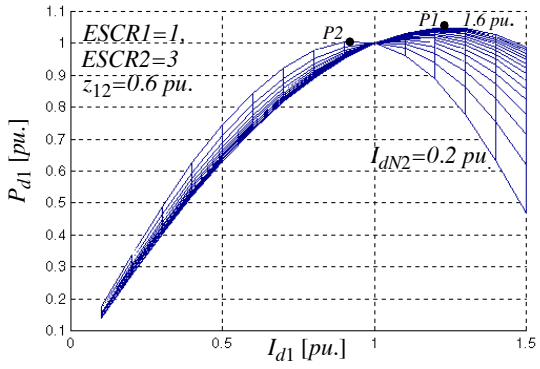

Figure 2.11. Front projection of the SMPC surface.

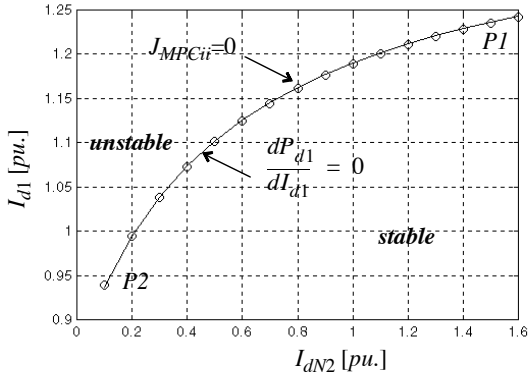

Figure 2.12. Plan projection of the SMPC surface.

Ψ is the right column eigenvector matrix of J_{MPC}.

η is the left column eigenvector matrix of J_{MPC}.

Λ_{MPC} is a diagonal matrix with i-th diagonal element as the i-th mode eigenvalue λ_i.

Applying eq. (2.17) to eq. (2.15), and noting that $\Psi^{-1} = \eta$ gives

$$\Delta p_d = \Lambda_{MPC} \Delta i_d \tag{2.18}$$

where $\Delta p_d = \eta \Delta P_d$ and $\Delta i_d = \eta \Delta I_d$ are the vector of incremental modal DC power and DC current, respectively. For the i-th eigenmode, eq. (2.18) can be written as

$$\frac{\Delta p_{d_i}}{\Delta i_{d_i}} = \lambda_i \tag{2.19}$$

where

$$\Delta p_{d_i} = \sum_{j=1}^{n_t} \eta_{ij} \Delta P_{d_j}, \quad i = 1, \ldots, n_t \tag{2.20}$$

$$\Delta i_{d_i} = \sum_{j=1}^{n_t} \eta_{ij} \Delta I_{d_j}, \quad i = 1, \ldots, n_t \tag{2.21}$$

and n_t is the number of converter AC buses.

It is seen from eq. (2.19) that the sign of the eigenvalue determines the direction of the incremental relationship. Positive eigenvalues cause positive modal DC power changes in response to positive modal DC current variations, and vice versa for negative eigenvalues. At the transition of signs, the minimum eigenvalue becomes zero and eq. (2.19) becomes

$$\frac{\Delta p_{d_i}}{\Delta i_{d_i}} = 0 \tag{2.22}$$

This is akin to eq. (2.1) for the single-infeed case. However, this is a modal relationship, thus corresponding to the MPC for the single-infeed configuration, the *Modal Maximum Power Curve* (MMPC) may be defined using eq. (2.19). The system operating conditions resulting in eq. (2.22) would thus represent the *Modal Maximum Available Power* of the system. Alternatively, eq. (2.19) may be expressed as

$$\frac{\Delta i_{d_i}}{\Delta p_{d_i}} = \frac{1}{\lambda_i} \tag{2.23}$$

Again, positive eigenvalues cause positive modal DC current changes in response to positive modal DC power order variations. This corresponds to stable DC power control behaviour. For a zero minimum eigenvalue, an infinitesimally small change in the modal DC power order causes an infinite change in the modal DC current, hence instability of the DC power control. Therefore, for stable DC power behaviour eq. (2.19) and eq. (2.23) imply

$$\lambda_{min} > 0 \; ; \qquad \lambda_{min} = min\{\lambda_1, \ldots, \lambda_{n_t}\} \tag{2.24}$$

Eq. (2.19) may be used to derive graphical plots in parameter space to define the MMPC stability boundary. In such case, the plots are values of parameters for which the system minimum eigenvalue, λ_{min}, becomes zero. Thus, the plots are the MMPC stability boundaries that demarcate the parameter space into stable and unstable regions.

Example 5 Consider the multi-infeed configuration of Figure 2.8 with the following system parameter values: $ESCR1 = 1$, $ESCR2 = 3$, $z_{12} = 0.6$ p.u. The MMPC stability boundary in the $P_{dN_1} - P_{dN_2}$ parameter space (the subscript label N denotes rated quantities) is shown by the plot in Figure 2.13. In Figure 2.13, the region above and below the curve are thus unstable and stable regions, respectively. The curve comprises values of the parameters for which λ_{min} becomes zero, thus it is the system MMPC stability boundary.

2.5.2 Voltage Sensitivity

Minimum Eigenvalue

The concept of voltage sensitivity is similarly extended to the higher-order configurations, using the power flow solution model for the single-infeed case. For

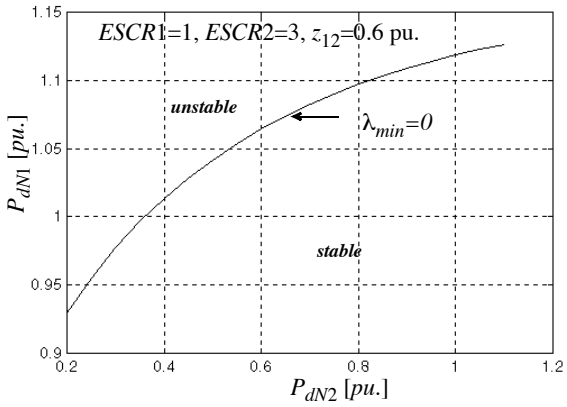

Figure 2.13. MMPC stability boundary in P_d space.

the case of higher order configurations, it is given by

$$\begin{pmatrix} \Delta P \\ \Delta Q \end{pmatrix} = \begin{pmatrix} J_{P\delta} & J_{PU} \\ J_{Q\delta} & J_{QU} \end{pmatrix} \begin{pmatrix} \Delta\delta \\ \Delta U/U \end{pmatrix} \tag{2.25}$$

where

ΔP is a vector of incremental change in converter AC bus active powers.

ΔQ is a vector of incremental change in converter AC bus reactive powers.

$\Delta\delta$ is a vector of incremental converter AC bus voltage angles.

$\Delta U/U$ is a vector of incremental converter AC bus relative voltage magnitudes.

$J_{P\delta}$, J_{PU}, $J_{Q\delta}$, J_{QU} are the partial derivatives of the power flow equations with respect to the voltage angles and magnitudes.

If the active power is held constant at the converter AC buses and only incremental reactive power is applied, then ΔP may be assumed to be zero, and eq. (2.25) thus reduces to

$$\Delta Q = J_R \frac{\Delta U}{U} \tag{2.26}$$

where $J_R = J_{QU} - J_{Q\delta} J_{P\delta}^{-1} J_{PU}$ is the QU reduced Jacobian matrix. Alternatively, eq. (2.26) can be expressed as

$$\frac{\Delta U}{U} = J_R^{-1} \Delta Q \tag{2.27}$$

Though eq. (2.27) appears similar to the VSF in eq. (2.6), there is no direct relationship for the converter AC bus in question, due to the coupling from the other non-zero off-diagonal elements of J_R^{-1}. To obtain a decoupled form, an eigenvalue decomposition technique similar to the MMPC approach in subsection 2.5.1 may be used. Thus applying the same decomposition to J_R^{-1} in eq. (2.27) gives

$$\Delta u_i = \frac{\Delta q_i}{\lambda_i} \tag{2.28}$$

where

$$\Delta u_i = \sum_{j=1}^{n_t} \eta_{ij} \frac{\Delta U_j}{U_j} \qquad \Delta q_i = \sum_{j=1}^{n_t} \eta_{ij} \Delta Q_j \qquad i = 1, \ldots, n_t$$

Δu_i is i-th mode of incremental modal voltage.

Δq_i is i-th mode of incremental modal reactive power.

$\Delta \lambda_i$ is i-th mode eigenvalue of the QU reduced Jacobian matrix, J_R.

$\Delta \eta_i$ is i-th row left eigenvector of the QU reduced Jacobian matrix, J_R.

n_t is the number of converter AC buses.

It is seen that there is now a direct $\Delta U/\Delta Q$ relationship in eq. (2.28), similar to the VSF in eq. (2.6). However, the relationship is in modal form, thus eq. (2.28) may be considered as the modal VSF ($MVSF$), i.e. the multi-dimensional equivalent of the single-infeed VSF.

The $MVSF$ can be used as stability indicator, similar to the VSF. From eq. (2.28), for positive λ_i the incremental modal voltage is "in phase" or changes in the same direction with the incremental modal reactive power. This corresponds with voltage stable situations. However, when λ_i is negative, the incremental modal voltage is in "anti-phase" or changes in the opposite direction with the incremental modal reactive power. This corresponds to voltage unstable situations. At the transition between the stable and unstable region of operation, λ_i becomes zero meaning that any infinitesimal change in modal reactive power causes infinite modal voltage change. Thus, the bus voltage would also be correspondingly unstable since the incremental modal voltage is a linear combination of the incremental bus voltages. Thus for a system to be voltage stable, the minimum eigenvalue λ_{min} must be positive at every operating point:

$$\lambda_{min} > 0 \qquad \lambda_{min} = min\{\lambda_1, \ldots, \lambda_{n_t}\} \tag{2.29}$$

Example 6 Consider the multi-infeed configuration of Figure 2.8 with the following system parameters; $P_{dN1} = 1$ p.u., $P_{dN2} = 0.5$ p.u., $z_{12} = 0.6$ p.u. Figure 2.14 shows the $MVSF$ stability boundary in the $ESCR1 - ESCR2$ parameter space. For all $ESCR$ values on the boundary, λ_{min} is zero.

Participation Factors

For the modal approach, not only is the minimum eigenvalue useful in estimating the proximity to voltage instability but the eigenvectors also contain information concerning how critical system locations are. The eigenvectors may be used to define a *participation factor* [11] given by

$$p_{ij} = \Psi_{ij} \eta_{ji} \tag{2.30}$$

where

p_{ij} is the participation factor for the converter AC bus i in the j-th voltage variation mode

$\Delta \eta_{ji}$ is the i-th element of the j-th row left eigenvector matrix.

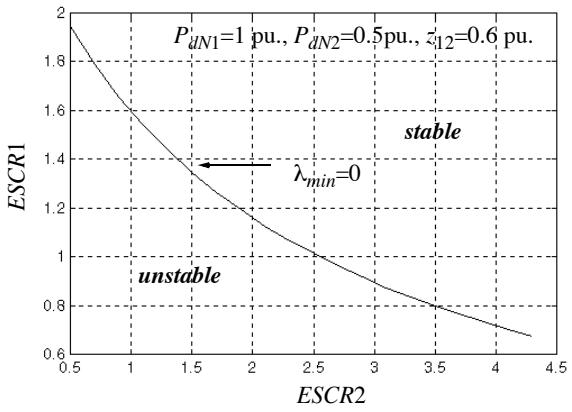

Figure 2.14. $MVSF$ stablity boundary in $ESCR$ space.

$\Delta\Psi_{ij}$ is the i-th element of the j-th column right eigenvector matrix.

n_t is the number of converter AC buses.

Physically, Ψ_{ij} is a measure of the activity of converter AC bus i in the j-th voltage variation mode, η_{ji} is the weighting of the contribution of this activity, their product p_{ij} is a measure of the net participation of bus i in the j-th voltage variation mode.

In the context of multi-infeed configurations, bus participation factors computed from the eigenvectors associated with the minimum eigenvalue provide information on the critical converter AC bus. The bus with the largest participation factor is the critical bus. Consequently it is also the most effective system location for implementation of remedial measures [13].

2.6 Incorporation of Local Devices

The equations developed in the preceding sections do not consider any system component, e.g. loads, compensators, connected locally at the converter AC bus. However, these devices could impact significantly on the power/voltage stability of the AC/ DC interconnection [9], [15], [16].

2.6.1 Loads

In this subsection, the basic equations associated with power stability are presented for the various system configurations with static loads connected at the converter AC buses as shown in Figures 2.15 - 2.17. It is assumed that the load models have static load characteristics given by

$$\frac{P}{P_L} = K_{PC} + K_{PI}U + K_{PZ}U^2 + K_{PU}U^{n_{PU}} \tag{2.31}$$

$$\frac{Q}{Q_L} = K_{QC} + K_{QI}U + K_{QZ}U^2 + K_{QU}U^{n_{QU}} \tag{2.32}$$

where

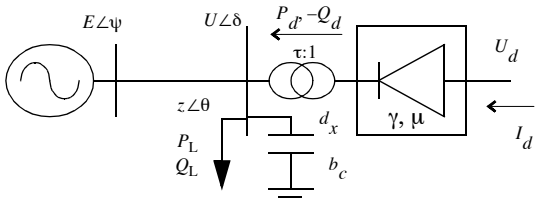

Figure 2.15. Simplified single-infeed configuration incorporating static load models.

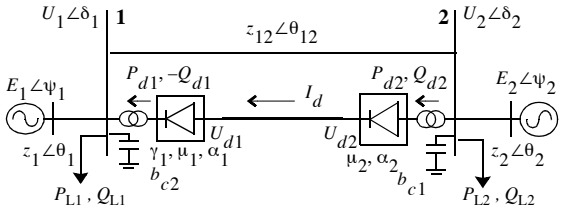

Figure 2.16. Single-infeed with parallel AC line configuration incorporating static load models.

$K_{PI} = 1 - (K_{PC} + K_{PZ} + K_{PU})$

$K_{QI} = 1 - (K_{QC} + K_{QZ} + K_{QU})$

$K_{PC},\ K_{QC}$ is the per unit of constant MVA active and reactive load, respectively.

$K_{PI},\ K_{QI}$ is the per unit of constant current active and reactive load, respectively.

$K_{PZ},\ K_{QZ}$ is the per unit of constant impedance active and reactive load, respectively.

$K_{PU},\ K_{QU}$ is the per unit of voltage dependent active and reactive load, respectively.

$n_{PU},\ n_{QU}$ is the voltage sensitivity exponent for active and reactive load, respectively.

$P_L,\ Q_L$ is the nominal (initial) active and reactive load, respectively.

Using the same approach as in subsections 2.2.1 and 2.5.1, the power flow equations incorporating the load models of eqs . (2.31) and (2.32) are similarly linearized and reduced to give the following.

For the single-infeed configuration, Figure 2.15, the following holds

$$\frac{dP_d}{dI_d} = \frac{rU\cos(\gamma+\mu)\left[U^4 ESCR^2 + (b+KQ)\left(U^2 ESCR + \widetilde{Q}_d\right) - \widetilde{Q}_d^2 - \widetilde{P}_d\overline{P}_d\right]}{\det J_I} \tag{2.33}$$

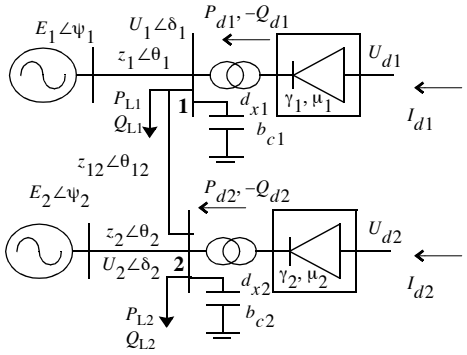

Figure 2.17. Simplified multi-infeed configuration incorporating static load models.

where r, b are as given in subsection 2.2.1 and

$$\det J_I = U^4 ESCR^2 - \widetilde{Q}_d^2 + \left(U \frac{\partial Q_d}{\partial U}\bigg|_{I_d} + KQ \right)\left(U^2 ESCR + \widetilde{Q}_d\right) - P\left(P - U\frac{\partial P_d}{\partial U}\bigg|_{I_d} + U\frac{\partial P_L}{\partial U} \right)$$

The zero of eq. (2.33) solves to give

$$CESCR = \frac{1}{U^2}\left[-\frac{b+KQ}{2} + \sqrt{\left(\frac{b+KQ}{2} - \widetilde{Q}_d\right)^2 + \widetilde{P}_d \overline{P}_d} \;\right] \tag{2.34}$$

where

$\widetilde{P}_d = P_d - P_L$, $\overline{P}_d = P_d + KP$ and $\widetilde{Q}_d = Q_d + Q_L$

$KP = [-K_{PC} + K_{PZ}U^2 + (n_{PU} - 1)K_{PU}U^{n_{PU}}]P_L$

$KQ = [K_{QI}U + 2K_{QZ}U^2 + n_{QU}K_{QU}U^{n_{QU}}]Q_L$

$U\dfrac{\partial P_L}{\partial U} = [K_{PI}U + 2K_{PZ}U^2 + n_{PU}K_{PU}U^{n_{PU}}]P_L$

The basic equations for the multi-infeed and single-infeed with a parallel AC line configurations are identical in form, given by

$$\overline{CESCR1} = \frac{1}{U^2}\left[-\frac{b' + KQ_1}{2} + \sqrt{\left(\frac{b+KQ_1}{2} - \widetilde{Q}_{d1}\right)^2 + (\widetilde{P}_{d1}\overline{P}_{d1} + P_0 + Q_0)} \;\right] \tag{2.35}$$

where the quantities involved are given in chapter 8 of ref. [17].

2.6.2 Other Devices

For a general device connected at the converter AC bus of the single-infeed configuration, a general expression defining the MAP condition may be derived

as

$$\frac{dP_d}{dI_d} = \left(rU\cos(\gamma+\mu)\left[U^4 ESCR^2 + \left(b + U\frac{\partial Q_d}{\partial U}\right)\left(U^2 ESCR + Q_d\right) \right.\right. \\ \left.\left. - Q_d^2 - P_d\left(P_d - U\frac{\partial P_d}{\partial U}\right)\right]\right) / \det J_I \tag{2.36}$$

where r, b, and $\det J_I$ are as previously defined. Here, $\partial P_d/\partial U$, $\partial Q_d/\partial U$ are the voltage dependence of the active and reactive power output, respectively, of the locally connected device. For example, an SVC whose power out given by

$$P_{SVC} = 0 \qquad Q_{SVC} = K_{SVC}U \tag{2.37}$$

within its linear control range would have voltage dependence given by

$$\frac{\partial P_{SVC}}{\partial U} = 0 \qquad \frac{\partial Q_{SVC}}{\partial U} = K_{SVC} \tag{2.38}$$

From eq. (2.36), the MAP condition for the single-infeed configuration of Figure 2.1 with a general device locally connected may be similarly specified and the $CESCR$ derived.

2.7 Relationship Between Power and Voltage Stability Methods

The relationship between the power and voltage stability analysis methods for the various system configurations is shown in this section.

It was first shown in [10], for the single-infeed configuration of Figure 2.1 with the converter operating in CEA/constant power control mode, that the MAP condition coincides with the VSF becoming infinite at the same operating point. This is shown for sample system parameter values in Figure 2.18 where the VSF tends to infinity and the dP_d/dI_d index becomes zero at the same $ESCR$ value, i.e. $CESCR = 1.4775$.

It can be also shown, [14],[17], for the multi- infeed configuration with all converters operating in CEA/constant power control, that the MMPC and $MVSF$ stability boundaries coincide, i.e. λ_{MPC} and λ_{VSF} become zero for the same parameter values in the parameter space. An example is shown in Figure 2.19 where the $MVSF$ (circle) and MMPC (solid line) stability boundaries coincide in the $ESCR2 - z_{12}$ space.

It can be further shown, [14],[17], that the MMPC and $MVSF$ methods for the multi-infeed configuration, formulated from eqs. (2.15) and (2.26), respectively, decouples into the VSF and MPC methods for the single-infeed configuration when z_{12} tends to infinity.

These relationships can be illustrated by a relationship structure as shown in Figure 2.20. From this diagram it is seen that the modal technique extends the power/voltage stability analysis methods for the single-infeed to those for the multi-infeed configuration, and vice versa.

In a more general context, the relationship between the various maximum power and voltage sensitivity based methods for the various system configurations, viz. Figures 2.15 - 2.17, was shown in [15], [17]. These relationships, summarized in Table 2.2, hold with or without load models locally connected at the converter AC buses.

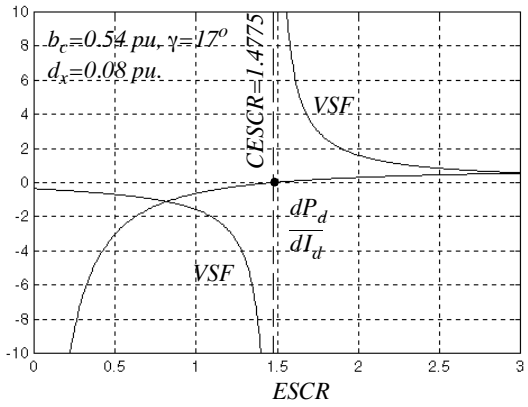

Figure 2.18. Relationship between VSF and MPC for single-infeed configuration in constant power control.

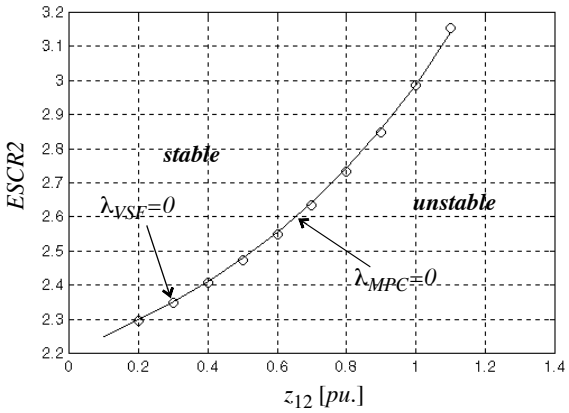

Figure 2.19. Relationship between MMPC and $MVSF$ stability boundary for multi-infeed configuration in constant power control.

Example 7 These relationships are also illustrated in Figures 2.21 - 2.23 for the various system configurations of Figures 2.15 - 2.17 having the following sample parameters: $P_{L1} = P_{L2} = 0.1$ p.u. (constant impedance), $Q_{L1} = Q_{L2} = 0.075$ p.u. (constant MVA), $z_{12} = 0.6$ p.u., $\gamma_1 = \gamma_2 = 17°$, $b_{c1} = b_{c2} = 0.54$ p.u., $d_{x1} = d_{x2} = 0.08$ p.u. Initial conditions are $P_{12} = 0.2$ p.u. (for multi-infeed) and - 0.2 p.u. (for single-infeed with parallel AC line), and U_{d1}, U_{d2}, I_{d1}, I_{d2}, U_1, U_2 are all 1 p.u. For the multi-infeed and single-infeed with parallel AC line configurations, the constituent converter of interest is the referenced system and

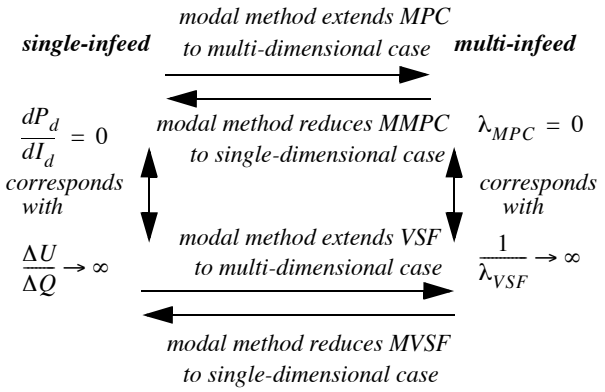

Figure 2.20. Relationship structure for voltage/power stability analysis methods with converters in constant power control.

Configuration	Maximum Power	Voltage Sensitivity
Single-Infeed	MPC	VSF
Single-Infeed with parallel AC line	MPC	$MSVF$ (constant power)
Multi-Infeed	SMPC	$MVSF$ (constant power, constant current)
Multi-Infeed	MMPC	$MVSF$ (constant power, constant power)

Table 2.2. Relationship between power and voltage stability methods with and without load models.

the neighbouring constituent converter is then the influencing system. For the single-infeed configuration, the parameter subscript indices are omitted and only the relevant parameters apply. Note that the relationship for the multi-infeed configuration without incorporating load models is not shown in Figure 2.22, but the correspondence is similar to Figure 2.19.

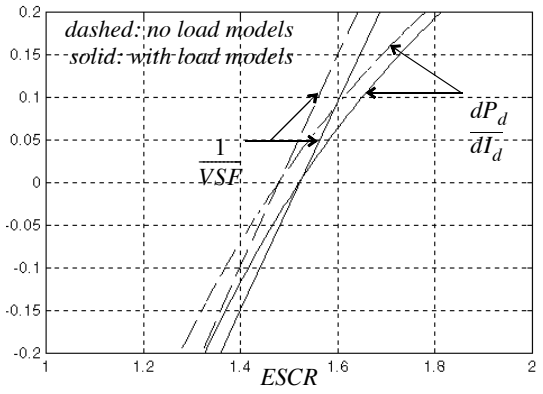

Figure 2.21. Coincidence of VSF and MPC for single-infeed configuration with and without load models.

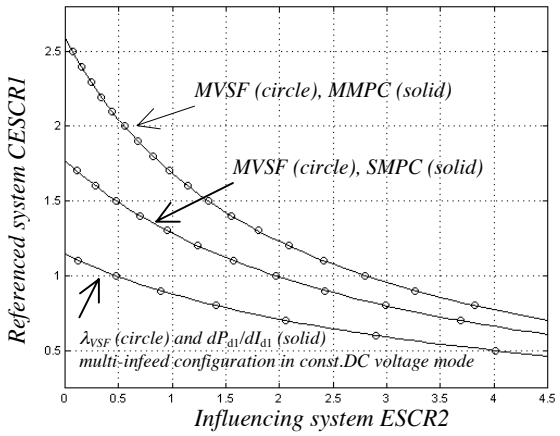

Figure 2.22. Stability boundaries for multi-infeed configuration with load models.

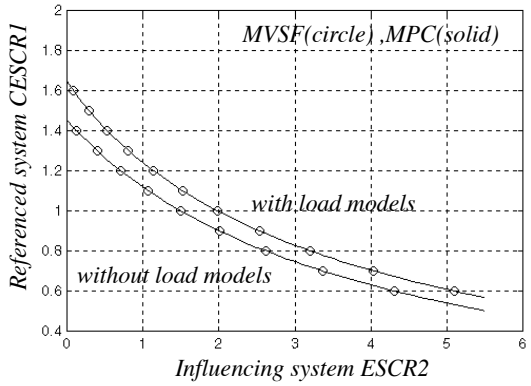

Figure 2.23. Stability boundaries for single-infeed configuration with parallel AC line with and without load models.

2.8 Appendix: Definition of ESCR

Since the single-infeed configuration of Figure 2.1 is a single converter system, the system MVA base could be uniquely chosen as the converter rated DC power. Consequently, the $ESCR$ for the system could be uniquely defined. For higher-order configurations, the situation is somewhat ambiguous since there are multiple constituent converters, each with its individual rated DC powers. Thus, the $ESCR$ for a constituent converter with a DC power rating different from the common MVA base, cannot be defined with the usual meaning, i.e. with respect to its own DC power rating. To resolve this, one constituent converter, say the i-th, can be chosen as the reference. Then the $ESCR$ of this reference constituent AC/DC system, $ESCR_i$, is defined in the usual meaning as

$$ESCR_i = \frac{1}{z_i} - b_{ci} \tag{2.39}$$

where z_i, b_{ci} are in p.u. with the rated DC power P_{dNi}, rated AC voltage U_N, as the common system MVA and voltage base, respectively. Now, a DC *Power Base Ratio* (PBR_j) is defined as the rated DC power of a constituent converter, say j-th, with rated DC power P_{dNj}, relative to the reference system and given by

$$PBR_j = \frac{P_{dNj}}{P_{dNi}} \tag{2.40}$$

Then, the $ESCR$ of the j-th constituent AC/DC-system, $ESCR_j$, can be defined as

$$ESCR_j = \frac{1}{PBR_j}\Big[\frac{1}{z_j} - b_{cj}\Big] \tag{2.41}$$

where $ESCR_j$ is thus defined with respect to its own MVA base, i.e. P_{dNj}, consistent with the usual definition. However, z_j, b_{cj} are still in p.u. on the common MVA and voltage base, i.e. P_{dNi} and U_N respectively. In this chapter, references to $ESCR$ associated with the higher-order configurations are made in the context of the above definitions. Also d_x is defined as follows

$$d_x = \frac{X_c I_{dN}}{\sqrt{2} U_N \tau_N} \tag{2.42}$$

where X_c, τ_N are the converter transformer reactance and turns ratio, respectively. The subscript label N denotes rated quantities.

3
Comparison of MPC with Detailed Simulations

Several indices have been developed for the stability analysis of HVDC Systems. Ainsworth [5] introduced the concept of *Maximum Available Power* (MAP). This index defines the stability limit for an HVDC System with the rectifier controlling the DC power and the inverter operating at constant extinction angle. Hammad [7] has introduced the *Voltage Stability Factor* (VSF) in which the change in sign of the ratio ($\Delta Q/\Delta V$); or incremental reactive power to incremental voltage determines the onset of instability. Similar indices have been introduced by Franken and Andersson [10], and by Nayak et al [8]. These indices are typically based on the steady-state DC equations and thus do not represent the full dynamic behavior of the system.

More recently, several investigators have attempted to determine the accuracy of these indices. Franken et al [10] have used stability programs, as Pilotto [18], Nayak [8] have attempted to use electromagnetic transient (EMTP-type) programs. These analyses generally confirm the usefulness of the steady state indices. However, recent studies by Reeve et al [9] that consider AC and DC lines in parallel and a more detailed load representation, show variations from results obtained from the straightforward calculation of these indices.

Similar discrepancies may arise when synchronous compensators are present at the converter bus. In this case the effective short circuit ratio ($ESCR$) is calculated assuming the transient impedance (X'_d) of the synchronous compensator to be lumped with the impedances of the external AC network and filter. This $ESCR$ value is later used in the calculation of the MPC. The details of the excitation control system are also usually ignored. In this section the MPCs obtained with the simplified model are compared with those obtained using a detailed electromagnetic transient simulation model.

The study system is derived from the first CIGRE HVDC benchmark [19] (60 Hz). The following changes are made to the benchmark: Inclusion of a local load at the inverter bus of 300 MVA, 0.95 power factor local load at the inverter bus. Inclusion of a synchronous compensator rated -165/+300 Mvar on the bus. The resultant system is shown in Figure 3.1.

3.1 Simulations Using a Simplified Model

As a first step, the MPC was calculated for this system using the steady-state DC and AC equations. The machine was represented by its transient reactance behind a fundamental frequency AC source as is customary in most studies. The transient simulation model was also similarly simplified resulting in the equivalent setup shown in Figure 3.2.

The AC sources were selected to provide rated bus voltage at rated DC current. The MPC in this case is a plot of the delivered DC power v/s the DC

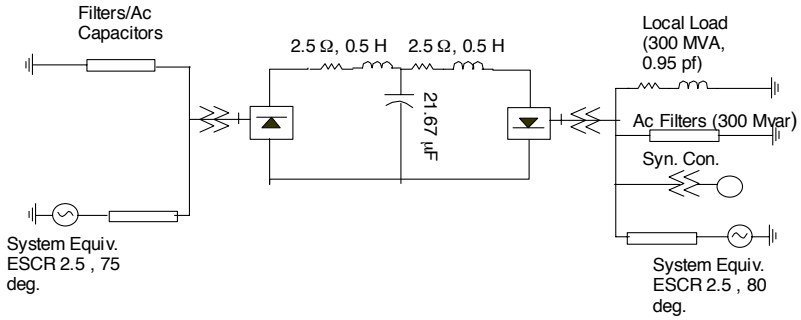

Figure 3.1. Modified CIGRE benchmark model [19].

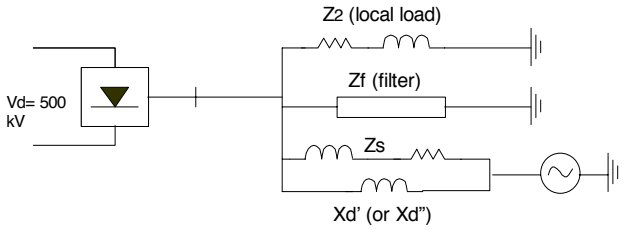

Figure 3.2. Simple test system.

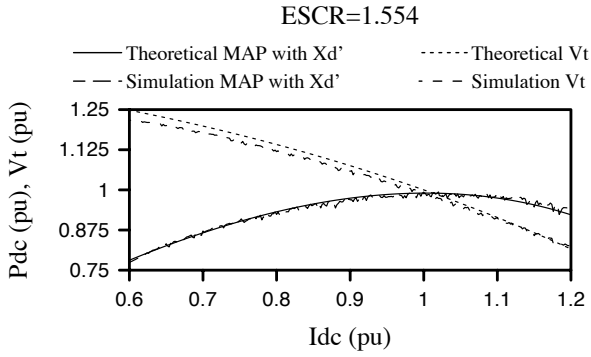

Figure 3.3. Comparison of theoretical and simulated MPC assuming a simple network equivalent.

current (see solid curve in Figure 3.3). A system in power control is stable when its operating point lies to the left of the peak of the resultant inverted parabola shaped curve. This is because the power controller effects an increase in power by requesting an increase in DC current, consistent with the rising curve to the left of the peak. Obviously, to the right of the peak, a current increase causes a power decrease resulting in the instability of the power control mode.

Figure 3.3. shows the theoretically calculated curves for DC power and AC bus voltage obtained from steady-state equations (see Appendix, section 3.4)

superposed on the simulated curve, obtained from a detailed electromagnetic transient simulation. The selected $ESCR$ of 1.554 is the critical $ESCR$, i.e. the onset of instability occurs at the rated DC current for this value. The simulated curve was obtained by ramping the DC current over 30 s (in a quasi steady-state manner) and recording the DC power. It should be noted that the MPC characteristic is derived using (simplified) steady-state equations, whereas the simulated model uses a far more detailed representation, with the individual switching of each thyristor and other non-linearities. Nevertheless, the two approaches yield identical results as seen in Figure 3.3; thereby indicating that the MPC approach is useful in the case where the AC system can be represented by a simple Thevenin equivalent.

3.2 Inclusion of a Synchronous Compensator at the Converter Bus

3.2.1 Differences Arising from Neglecting the Zero-Power Constraint for the Synchronous Compensator

This investigation was carried out in order to check whether the MPC approach can be used to determine the stability limits of inverters with synchronous compensators on the AC bus bar. In this particular study, the exciter response was not modelled and it was assumed that the field voltage of the machine remained at a fixed value. As the flatness of the MPC makes it difficult to determine the exact point at which the peak occurs, another equivalent approach is to plot the index $CSI = dP/dI_d$ as a function of the parameter being varied. The point at which this quantity crosses the horizontal axis is thus the transition point from stable to unstable operation. This index is also referred to as the controller sensitivity index for the constant power mode of operation [8], see also section 2.4.

It can be argued that lumping the synchronous compensator with the network equivalent as in Model 1 (Figure 3.1) is an oversimplification. This is because the actual synchronous compensator does not absorb or deliver any real power in the steady state. No such assumption is made in the traditional MAP which means that real power may be supplied or delivered by the synchronous machine. The equations in the Appendix, section 3.4, can be modified to include an additional constraint for the synchronous compensator so that it produces zero power. A new set of MAP (or equivalently CSI) curves now results as shown in Figure 3.4. The method for obtaining the simulated curves is as described in section 3.1.

In simplifying the machine to an equivalent, two assumptions are possible: Assume a synchronous reactance of X'_d or X''_d for the machine. As can be seen, the added assumption makes a significant difference to the CSI and hence to the instability point on the MAP characteristic. In comparison with a detailed model the curves generated with the $P_{syn} = 0$ summation match the observed response more closely.

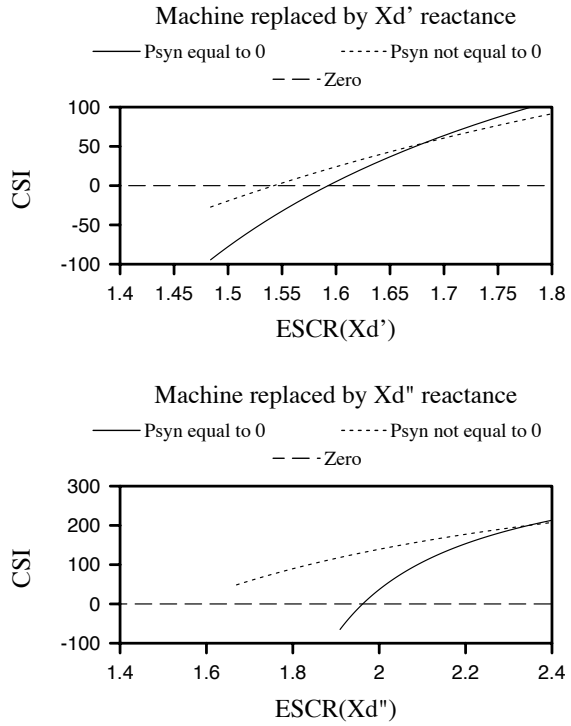

Figure 3.4. CSI_P curves with and without $P_{syn} = 0$ assumption.

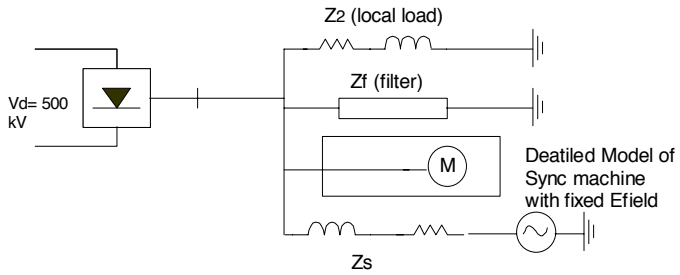

Figure 3.5. Detailed machine model with fixed excitation.

3.2.2 Comparison with a Detailed Machine Model with and without Excitation Control

In this comparison the curves obtained via theoretical calculations were compared with a full electromagnetic transient model of the machine shown in Figure 3.5. As before, the field voltage was assumed fixed, but in the simulation the machine was represented by a two-axis theory based model. The resultant curves are as shown in Figure 3.6. for a typical $ESCR$ of 1.6.

The curves in Figure 3.6 show the DC power and AC bus voltage regulation as a function of the DC current. The analytically calculated curves for two

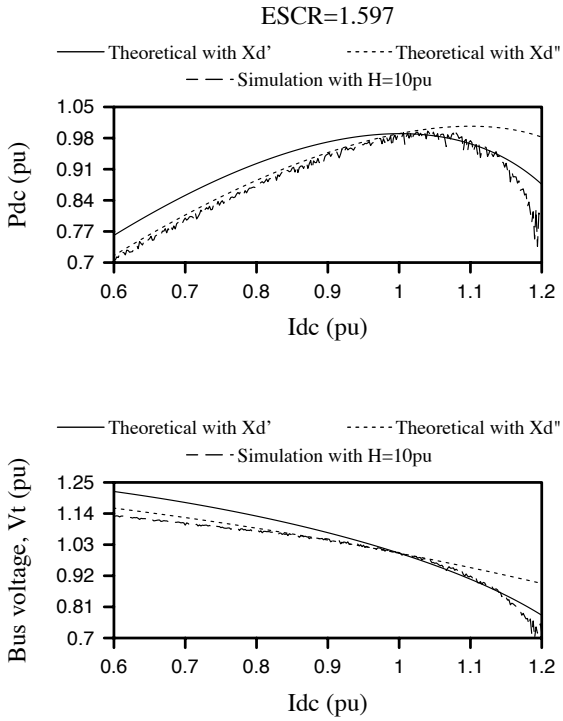

Figure 3.6. Comparison of theoretical MPC and with detailed machine model based simulation (E_{fd} constant).

assumed reactance values (X'_d and X''_d) are superposed on the simulated characteristic. The simulated characteristic (obtained as described in section 3.1) appears to follow the X''_d based analytical result more closely at least at lower DC current levels. After the peak is reached, the simulated curve deviates from the X''_d based characteristic and appears to be closer to the X'_d based characteristic. However it can be seen that the peak of the actual curve is more closely approximated by the X'_d based curve.

The oscillations in the simulated waveform, particularly in the area where MAP is exceeded are due to the electrical and mechanical transients excited in the model by the slow ramp-up procedure.

3.2.3 Inclusion of Controlled Excitation

The impact of modeling excitation controls on the simulated MPC is now presented. The model used in the simulation is as shown in Figure 3.7. A simple Proportional-integral control system was assumed with an exciter ceiling of ± 12 p.u., which is typical for modern fast acting excitation systems.

For such a system, the MPC (a steady state concept), can be derived by assuming the bus voltage of the synchronous compensator to be constant. A properly acting excitation system (droop ignored) would indeed achieve this. With such an assumption, the short circuit capacity of the inverter's AC bus approaches infinity and the bus can be regarded as an infinite bus. The resulting

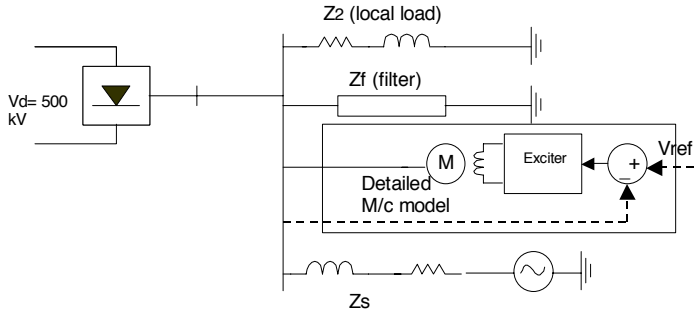

Figure 3.7. Detailed machine model with excitation system included.

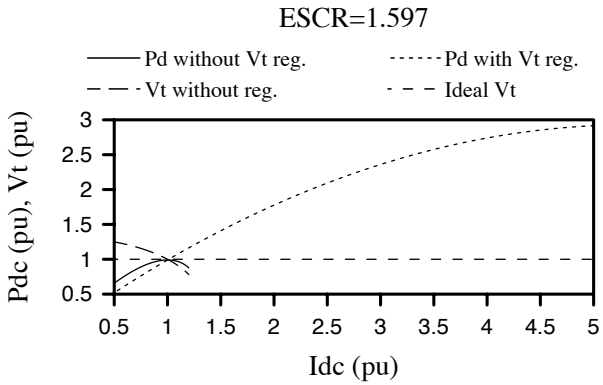

Figure 3.8. MPC and bus voltage characteristics with and without ideal excitation.

MAP now has a very large value and occurs at a very large DC current as shown in Figure 3.8. The MPC and voltage characteristics for the earlier case (as in Figure 3.2) are also superposed for comparison.

However, when a detailed simulation is carried out, this expected result does not occur. The system follows the theoretical curve as seen in Figure 3.9 (solid and dashed traces). Note that only a portion of the x-axis range of Figure 3.8 is plotted. The system becomes unstable at $I_d = 1.08$ p.u. This is due to instability caused by the excitation system dynamics, which were ignored in the theoretical calculation. The exact onset level is also seen to vary depending on the controller gains. This shows that the results obtained from a simple MPC analysis could be excessively optimistic when excitation control is ignored.

If instead of modeling the machine in detail, a simplified exciter-machine model as shown in Figure 3.10 is used, the results are in agreement with the curve derived in Figure 3.8. In this approach the exciter-machine system is modeled as a Proportional-Integral controller whose output is the Thevenin voltage behind the machine impedance X'_d. The resulting curves are shown as the dotted lines in Figure 3.9. In this case the instability does not occur as in the detailed model, but the curve flattens out after a current of 1.1 p.u. is reached due to the attainment of a limit in the DC current controller. This

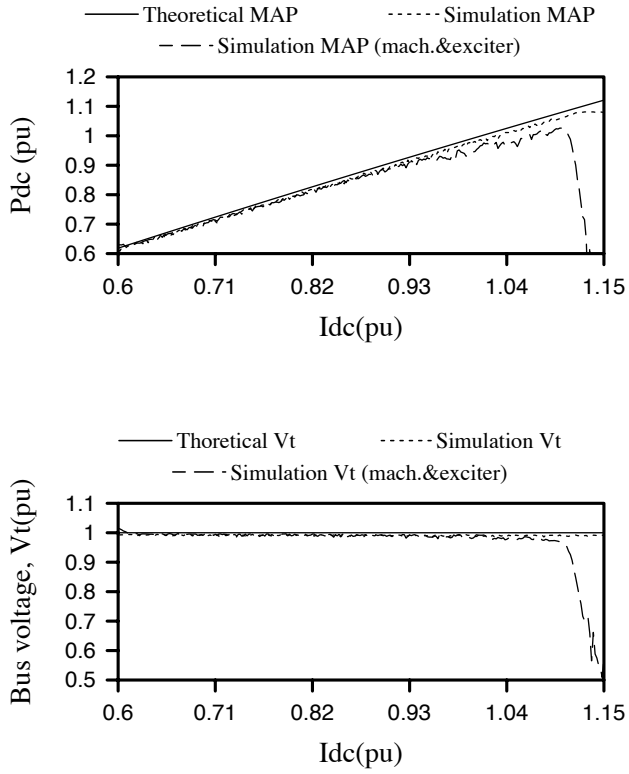

Figure 3.9. Theoretical and simulated MPC with excitation controls.

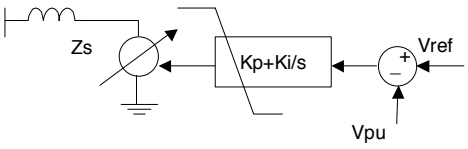

Figure 3.10. Simplified machine-exciter model.

proves that the instability observed with the detailed machine model is indeed due to dynamics which are ignored in the theoretical calculation of MPC.

3.3 Conclusions

The following observations can be made based on the above results:

- The MPC characteristic agrees with detailed transient simulation when machine dynamics are not modeled.
- When the Synchronous Compensator is included but the exciter dynamics are ignored, the theoretically obtained graphs (with X'_d or X''_d for the

impedance) do not follow the simulated MPC over the entire range. However, a reasonable figure for the MAP can be arrived at using X'_d in the theoretical derivation.

- When Modelling Synchronous Compensators in MPC analysis, the additional condition of $P = 0$ gives more accurate results.
- Inclusion of an exciter results in an actual response that tracks the MAP result, but only up to a point. The margin of stability is not improved.

3.4 Appendix: Equations used in MPC Calculations

With Simple A.C. Thevenin Equivalent Source

$$U_t = \frac{\sqrt{2}X_c I_d}{\tau(\cos\alpha + \cos\gamma)} \tag{3.1}$$

$$\cos\phi = \frac{\cos\gamma - \cos\alpha}{2} \tag{3.2}$$

$$U_d = \frac{3\sqrt{2}}{\pi}\tau U_t \cos\gamma - \frac{3}{\pi}X_c I_d \tag{3.3}$$

$$P_d = I_d U_d \tag{3.4}$$

$$\overline{E}_{sys} = U_t - \frac{Z_s j X'_d}{Z_s + jX'_d}\Big(\frac{P_d e^{j\phi}}{U_t\cos\phi} - \frac{U_t}{Z_f} - \frac{U_t}{Z_{ll}}\Big) \tag{3.5}$$

With Constraint on Real Power into Synchronous Compensator Eqs. (3.1) - (3.4) are used together with a modified equation 5 as shown below and an additional constraint equation

$$\overline{E}_{sys} = U_t - Z_s\Big(\frac{P_d e^{j\phi}}{U_t\cos\alpha} - \frac{U_t}{Z_f} - \frac{U_t}{Z_{ll}} - j\frac{Q_{syn}}{U_t}\Big) \tag{3.6}$$

$$Q_{syn} = \sqrt{3}U_t\Big(\frac{E_f\cos\delta - U_t}{X'_d}\Big) \tag{3.7}$$

The variables used in the above equations are thus defined:

U_t : Line to line voltage on commutating AC busbar (kV)

X_c: Commutating impedance (Ω)

U_d, I_d, P_d: DC voltage (kV), DC current (kA) and DC power (MW)

τ: Transformer turns ratio (converter side: ac network side)

α : Delay angle of inverter (deg)

γ : Extinction angle of converter (deg)

ϕ : Power factor angle of converter (deg)

Z_f : Complex impedance of AC filters

Z_{ll} : Complex impedance of local load

E_{sys}, Z_s: Thevenin equivalent voltage (kV) and impedance (Ω) of AC network

δ: Angle of synchronous machine equivalent, with respect to the commutating AC busbar voltage (deg)

Q_{syn}: Reactive power from synchronous compensator (positive for capacitive operation) (Mvar)

E_f: Voltage behind synchronous impedance (proportional to excitation voltage) (kV)

X'_d, X''_d: Transient and subtransient impedances of synchronous compensator (p.u.)

4
Influence of System Operating Conditions and Converter Design

It is common to assess the AC/DC interconnection by a *Short Circuit Ratio* (SCR) or by an *Effective Short Circuit Ratio* ($ESCR$) where the AC system is represented by a Thevenin equivalent voltage source of fundamental frequency behind an equivalent impedance, refs. [4] and [20]. However, the term SCR being useful in preliminary planning, does not account for location of loads. Similarly, the concept of *Maximum Available Power* (MAP), as characterized by Maximum Power Curves, MPCs, is influenced by load characteristics as well as operational tap-changing strategies and interaction between the rectifier and inverter AC buses via parallel AC path [21].

The MAP concept and its quantification have been largely based on the established technology of naturally commutated converters. The different reactive power behavior of emerging voltage-sourced converters and capacitor-commutated converters has a corresponding influence on the MPC and the AC voltage profiles as DC power is varied.

4.1 Effect of Load Modeling on the MAP and AC Voltage

The change in the DC current influences the AC system voltages and consequently the load voltages. In [9], the authors have investigated the influence of the load model on the MPC for a modified version of Test System T-2 in [22], see Figure 4.1. The Test System is modified such that values of $ESCR$ on the inverter side of 2.60 and 1.26 have been achieved.

For the first case, an $ESCR$ of 2.60 produces a nominal operation below MAP. The load flow program at a nominal operating point determines the converter transformer which are kept constant for operation different from nominal. With constant current control at the rectifier and minimum γ at the inverter, the DC current order is increased from zero to the point where the load flow fails to converge. The MPC are obtained by repetitive runs of the EPRI IPFLOW 2.1 load flow using the procedure described above and for different load models:

1. Test System without the inclusion of load models and with voltage sources generating and absorbing the transmitted power for validation with a Thevenin source AC model used in basic SCR ($ESCR$) calculation;

2. Constant PQ load model, as often used in steady state analyses but assumed to be overly pessimistic in voltage stability studies;

3. Impedance load model which is sensitive to changes in the AC voltage magnitude and consequently to the changes in DC current order;

4. Voltage dependent load as found appropriate in voltage stability studies; a polynomial load model has been used:

$$P_L = P_n(0.83U^0 - 0.30U^1 + 0.47U^2) \tag{4.1}$$

$$Q_L = Q_n(6.70U^0 - 15.3U^1 + 9.60U^2) \tag{4.2}$$

The approach has been to normalize the loads to provide the same P and Q at the nominal operating point of the DC system while permitting the interaction away from nominal to respond to above mentioned load models. The curves in Figure 4.2 indicate that MAP and I_{MAP} are sensitive to the assumption of load model and the operation above rated DC current shows a spread in the MPCs.

For the Test System of $ESCR$ of 1.26, the $ESCR$ is less than the critical value for which nominal operation coincides with maximum power. Figure 4.3 shows the MPCs for different load models, provided that the nominal operating point for all load models used is the same.

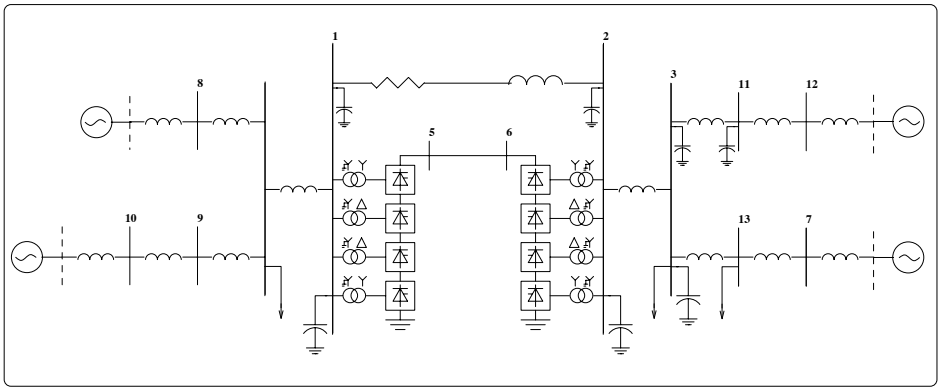

Figure 4.1. Test System T-2 [22].

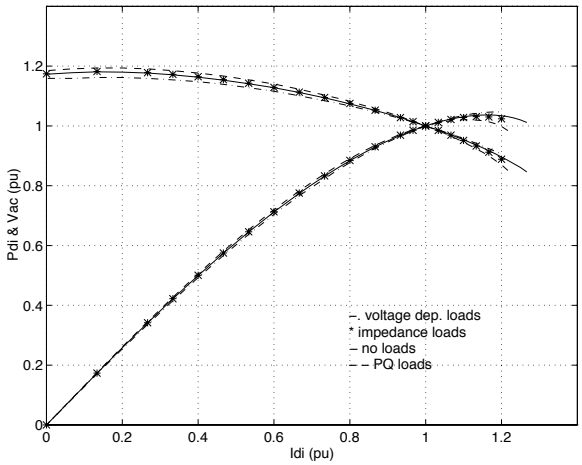

Figure 4.2. MPC sensitivity to load model ($ESCR = 2.60$) [9].

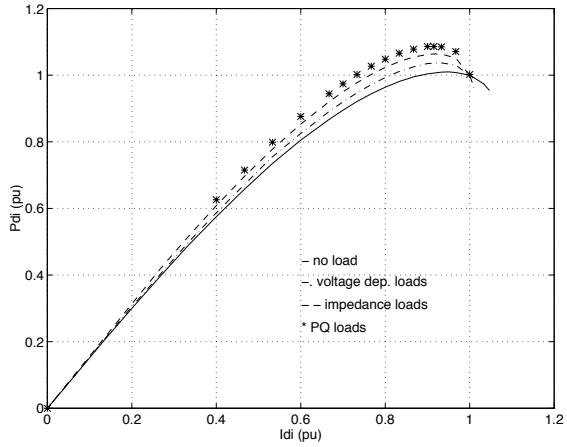

Figure 4.3. MPC sensitivity to load model ($ESCR = 1.26$) [9].

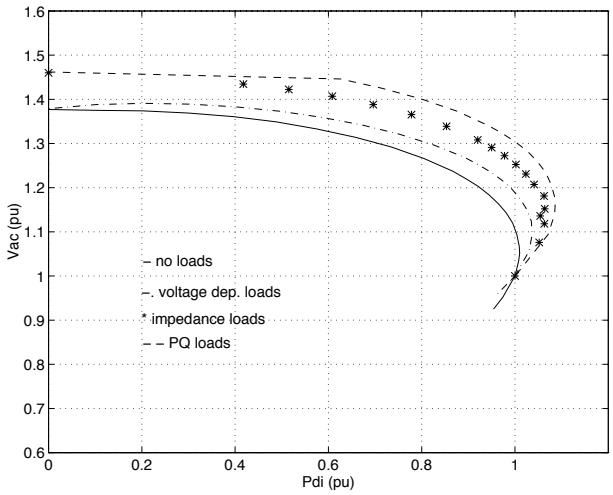

Figure 4.4. Voltage variations for different load models (ESCR=1.26) [9].

The discrepancies between the curves become more marked as the $ESCR$ of the inverter is reduced, as shown in Figure 4.3. A comparison of Figure 4.2 and Figure 4.3 suggests that load representation is not a critical need in high SCR situations but is progressively significant as the SCR reduces.

With constant current control rather than constant power control at the rectifier, the load flow was able to converge in all four cases for a current larger than and a common nominal operating point above was achievable. It is notable from Figure 4.3 that the maximum available powers for the PQ and voltage-dependent loads of 1.086 and 1.037, respectively, are higher than for the case with no load included when the MAP was 1.01.

The four curves in Figure 4.4, so-called nose curves as commonly referred to in voltage stability studies, show AC voltage variations at the inverter AC bus for

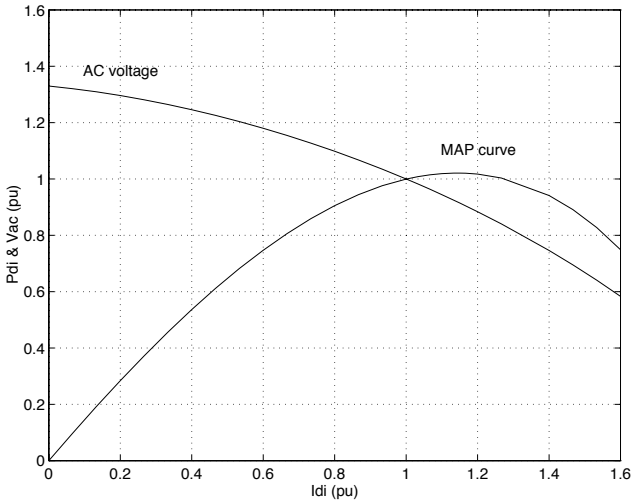

Figure 4.5. MPC and AC voltage for test system with no parallel AC line (ESCR=1.69) [9].

different DC powers. The turning point between stable and unstable operation (between $dU_{ac}/dP_d \leq 0$ on the upper branch and $dU_{ac}/dP_d \geq 0$ on the lower branch) corresponds to the different MAP values in Figure 4.3. The spread between AC voltages is particularly noticeable below the nominal operating point of 1.0 pu for DC current and power. This suggests that provisions for voltage control during start up, and scheduled changes in DC power, need to take into consideration different load models in assessing stability issues.

4.2 Effect of a Parallel AC Line

When the parallel AC line is removed from the test system the calculated $ESCR$ at the inverter decreases from 2.60 to 1.69, due to the reduced short-circuit level. Note that the required shunt compensation is correspondingly reduced; a new AC/DC load flow was run to provide nominal AC and DC conditions. The MPC and AC voltage profile at the inverter bus, with a PQ load model, are shown in Figure 4.5. Compared with the equivalent curve in Figure 4.2, it has the same maximum power of 1.21 pu, contrary to usual expectations, at a DC current of 1.15 pu compared to 1.11 in Figure 4.5. This also indicates that the apparent strengthening of the inverter AC bus by the parallel AC line does not produce a correspondingly increased MAP. This is due to the complex reactive power interactions of the rectifier and inverter AC buses via the AC line as the DC power is varied. The reduced need for capacitive compensation at the inverter bus, when the AC line is disconnected, is also a contributing factor.

The SCR and $ESCR$ values do not characterize any specific AC coupling between the rectifier and the inverter and therefore are not sensitive to the AC configuration nor to any changes. Consequently, other than for very preliminary analysis, it would be prudent to incorporate as much actual system representation, as is known, in planning studies relaying a MAP concept.

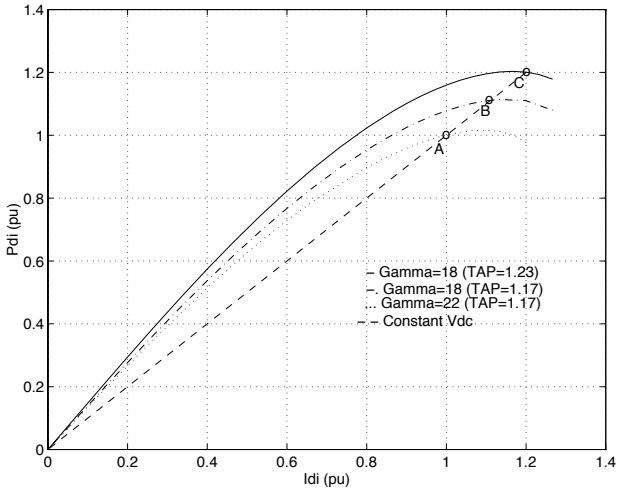

Figure 4.6. Effect of tap changing on power transfer [9].

4.3 Effect of Tap Changing

The three curves in Figure 4.6 illustrate the increase in MAP as a result of operating at a reduced minimum extinction angle (22° to 18°) and also as a result of tap changing. The straight line of inverter control to maintain constant DC voltage has its nominal operating point at A for $\gamma = 22°$. As DC current increases, the margin of voltage control reaches the $\gamma = 18°$ limit at B with a tap of 1.17. Tap changing to 1.23 permits the control margin to be restored (by efficiently switching the MPC) until, with a further increase in DC current, a new limit of minimum γ is reached at C.

The transition A-B-C permits DC power to increase while the three selected operating points are progressively below and above the respective prevailing MPCs. Since such an operating mode is typical of low SCR situations, the consequences of tap changing need to be included in performance evaluation.

The enhancement of MAP by tap changing, under operational conditions, would apply to slowly changing system conditions within the time-response capabilities of the tap-changing mechanism. This would be typical of the response to load changes, as opposed to abrupt changes such as line switching.

The corresponding voltage profiles at the inverter AC bus are shown in Figure 4.7. Tap changing permits DC voltage control (and hence power control in conjunction with rectifier DC current control) to be extended to increase power by 20%. At this limit, increasing DC current reduced DC power as the AC voltage starts to collapse.

4.4 MPC for Capacitor Commutated Converters

The MPCs presented so far have all assumed that the converters are line commutated (LCC). Recently Capacitor Commutated Converters (CCC) of current source type have been put into operation, see refs. [23] and [24], which have

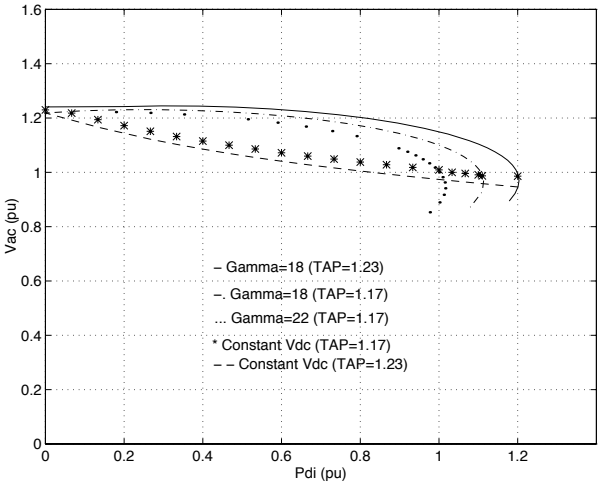

Figure 4.7. AC voltage against DC power with tap changing [9].

Type	SCR	Q_c (p.u.)	U_{TOV} (p.u.)	Figure
CCC	2.0	0.13	1.07	4.8
LCC	2.0	0.50	1.27	4.9
CCC	0.93	0.13	1.71	4.10
LCC	0.93	0.50	3.18	4.11

Table 4.1. Data and for the systems which MPCs are given in Figures 4.8 to 4.11. It should be noted that the U_{TOV} values given refer to complete load rejection without taking any non-linear effects, e.g. transformer saturation and arrester action, into account.

drastically better properties when it comes to voltage and power stability as will be shown in this section.

MPCs for cases with data according to Tabel 4.1 are shown in Figures 4.8 to 4.11. From these it is clearly seen that CCC exhibits superior performance.

4.5 Conclusions

The study has shown the necessity of plotting maximum power curve and obtaining the maximum available power for the particular AC/DC system and particular control mode at the inverter. It has also been shown that the basic SCR calculation, while still very helpful in the first stage of design, is insufficient in itself for evaluating the power transfer capability and power stability of the DC system. The presence and characteristics of AC loads as well as the presence of any parallel AC lines influence the maximum available power transfer and make the nose curves more diverse. Furthermore, the power transfer capability is affected by the adopted strategy for tap changing. It was also shown that CCC has superior performance when it comes to voltage and power stability.

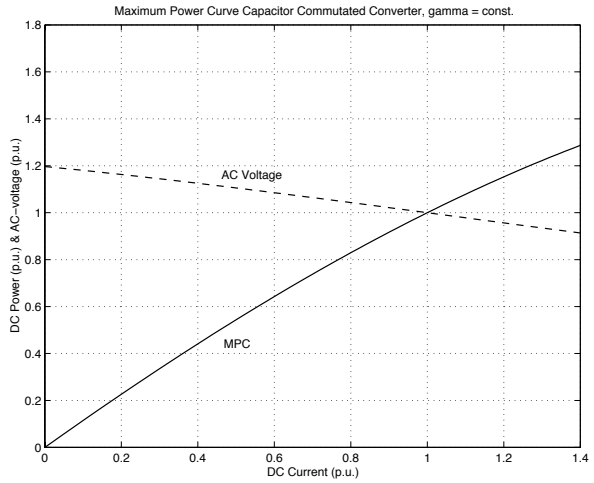

Figure 4.8. Maximum Power Curve (MPC) of a system with CCC and $SCR = 2.0$.

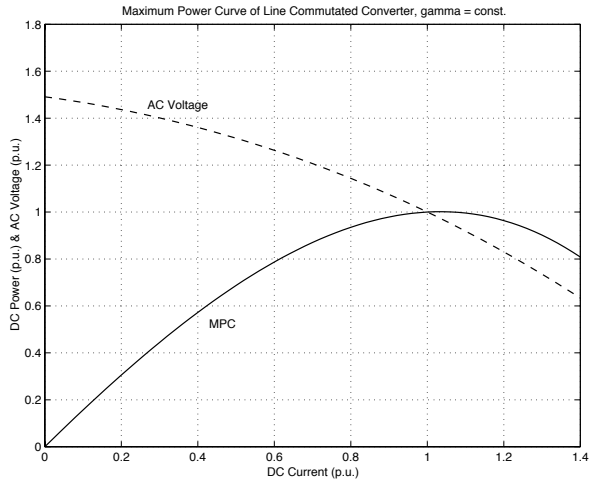

Figure 4.9. Maximum Power Curve (MPC) of a system with LCC and $SCR = 2.0$.

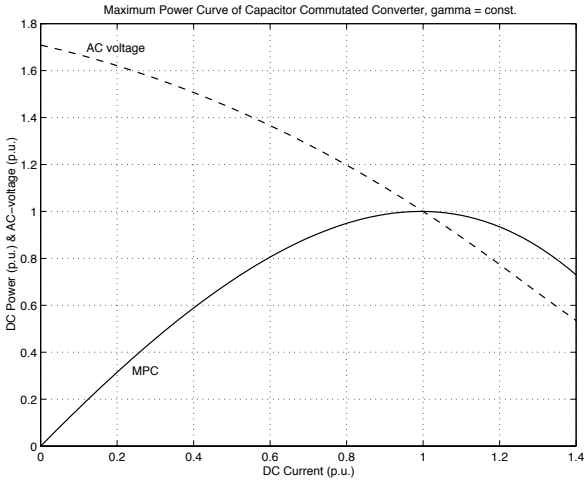

Figure 4.10. Maximum Power Curve (MPC) of a system with CCC and $SCR = 0.93$.

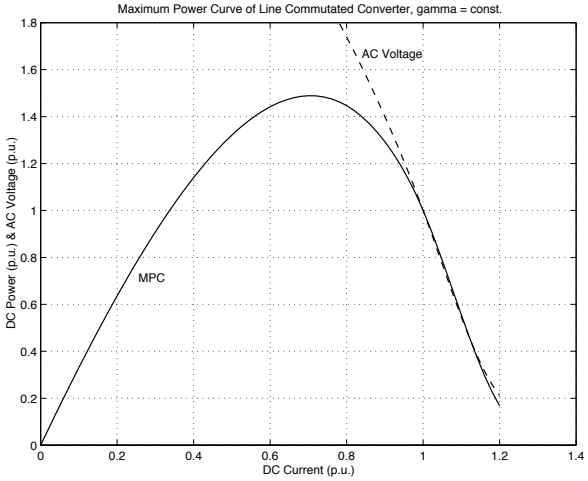

Figure 4.11. Maximum Power Curve (MPC) of a system with LCC and $SCR = 0.93$.

5
Multi-Infeed HVDC Systems

5.1 Development in the Study of Multi-Infeed HVDC Systems

Traditionally, HVDC links are built as point-to-point interconnections or single-infeed HVDC systems as they are commonly known, although other system configurations such as back-to-back, multi-terminal, HVDC links have also been built. When the HVDC link is terminated at an AC system location of low short circuit capacity relative to the power rating of the HVDC link, the AC/DC interconnection is said to be weak. Concomitant problems relating to system stability and performance are typically voltage/power instability, high temporary over-voltages, low frequency resonances and harmonic instabilities, long fault recovery times, and susceptibility to commutation failures [25], [26]. These situations can result in equipment damage or lead to graver scenarios as system collapse. Therefore a fundamental understanding of their nature, developing analytical techniques, and finding countermeasures, are crucial to enable successful planning, design, and operation of power systems exhibiting such problems. A comprehensive and systematic analysis of all important AC/DC interactions for the single-infeed HVDC system is given in [4], while a survey and review of AC/DC interconnections exhibiting such problems are presented in [27], [28].

As the use of HVDC transmission continues to develop, situations will also arise where two or more HVDC converters terminate at AC system locations that are electrically in close proximity, for example a common AC area fed by point-to-point HVDC links. In a general context, these converters in close proximity can be any combination of inverters and rectifiers [29], [30]. Such system configurations are loosely termed as multi-infeed HVDC systems. Situations as these arise particularly in regions where the power systems of neighboring countries are dominantly interconnected by HVDC links. Already such system configurations are emerging or in existence such as those in Scandinavia, Southern California, Manitoba, and Quebec. These system configurations are anticipated to give rise to new phenomena concerning interactions between the constituent HVAC and HVDC systems, especially when one or more of the AC/DC interconnections are relatively weak. Hitherto, due to the recent origin of multi-infeed HVDC systems there has only been rudimentary investigations on the interaction phenomena and potential associated problems. However the reality and practicality of such system configurations have spurred growing interest in this area. As far we are aware, pioneering investigations only began as recent as the works in [29], [30], though some aspects of these system configurations had been investigated in an earlier work [31]. In [29] various categories of multi-infeed HVDC systems were defined followed by a simulator study on a practical system representing one of the categories. The study found intimate interactions between the various constituent systems and control coordination among the constituent HVDC links was particularly important. In [30] an in-

sight into various potential problems arising from multi-infeed HVDC systems was given. These include small-signal instability due to control interactions among the constituent HVDC links, voltage instability and collapse, increased commutation failures in one constituent HVDC link due to AC faults occurring in the vicinity of a neighboring one, transient AC voltage depression due to simultaneous recovery of constituent HVDC links after an AC fault. Similar to [29], control coordination among the constituent HVDC links or modification of the HVDC control modes were identified as potential solutions to overcome the associated problems. In [32] a digital simulator study was performed to investigate the transient response and recovery of multi-infeed HVDC systems based on different control strategies of the constituent HVDC links. Transient recovery of the studied system was found to be highly system dependent although certain control strategies could provide robust system response. In [33] synchronizing and damping torque modulation applied to the controls of constituent HVDC links of a multi-infeed HVDC system were investigated. Cooperative coordination of controls among the constituent HVDC links was shown to provide effective damping and synchronizing torque in a de-coupled manner, to achieve overall system integrity with respect to electromechanical stability.

As seen, a broad spectrum of system phenomena could potentially arise in multi-infeed HVDC systems [29], [30], [32], [33]. Conceivably these system phenomena are related to those arising from single-infeed HVDC systems, since multi-infeed system configurations historically evolved from the latter. Moreover, voltage/power instability problems clearly hold special interest since these had been among the most important technical concerns for single-infeed HVDC systems. In this respect it is appropriate to know how close these system phenomena correspond, under what conditions they differ, and whether the analytical techniques developed for the single-infeed situation could be similarly applied to the multi-infeed case. A host of other fundamental questions arise and there is clearly a need to address them. These questions essentially provide the main motivation for the work in [12] - [17], and [35] - [37]. Specifically these works aim to achieve the following objectives;

- deriving a fundamental understanding of the voltage/power instability and interaction phenomena in multi-infeed HVDC systems.
- developing techniques to analyze them.
- finding viable countermeasures to overcome the associated problems.

5.2 System Models

In the literature, study of multi-infeed HVDC systems have generally used system configurations with two [29], [12], [30], [32], [33] or three [13], [34] point-to-point HVDC links. However, the AC network representation in these system configurations varies considerably in complexity and topology. For example, in [30] the HVDC links are embedded in a very large AC system while in [29] the AC network is a mere 5-bus system interconnected by HVDC links whose remote converter terminals are interconnected by islanded single-bus AC systems. Thus the diversity in system representation offers no ground to abstract a benchmark multi-infeed HVDC system model. Nevertheless, in general a benchmark

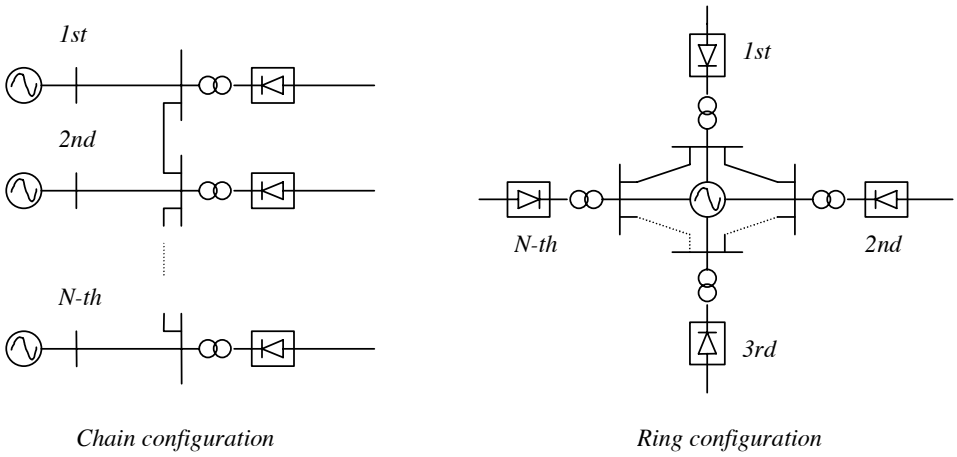

Figure 5.1. Multi-infeed HVDC system configuration constituted by point-to-point HVDC links.

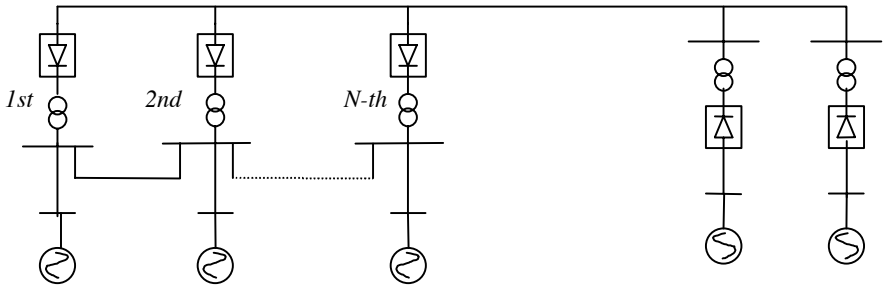

Figure 5.2. Multi-infeed HVDC system configuration constituted by multi-terminal HVDC links.

system model suitable for systematic investigations should have the following characteristics;

- A system topology that derives its roots from the classical single-infeed HVDC system configuration. This strong analogy between the single- and multi-infeed HVDC system configuration is essential to allow analytical comparisons between them.
- A system model that is simple but representative of the multi-infeed HVDC system configuration. This allows simulation studies based on a realistic system model, at the same time theoretical analysis on it can be done without being distracted by intractable mathematical rigour.

These desired characteristics motivated much use of the system configuration as shown in Figure 5.1 for the work in [12] - [17], and [35] - [37]. Figure 5.1 shows two variants of this system configuration, namely the chain and ring multi-infeed HVDC system configuration, but their essential characteristics are

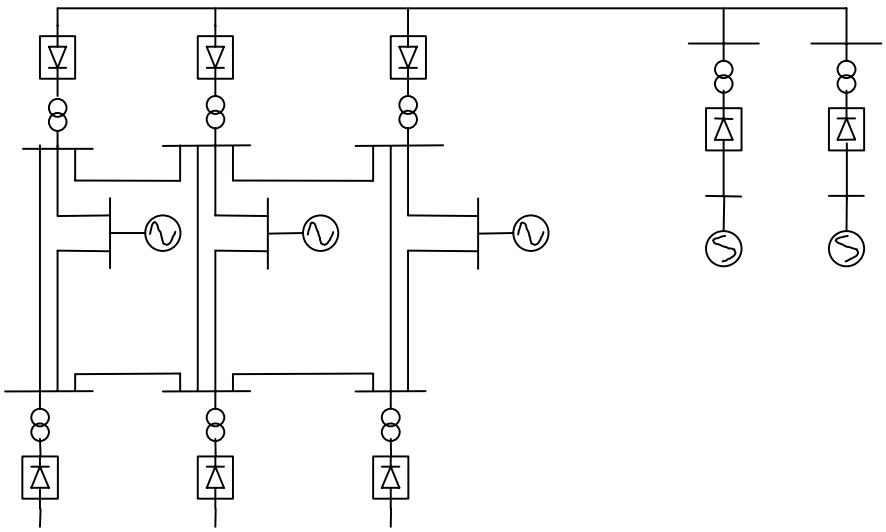

Figure 5.3. Multi-infeed HVDC system configuration constituted by multi-terminal and point-to-point HVDC links.

that they comprise point-to-point HVDC links and all the converters are inverters. This is perceived to be the most common and onerous situation with respect to voltage and power instability. Other system configurations and converter type combinations are of course possible, such as shown in Figure 5.2 where the multi-infeed HVDC system configuration is constituted by multi-terminal HVDC links. Ultimately a most general multi-infeed HVDC system configuration would conceivably be as shown in Figure 5.3, being constituted by point-to-point as well as multi-terminal HVDC links. This system configuration could potentially come about as a result of the Baltic Ring, East-West Europe, and southern Scandinavia HVDC projects.

As for converter type combinations, in general there are a number of possibilities as categorized in [29], described below and schematically shown in Figure 5.4;

- Type 1A: converters of the same type connected to different HVDC systems.
- Type 1B: converters of the same type connected to a common HVDC system.
- Type 2A: converters of mixed type connected to different HVDC systems.

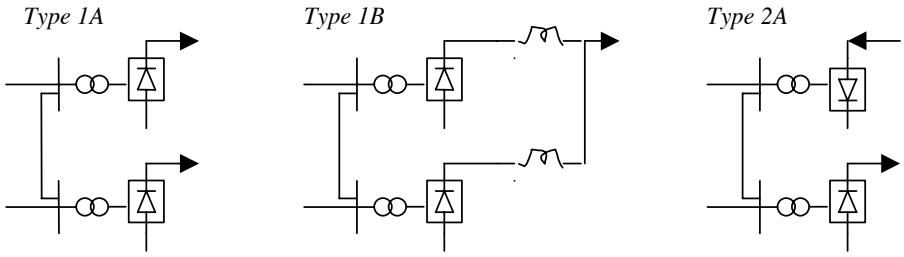

Figure 5.4. Three categories of converter type combinations for multi-infeed HVDC system configurations.

5.3 Analysis of Voltage/Power Stability of Multi-Infeed HVDC Systems

Voltage stability of AC power systems has been studied from static (or quasi-static) and dynamic approaches. Recent works have also treated voltage stability from a nonlinear dynamical system theoretic perspective. Likewise for HVDC systems, voltage and power stability investigations have followed similar approaches but using analysis techniques and concepts that are pertinent to HVDC systems. These approaches and analysis techniques can be organized into a framework as shown in Figure 5.5. The following discussion on past work concerning stability analysis of multi-infeed HVDC systems is with reference to this framework.

Static Approach

Sensitivity Technique The underlying assumption for the static approach to study voltage/power instability in HVDC systems is that the phenomenon occurs so fast that the AC/DC system dynamics do not appreciably affect it. Thus the DC line and converter pole control dynamics, and voltage control dynamics in the AC system are neglected. The stability of the AC/DC system is thus essentially determined by the algebraic system states that govern the power flow in the system, and sensitivity of system states to small changes in controlling system quantities is used as a measure of system stability.

Two main concepts based on the sensitivity technique had been proposed in the past to analyze the voltage/power stability of weak single-infeed HVDC systems. One approach known as the Maximum Power Curve (MPC) method is based on the concept of Maximum Available Power (MAP) and was introduced in [5] and [6]. The other approach, known as the Voltage Stability Factor (VSF) method, is based on the concept of voltage sensitivity and was first presented in [7].

Taking cue from these concepts for the single-infeed HVDC system, they were extended to analyze the voltage and power stability of multi-infeed HVDC systems in [12], [17], [37]. This entails use of the system power flow model and modal analysis technique. Briefly, this mathematical technique decomposes the multi-dimensional AC power flow Jacobian into its modal equivalent. The

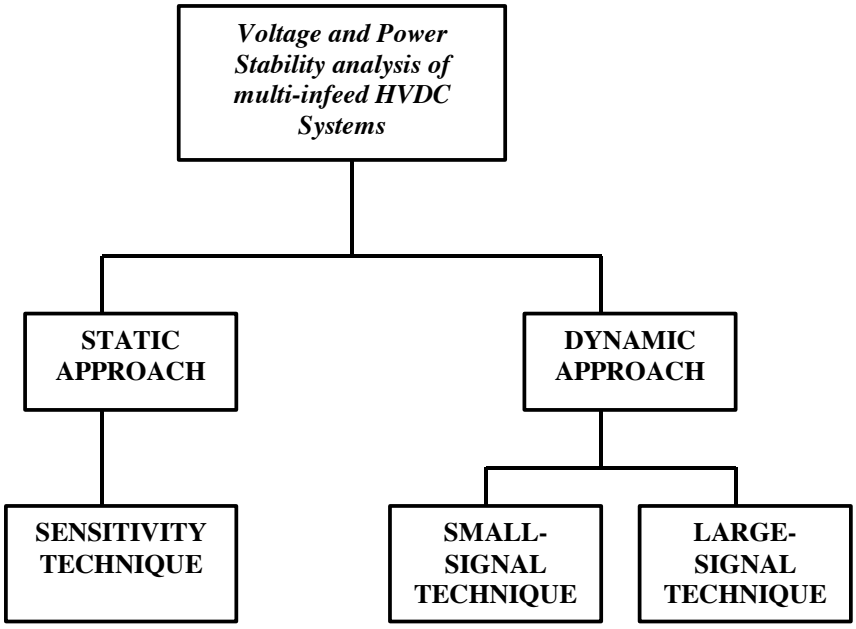

Figure 5.5. Frameworks for voltage and power stability analysis of multi-infeed HVDC systems.

resulting incremental modal voltages thus relate with the modal reactive power injections in a de-coupled form and through an eigenvalue of the corresponding mode. This is intuitively akin to the *VSF* of the single-infeed case and can be interpreted as the modal voltage sensitivity factor *MVSF* for the multi-infeed HVDC system.

Based on the above technique, a general and comprehensive method for voltage stability analysis of multi-infeed HVDC systems was developed in [12], [17], [37]. The technique was further developed in [13] through use of participation factors of the critical modes to determine the critical system location in a multi-infeed HVDC system where the most severe system phenomena are expected to occur, and for evaluating the effectiveness of remedial actions implemented.

Similarly the modal analysis technique incorporating the concept of maximum available power was proposed in [12] to investigate the power stability of multi-infeed HVDC systems. It was shown in [12], [17] that the DC power flow Jacobian could be decomposed into its modal equivalent and the resulting incremental modal DC power and modal DC currents are related in a manner similar to that for the single-infeed case. A limiting condition, akin to the Maximum Available Power (*MAP*) condition for the single-infeed case, is also reached when the eigenvalue of the corresponding mode vanishes. Thus the concept of Modal Maximum Available Power (*MMAP*) for multi-infeed HVDC systems could be similarly proposed.

Similar to the relationship between the power and voltage analysis methods for the single-infeed case shown in [10], such relationships were also shown in [12], [17] to exist for the multi-infeed HVDC case. It was also shown in [12], [17] the inter-relationship between the methods for the single-infeed and multi-

infeed HVDC systems. From such relationship structure it was established that the modal power/voltage analysis methods for multi-infeed HVDC systems are the multi-dimensional equivalent of the corresponding ones for the single-infeed case. In [16] it was further shown that these relationships are preserved when load models are incorporated into the system models.

In [9] the influence of static load characteristics on the MPC was shown for a HVDC link with a parallel AC line interconnection. Similar to this, the influence of static load characteristics on the voltage/power stability of multi-infeed HVDC systems was shown in [15], [16], [17]. In [15], [16], [17] the basic voltage and power stability equations incorporating static load characteristics were derived and used to show the effect of load and system parameters on the voltage/power stability margins of multi-infeed HVDC systems. Conditions for ascertaining the most unfavorable static load characteristics with respect to degrading the voltage and power stability margins were derived in [16]. Indices to characterize and estimate a bound for the effect of static load characteristics on the system stability margins were also defined and studied in [16].

Dynamic Approach

The dynamic approach to voltage and power stability analysis of HVDC systems considers the full or at least the most essential dynamics of the system. The AC/DC system is thus represented by a nonlinear differential-algebraic system model and solution techniques are applied according to the problem of interest, that is whether the instability problem is due to a large or small-signal system disturbance.

Small-Signal Technique For small-signal considerations, the differential-algebraic system model may be linearized, the algebraic states eliminated, resulting in a small-signal differential system model. This technique has been applied to HVDC systems to study the dynamic stability with respect to electromechanical [38], [39] and DC control loop induced oscillations [40]. It was in [30] that this technique was first applied to investigate electromechanical oscillations in a large AC system with multiple HVDC links. In [33] synchronizing and damping torque modulation applied to the controls of constituent HVDC links of a multi-infeed HVDC system similar to the one used in [30] were investigated. Cooperative coordination of controls among the constituent HVDC links was shown to provide effective damping and synchronizing torque in a de-coupled manner, to achieve overall system integrity with respect to electromechanical stability. It was in [30] and [33] that a controllability table, defined as the ranked normalized frequency response of the transfer function between the modulating and rotor speed signals, was derived. It was shown how the controllability table could provide reliable information regarding how and where the DC link modulation is most effective in a multi-infeed HVDC system to damp the troublesome oscillatory modes.

Another aspect of small-signal technique applied to HVDC systems is the study of non-linear phenomena associated power/voltage instability. This was first briefly investigated in [41] for the single-infeed HVDC system. It was in [17], [36] that a fundamental and comprehensive study of nonlinear phenomena in HVDC systems was embarked upon. In these works, two principal voltage collapse mechanisms in HVDC systems arising from nonlinear phenomena,

namely the saddle-node and Hopf bifurcation, were studied for the single-infeed and multi-infeed HVDC systems. It was also shown in [17], [36] that the quasi-static and dynamic conditions for voltage collapse considered via saddle-node bifurcation in the HVDC system models considered were equivalent.

Large-Signal Technique Another important aspect of system phenomena in multi-infeed HVDC systems is the transient or large-disturbance system behavior pertaining to system recovery and collapse. Past work performed in this respect can be found in [26] for the single-infeed HVDC and [29], [30] for the multi-infeed HVDC case. For this type of problems, the common investigation technique is to use nonlinear time-domain simulation using an electromagnetic transients program [29], [30].

6
Planning and Analysis of Systems - Principles and Concepts

6.1 Background

In the actual application and installation of HVDC schemes in the last few years, there is an impression that not so much attention has been paid to the power/voltage stability phenomenon. This is probably because most, if not all, recent HVDC schemes have been applied into systems where the inverter AC system is relatively strong, that is, with a high Equivalent Short Circuit Ratio (*ESCR*). In these cases, it is unlikely that power instability would be a problem unless unusual operating conditions were imposed. However, this phenomenon is still very real and a major issue whenever a conventional, line-commutated thyristor-controlled HVDC inverter is applied into an AC system with a low *ESCR*.

In the past, a number of DC schemes experienced the full effects of this power instability, including in some cases the resulting consequences of system collapse. In these systems, the problem has been mitigated by invoking special supplementary controls on the DC or by a combination of controls and special compensation considerations [4], [42], [43].

In recent years, new developments in HVDC technology provide the potential to significantly reduce any manifestation of the power stability problem in most systems. Developments such as capacitive-commutated converters (CCC) and voltage-source inverters (VSI) now make it theoretically possible to apply DC links into much weaker AC systems without these problems. Both the controls and the parameters incorporated into these new technologies are such that they present positive impacts towards the prevention or mitigation of instability. The application development of these technologies is still progressing and a full treatment of their theory, operation and system effects are beyond the scope of this document. However, it is important to note that in these cases the basic principles of the stability phenomenon do not change. But the modes of operation and limits of DC application can change.

6.2 Simplified Explanation of Power/Voltage Instability Phenomenon[1]

A power/voltage instability in a conventional, line-commutated HVDC system can basically arise out of an inter-relationship between the AC voltage, DC controls and the DC current. It manifests itself mainly in "weak" AC systems because it depends almost entirely on the "stiffness" of the AC voltage. In simple

[1]This section is identical with section 1.2, but since it is essential for the subsequent discussion in this chapter it is repeated in full here.

terms, the basic mechanism of the instability occurs as follows: Suppose the AC voltage drops just a small amount; then the DC voltage at the inverter drops proportionately (they are directly related). But the main function of the DC controls in many DC schemes is to hold constant power order ($P_d = U_d \cdot I_d$). If the DC voltage (U_d) goes down, the only way the controls can maintain constant power is to increase the DC current (I_d). However, as soon as it does this, the reactive power consumption of the DC increases because this is directly related to the DC current. Unless the additional reactive power is immediately (very important - this will be explained later) available, the AC voltage will dip further and start the cycle all over again. In other words, an unstable cycle will be started and perpetuated which, unless it is stopped in some way, can lead to a runaway condition and a total collapse of the entire AC/DC system.

6.3 "Weak-Connection" Versus "Weak-System" In-Feed of a DC Link

Interaction phenomena between AC and DC systems are usually discussed in the context of weak systems in general, without qualifications about the topology of the AC system. That is, a weak system is any system that results in a low *ESCR* connection of a DC converter.

At this time, it is of great clarifying value to introduce a new definition for the concept of a "weak-connection" of a DC converter, to differentiate from weak systems in general for AC/DC interaction phenomena, but particularly for the DC power stability phenomenon.

A weak system or low *ESCR* connection of a DC converter can result from a number of topological circumstances. One case, which is generally considered the classic case within this topic, is where the DC power in-feed is large compared to the strength of the entire composite AC system. A sub-case of this is where the large DC power is from multiple DC in-feeds. This classic case is the one most likely to require the need for converters in power control (or system frequency or damping control) and for the inverter in minimum extinction angle control as dictated by the DC design and operating economics. Therefore, most of the stability principles discussed herein apply to the greatest extent to this topological case.

It is quite feasible, however, to have a low *ESCR* connection of a DC converter to an otherwise large or 'strong' AC system. This condition will be defined as the weak-connection case. A number of existing HVDC schemes are like this. The usual circumstance will be when a relatively low power DC link, often a back-to-back link, is connected to a particularly weak part of the AC network. This could result, for example, if the converter is connected to only one or two long, radial AC lines, electrically remote from the strong part of the main network. For low power weak-connection cases, it may be technically and economically feasible to avoid power stability problems by employing controls other than constant power, such as constant current, and by utilizing extinction angles higher than minimum with the inverter in voltage control, for example.

6.4 Important Parameters of the System

The reason that the unstable mechanism described above manifests itself predominantly in weak AC systems can be explained by the following concept:

The amount of power that can be delivered into an AC system from a DC link is mainly dependent on the reactive supply to the inverters and on the AC voltage at the inverter commutating bus. When a converter is connected to a weak system, increasing DC power will tend to lower the AC bus voltage dependent on the ability of the system and connected elements to supply the rising reactive power requirements of the valves. As the DC current is increased, the DC power will also increase until a point is reached when the rising reactive consumption begins to lower the AC voltage, and therefore the DC voltage, at a faster rate than the increase in current. The result is that any further increase in current will actually lead to a decrease in DC power, giving the instability.

This instability with DC is similar to the voltage instability or voltage collapse mechanisms that occur in pure AC transmission networks. The instability involves all quantities when it occurs, including power, DC current, DC voltage, firing angles and AC voltages. The dominant feature of the instability, however, from the system point of view, is voltage collapse at the inverter. It is therefore often called voltage instability, similar to instability in AC systems. However, in DC, the current can be absolutely controlled, even if the AC voltage is not controlled or maintained. If the current ordered is too high for the system to support, then falling AC voltage will result in reduced power, but the system can still operate without runaway and it can be temporarily stable but unsatisfactory. If, on the other hand, the DC is operating in power control and with a power order too high, then the falling DC power results in increasing current order. This in turn then decreases the AC voltage, through larger reactive consumption, to such an extent that it leads to a runaway and unstable condition. Since the instability is thereby caused by a power closed loop control, it can be viewed as a power instability from the DC point-of-view and a voltage instability from the AC point-of-view. If operation in a particular system happens to be near the critical point of instability, then small changes in the system conditions can produce large voltage changes and possible oscillations.

It should be noted that the DC power instability, in its most simple theoretical form, is mathematically at zero frequency and in this form it is not dependent on the response time of the DC line or the controls. The general conditions of occurrence of this instability are then normally as follows:

1. The DC is in power control or, similarly, in frequency or system damping control, where the power order could be in excess of a critical value. Even for a previously safe power level, this same power could become critical for a sudden reduction of the AC system strength or AC voltage, due to line switch-out or capacitor switch-out, respectively, for example, if adequate margin to instability is not provided to account for such perturbations.

2. The inverter is in constant (minimum) extinction angle (gamma) control, implying increased reactive consumption with increasing current.

3. The equivalent short circuit ratio (*ESCR*) (per unit admittance of AC system plus filters, capacitors and compensators on DC power base, see section 2.8) must be less than a certain critical value, assuming that the AC

> system stays constant; that is, before any dynamic compensation or voltage regulators have a chance to respond. From the AC system viewpoint, the critical value of *ESCR* and hence the maximum available DC power should then be dependent on the Thevenin voltage behind reactance and the equivalent system reactance in the classical case of AC system steady state stability. Real systems, however, do not act as fixed Thevenin equivalents over long times beyond a few hundred milliseconds. The Thevenin voltage in this case is not fixed. The general effect can be instability occurring in the form of relaxation oscillations at a low frequency, generally less than 5 Hz, depending on the response lags of machine voltage regulators correcting AC voltages, and on communication and master control lags in the DC The criterion for stability, however, will be practically the same as for a fixed Thevenin equivalent. If the DC control is for constant frequency, then the relaxation oscillation frequency will be lower because of system inertia effects, but the stability criterion will again be similar.

The criteria for power/voltage instability addressed above does not say anything about electro-mechanical stability because reactive power flow is the critical quantity, while in electro-mechanical stability, phase-angle shifts and frequency are predominately governed by active power flow. In addition, it is only valid for fundamental frequency. Steady state stability of the AC voltage is a prerequisite for normal system operation. However, the problem can become worse if the AC system is weak in the inertia sense, that is, if the total system inertia constant is so low as to cause substantial frequency drop during a fault or other event.

In other chapters, it is explained that for a given system with a finite impedance, expressed in terms of the *ESCR*, there is theoretically a maximum-available-power (*MAP*) that is allowable from DC for stable operation. Assuming static conditions in an AC/DC system, a general equation can be derived that gives the *MAP* level. As a corollary, if the maximum DC power is given, the equation can give the minimum strength (highest equivalent impedance or minimum *ESCR*) AC system required to support such a DC power level. Such equations are given and explained in subsection 2.2.1 and references [4], [44], [45].

The theoretical *MAP*, again in the simplest form, assumes a completely static system devoid of any dynamic voltage control. This *MAP* level can be visualized as a 'snapshot' of the system with everything temporarily fixed in time and condition, or as the maximum steady-state operating point of that system with no dynamics existing to improve upon it. As long as it is kept in mind that *MAP* is just one point in a dynamic system, then knowing this *MAP* level can provide valuable insight for planning the system and to determine what requirements there may be for satisfactory operation.

With everything fixed in time and condition (including controls), any attempt to operate that fixed system above its *MAP*, or, conversely, any attempt to weaken the system when it is operating at its *MAP*, implicitly implies the onset of voltage collapse in that system. The effects that the real, non-fixed, system controls have on stability will be treated in subsequent sections below.

6.5 Relationship Between DC Stability and Recovery from AC Faults

Before discussing the effects of dynamic voltage controls, another very important fundamental concept should be reviewed. In the planning of systems, the frequency of faults in the interconnected AC network and their overall effects on system design and performance usually results in these faults being one of the central topics in system studies.

In various studies on DC links, a general conception is often conveyed that if a DC link can recover satisfactorily from the worst-case AC faults, then it can be assumed to be stable for all conditions. This can be very misleading.

From the equations referenced above, it can be shown that the minimum strength system, expressed as the critical *ESCR*, required for power/voltage stability will typically be in the order of about 1.5 to 2.0, depending on the various values of the dc system parameters used in the equations. However, it is known in the industry that DC controls and control strategies can be designed to allow DC schemes to recover from AC faults in systems with *ESCR*s as low as l.0. This is even without any dynamic voltage assistance from compensation devices. The point here is not to discuss how this is done, but merely to point out that this is another domain of the controls, quite separate from the power/voltage stability and associated critical *ESC*R that is being addressed here.

The purpose of a fault recovery strategy is to limit the AC power being injected into the AC system so that at each instant of time, AC voltage and DC power are increasing toward normal steady-state values. The fault recovery strategy and corresponding response may in some cases share some phenomena with true power/voltage instability, but generally they cannot be considered as the same. If a particular system is stable in the steady state, then a fault recovery strategy can generally be devised to allow the DC link and AC system to recover to that steady state.

It follows that when studies on a particular AC/DC system conclude that it requires a certain *ESCR* to recover, all that is being done is to make a statement about a specific set of circumstances in that specific system. But this specific conclusion bears no direct relevance or does not prove anything about the critical *ESCR* associated with *MAP* and DC stability. The later is a true generalized theory of DC with only a few basic parameters identified. Therefore, the recovery from AC faults is generally out of context in this topic. From the theory and equations referenced above, there is only one steady-state critical *ESCR* (or *MAP*) for a given DC system. The only way it can be changed is to change a basic parameter contained within the confines of the classical DC theory equations. Note that the DC system is emphasized because the AC system and its possible topology and components does not even enter into the equation. The definition is from the DC side, not the AC side.

6.6 Effect of "Quasi-Static" Controls on Stability

Notwithstanding that the voltage collapse at an AC/DC interface is fundamentally similar to the classic voltage collapse in an AC system, there are some important related control aspects to consider in recognizing the system dynamics when a DC link is involved.

In this context, it is useful to first differentiate what can be called "quasi-static" controls from continuous, fast acting, dynamic voltage controls that may be associated with nearby reactive power compensation devices or with the DC itself. These will be dealt with later.

With respect to the normal DC controls, if the DC link is in constant minimum extinction angle control and constant power control, the onset of voltage collapse just beyond the *MAP* level will result in an unstable rundown of the AC voltage and DC power. This is, of course, assuming that no other dynamics enters into the picture. The DC constant power controller, in attempting to compensate for the collapsing AC/DC voltage, increases the DC current, which further aggravates the AC voltage drawdown. A total rundown can be prevented, in theory, by reverting to constant DC current control, similar to a control that may be employed in a weak-connection converter. This is effectively equivalent to forcing the DC to operate on a single, stable operating point on a different maximum power curve (MPC). But if the constant-current level corresponds to a power level more than the original system *MAP*, a stable operating point may be temporarily reached with the AC voltage unsatisfactorily low. If the DC uses some control other than constant power (with minimum extinction angle) in normal operation, it is sometimes argued that such a link is more stable than one controlling power. However, unless a DC link has a deliberate over-design that is never to be used, which would usually only be economic for low-power weak-connection cases, the maximum power that can be obtained from the DC occurs at the minimum extinction angle at full rated DC current. If the link ever operates there, even temporarily and no matter what the normal control, then the implication on voltage stability is exactly the same at that point for all cases and all schemes, regardless of other control modes. It should be noted that, even if the constant power control closed loop is opened, resulting in a pure constant current control, there is still a theoretical maximum power which can be supported by the AC system before voltage collapse takes place.

The points made above lead to the contention that the theoretical *MAP* and the critical minimum strength system values obtained from the "simple" equations are much more widely applicable and appropriate than may often be given credit.

Also, in the context of quasi-static controls, some mitigative measures can be enacted to either prevent or stop instability.

Based on the simple explanation given previously, the most obvious way to arrest the instability is to stop the normal controls from increasing the DC current whenever the AC voltage drops. But the normal controls must be allowed some margins and freedom, otherwise, other good things like regulation and damping during disturbances would also be stopped. Therefore, some under voltage threshold must be applied. In some systems, a U_{dhold} or similar control does this function. Basically, once the AC and hence DC voltage falls to a certain value, the U_{dhold} 'fools' the normal controls into thinking nothing further is happening and it stops increasing the DC current. This control can at least stop a runaway condition. But if this is the only protection, and if it is not functioning or if it fails, then a collapse could still result. Note also that this is equivalent to using a door-stop. It prevents the door from slamming the wall, but it does not close the door again. Therefore, this control 'stop' may not in itself prevent a bad operating situation.

While a U_{dhold} control can be a good back-up protection, there are other quasi-static or single action reactive controls, that are more effective in arresting a potential collapse, but still within the DC controls. This is by a SUVC (System Undervoltage Control) or by a PRBC (Power Runback Control). In principle, once the AC voltage falls to a certain level, these controls reduce or ramp-down the DC power by a set amount. This not only stops the collapse but it assists the AC voltage to recover by releasing reactive power back into the AC system, thereby returning the system back to a satisfactory operating state (it closes the door again).

The controls described above can only have limited capability to protect the system, and this is by design. In SUVC or PRBC controls, if the DC power were to be reduced by a large amount whenever an AC undervoltage occurs, then instability or collapse could almost always be prevented. But this would be generally unsatisfactory for system operation and for system requirements. In any system, the critical question will revert to determining how severe a contingency condition, reflected on the AC bus, that these controls must cater for and protect against. As examples, in many systems a determining contingency may be the loss of a large filter, capacitor bank or other large reactive power compensation device, including possible loss of nearby generating machines.

6.7 Effect of Dynamic Controls on Stability

Following on the above, in addition to any actions taken in the DC controls, the controls and characteristics of any nearby compensation equipment such as synchronous compensators (SCs) or Static Var Compensators (SVCs) can have a profound and rather complex effect on the voltage stability. Their basic function is to supply reactive power to the DC and to control the AC commutating voltage on a fast and continuous basis.

It was stated at the outset that unless additional reactive power is immediately available when the AC voltage drops, then the AC voltage will reduce further and the instability will be perpetuated. But if a connected compensating device had an infinitely fast response and unlimited range, then no limiting MAP would theoretically exist and system voltage collapse and DC instability would be impossible. On the other hand, if the compensator response were very slow or if it reached some compensating limit, then its ability to be able to prevent a system collapse would be correspondingly limited. The important factors are that any voltage controller must be sufficiently fast to correct any incremental voltage variations before 'runaway', and that it must have sufficient dynamic range to 'cover' for any event considered.

It is therefore established that there are two basic elements associated with the total analysis of the MAP and the voltage stability. One is the equivalent system impedance (usually considered as a static element and often expressed as $ESCR$) and the other is the voltage control (the dynamic element).

In the consideration of SVCs applied to DC, unlike synchronous compensators or other machines, SVCs do not directly contribute to system strength. It is sometimes stated that they can indirectly provide the equivalent to system strength by forced control action. But this appears to be a statement based mainly on their effective over voltage control, by activating controlled reactive absorption in the thyristor-controlled-reactor element. Power instability in a

weak system, however, is an AC under-voltage problem, not an over-voltage problem. And most SVCs by virtue of their most efficient conventional design, will cut-off their reactive absorption capability or be non-conducting in the reactive control element near full DC power, when the DC valves require maximum reactive power. But in contradiction, this is when the control is most needed for stability. If, on the other hand, the SVCs are over-designed to prevent cut-off in the reactor element at full DC load, then operation at normal conditions would be very inefficient and larger capacitor banks or filters must also be installed to counteract this design. Moreover, the reactive power loss from any static capacitor elements, on voltage reduction, is proportional to the square of the voltage drop, which then compounds the problem. This can create a severe design 'chase', whereby additional static capacitor banks can also lead to other problems such as greater over voltages, lower resonant frequencies with the AC system, aggravated DC operation due to voltage distortions and a decreased commutation failure performance [46], [47].

As an alternative to the SVC scenario discussed above, if the switching-on of static capacitors could be done fast enough in an emergency for stability, this could be done, in principle, without a controlled reactor element of a 'full' SVC. This would suggest that a fast-control, thyristor-switched-capacitor might be better for DC application. However, it should be noted that in thyristor-switched-capacitors, small finite steps are switched with response times up to one cycle plus control circuit decision time, resulting in dead bands of operation. This may not be able to stabilize, by itself, a DC converter and theoretically could make things worse if it results in any continuous jumping in and out of stable operation.

It is especially interesting to extend the above basic considerations to the situation of synchronous compensators (or other synchronous machines) connected to or nearby an inverter AC bus. Although expensive, synchronous compensators are most effective in curing instability because they genuinely contribute to the system strength (reduce the equivalent system impedance) through their impedance in the classic and static sense. In reality, however, this contribution is not static, but dynamic, and this will be discussed extensively below. Besides the assistance for power/voltage stability, synchronous compensators also have the advantages of providing inertia, raising the harmonic resonance of the system, improving the harmonic behaviour of the AC system and improving commutation failure performance [46], [47].

6.8 Introducing the Concept of "Dynamic MAP"

In discussing the concepts to this point, the only assumption about the AC side is that the AC bus voltage remains constant for the steady state determination of critical *ESCR* or *MAP*. But when a dynamic variation in the AC bus voltage occurs in a real system, including a response to this variation by any machine or compensator controls, then the *MAP* point can in principle continuously vary with time within the same system perturbation. This produces what can be termed a "dynamic *MAP*" [45].

These system dynamics could, in theory, be accounted for in the voltage stability phenomenon in two different ways. A more complete equation-set could possibly be developed to include the dynamics. Alternatively, the classic

equation-set (assuming static conditions) could be retained and the dynamic effects of controls or machines could then be reflected in the system reactance representation for the *MAP* and *ESCR* calculations. An example would be the reflected machine reactance representation for synchronous compensators. The analysis and impacts of dynamic system modelling on the power stability of DC systems has recently been significantly advanced in research and in the literature [35].

In the case of retaining the existing equation-set and for a given AC system makeup, the task becomes one of finding the representation of that AC system that, in fact, fits the already defined critical *ESCR*.

For the case where synchronous machines or compensators are connected at or near to the inverter AC bus, for this stability phenomenon, the machine representation is coupled to its control dynamics. Depending on the design of the machine and its field controls, the machine dynamics can be significantly influential throughout a time frame extending from the fastest power frequency voltage changes right through to steady state. In other words, depending on the stability situation and event, the machine representation that is most appropriate for the "dynamic *MAP*" or that best fits the critical *ESCR* can, in principle, range from the lowest possible value of subtransient reactance, X''_d, to the direct axis reactance, X_d.

For example, an X_d representation could apply, even during a dynamic perturbation, if the machine goes, or is forced to, an overexcited field current limit, thus relinquishing dynamic AC voltage control. In this condition, a slow system rundown or collapse can occur unless something special is done to stop it. Actual system experience and studies [44], [45], [49] have demonstrated that this condition, while in the past being considered as the separate phenomenon of "steady state var starvation", is actually just a boundary point of exactly the same principle as the power instability mechanism in faster time frames. Moreover, if this condition can occur in a DC scheme with nearby machines, it could represent the worst scenario for the instability because it would require the highest machine reactance (X_d) to meet the minimum critical *ESCR* allowed for stability.

At the other 'end' of the of the reactance spectrum, at X''_d, a different story must be told. If nearby machines can be kept in continuous automatic-voltage-regulator (AVR) control during a dynamic event, that is, kept away from any rating or excitation limits, and if the machine controls can be made fast enough to absolutely control the AC bus voltage at impending voltage collapse, then the appropriate machine reactance that would apply to the critical *ESCR* could in theory approach X''_d. The entire problem then simply reduces to making the machine controls fast or effective enough to produce a "dynamic *MAP*" which would be equivalent to a steady state *MAP* corresponding to a machine representation using X''_d. Stated another way, as long as the machines are in continuous AVR control, then the faster the machine response, the lower the equivalent reactance in that time frame (X''_d the lowest) and the more it can contribute to the equivalent system strength for stability considerations.

There has been a long standing debate in the industry over whether X'_d or X''_d is the most appropriate to use for these considerations. However, the Nelson River DC system with its synchronous compensators [43] demonstrates that it is realizable to design modern machines with exciters fast enough such that X''_d can be the appropriate equivalent reactance determining stability. Of course,

where a DC system has older machines with slow exciters in close proximity, then this is a different matter.

6.9 System Studies of Stability on Actual System

To gain an understanding of the effects of control on the power/voltage instability in DC links, the Nelson River HVDC system has been extensively modelled on transient stability and other programs [45], [49] . This system, which has been well documented [42], [43] employs 6-160 plus 3-300 Mvar synchronous compensators, in addition to 757 Mvar of filters at the inverter for the two bipoles. The maximum rating of the two bipoles is 3854 MW. The design *ESCR* is 2.5 based on X_d'' of the machines, and with two machines out-of-service (the design criteria). The *ESCR* is, of course, much less when based on X_d' or X_d of the machines, which shows the importance of the machine representation for various phenomena. For normal system operating conditions with all elements in-service and normal loading, the operating *ESCR* is above 3.

For purposes of modelling in these studies, both bipoles were 'locked' in power control with no switching to current control. Both the System Undervoltage Controller (SUVC), which reduces DC power a fixed amount when the AC voltage falls below a set value, and the U_{dhold} control, which "freezes" DC current by way of the power-divide-by-voltage, were inactivated. These controls had been instituted on this system after power instability and collapse shutdowns were experienced. Also for the studies, the gains in all compensator exciters were proportionately reduced from their normally tuned values. Compensator numbers were reduced and capacitors were added to lower the *ESCR* to the point of voltage instability for a particular exciter gain. The compensators were always kept in a position where they retained non-limited AVR control. The instability was 'triggered' by a small increase in DC power or by a small filter trip. The results of this investigation are shown in Figure 6.1.

To explain Figure 6.1, at each voltage regulator gain setting indicated on the horizontal axis, the vertical-set of three "x-points" on the three curves are derived from the single system which results in the onset of voltage instability, when the compensators are operating with that particular gain setting. That is, each vertical-set of three "x-points" represents one given system with a fixed number of compensators and capacitors connected. Then, the vertical axis values for the three "x-points" (and hence the three curves) are determined by calculating the *ESCR* of that system corresponding to the three machine reactances of X_d, X_d' and X_d'' . Going from one gain setting to the next on the horizontal axis, or from one set of three "x-points" to another, means going to a different system with a different number of machines and capacitors to produce the onset of instability.

The horizontal dashed line ($ESCR = 2$) represents the critical *ESCR* of the DC system based on the classic steady state stability equations referenced previously. The relatively high value of $ESCR = 2$ results partly from the DC operating condition being at 1.1 p.u. loading with the AC bus at about 0.95 p.u. initial voltage (the worst operating condition criteria). This does not mean that such stringent operating conditions are required to produce instability - it just means that inducement is easier. By comparing the three "x-point" levels at each gain setting relative to the level of the critical *ESCR* of the dc system, it can

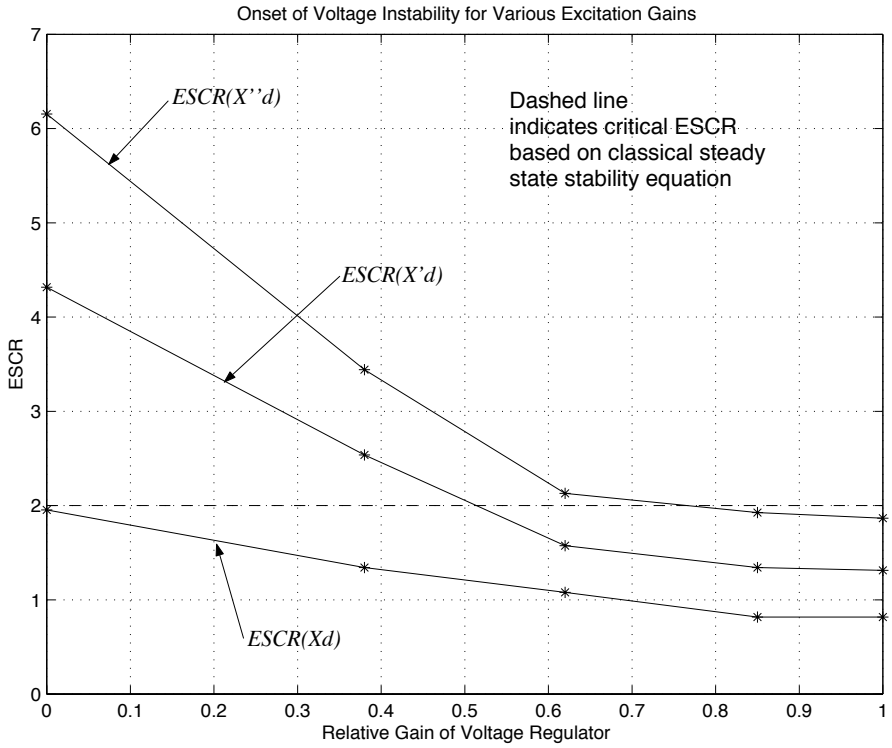

Figure 6.1. Curves showing the onset of voltage instability for various excitation gains on the synchronous compensators connected to the inverter AC bus (Nelson River HVDC system), as a comparison against the critical ESCR based on the classic steady state stability equation.

be determined which reactance is most appropriate to use in the steady state equivalent for calculating MAP; or for calculating the $ESCR$ to test against the critical $ESCR$. The "x-point" closest to the critical $ESCR = 2$ (in this case), based on the given system conditions, will indicate the most appropriate reactance. For example, at the normal voltage regulator gain (fastest response), the curves show that the $ESCR$ based on X''_d is the most appropriate to test for stability and to compare to the critical $ESCR$. As the effectiveness of the voltage regulator is changed from the normal fast control to a slower response (smaller values of gain), the curves show that the appropriate machine reactance for stability changes from X''_d to X'_d and finally, with the exciters disabled, to X_d.

These results show the importance of control to the voltage instability phenomenon. A modern, properly tuned exciter allows the use of X''_d in the equations and so maximizes the contribution of the machine.

When a machine is on a field current limit, the above results show that X_d will govern its contribution to the $ESCR$. Depending on the particular machine, X_d may be ten times or more than the X''_d quantity. For HVDC systems that depend on synchronous compensators or other machines for strength (generally, SC's would not be installed unless strength was required), then a field current

limit applied to these machines during operation leads to a dramatic reduction in the *ESCR* or the "dynamic *MAP*". For any operating states that produce this limit, there is likely to be a significant violation of the voltage stability criterion.

These considerations are important for any synchronous compensator design. There should be enough transient capability in the machines so that corrective action can be initiated before a field current limit is enforced.

The Nelson River DC system inverter bus is so dependent on synchronous compensators for reactive supply, as well as strength, that it is probable (virtually certain at full DC load) that the tripping of more than one compensator, or a combination of one compensator plus filters, will put the remaining machines on a limit before any X_d'' based instability is 'triggered'. The critical reactance would then revert to X_d , creating the condition for a slow voltage collapse mode characteristic of a "steady state var starvation".

Considering actual system experience, some years ago the inverter bus of this system suffered a number of voltage collapse events, which were only arrested by the out-of-step tripping of AC tie lines. The situation started developing at the time of increased power levels on the DC due to new generation and without an increase in reactive compensators. Generally, the collapse would be precipitated by the loss of a reactive power producing element, either a compensator or a filter, which would then force the operating compensators to an output limit. In fact, there has been no known situation, when the machines became limited, that did not initiate a voltage collapse. Conversely, there has not been a situation where the machines have been in full AVR control and a collapse initiated. These observations support the theoretical development of the above sections.

The initiation of the voltage collapse was at the time thought to be caused by simple "var starvation" - nothing to do with any critical *ESCR*. The theory for the power/voltage instability, which gained prominence later, was considered to be something separate. In reality, it was subsequently established, as explained above, that the "var starvation" was power instability, with X_d as the representative machine reactance. This is a more complete manner to describe these events because the lack of continuous voltage control does not necessarily mean a voltage collapse. There are many DC links that operate successfully without continuous AC voltage control as long as their operating states are above a critical *ESCR* (below their *MAP*). It is rather the change in machine reactance from X_d'' to X_d, which leads to a large change in *ESCR* and a resultant violation of the voltage stability criterion.

When the 3-300 Mvar synchronous compensators were added to the Nelson River system for additional strength, a formula for the critical *ESCR* was developed for use in the planning studies and for specifying the new machines [43]. The critical $ESCR = 2$ was derived from this formula. However, due to popular belief at the time, the new machines were specified to meet this target *ESCR* based on a machine reactance of X_d' instead of X_d'' in order to ensure operation below *MAP*. It was not until later that the implications of X_d'' and X_d as discussed above became known. It should be pointed out that for nominal conditions on this link, with DC power and AC voltage of 1.0 p.u., instead of 1.1 p.u. and 0.95 p.u., respectively, the critical *ESCR* is about 1.66.

Besides the additional compensators, there are now two controls installed on the Nelson River DC, which are intended to help correct or prevent the voltage

collapse problem. The first is the System Undervoltage Control (SUVC), which performs a relatively minor (about 300 MW) reduction when a collapsing AC voltage is detected. The second is a U_{dhold} control, which substitutes a fixed DC voltage into the constant-power-division circuit upon low AC voltage. While U_{dhold} should prevent a total collapse initiated by compensators on a limit, the violation of the criterion can be severe enough to cause a large change in AC voltage.

The main benefit of the SUVC is not in the small increase in ESCR from the reduction in DC power, but rather in the return of controllability to the compensators. Thereafter, the contribution of the compensators to the fault level in the ESCR calculation is based on X''_d instead of X_d . This is a dramatic increase in *ESCR*, which now makes the system stable. The SUVC is thus a dominant control in preventing voltage instability on this system for many possible conditions.

6.10 Implications for Other Systems

For a general HVDC system with no synchronous compensators, SVC's, or other machines nearby to the inverter AC bus, the calculation of the system state relative to the voltage stability criterion is fairly straightforward. For synchronous machines electrically further out into the AC network, the question of correct machine reactance and dynamics is of reduced concern since intervening line reactance will usually make the machine contribution and influence less important.

In addition to the discussion already made on SVC's, a system with a SVC at an inverter bus presents some further interesting considerations. With the effects of control ignored, the susceptance at which the SVC is operating is factored into the ESCR calculation for power stability. A SVC acting capacitively lowers the ESCR, which may be critical in an already weak system or even in the case of a weak-connection DC in-feed. It is therefore probable that, if the SVC is to be of any benefit, the control will be critical for viable operation. If the control were infinitely fast in correcting small-signal deviations, thereby keeping voltage absolutely constant, then it would totally 'hide' the weakness of the system or the DC connection point in terms relevant to stability. Of course, the closed loop control cannot be infinitely fast and in reality will tend to be tuned according to the minimum strength of the AC system into which it operates - the weaker the system, the slower the response. This would likely lead to an upper bound on the assistance a 'conventional' SVC can give to the prevention of voltage instability as the system becomes weaker. For DC application, the use of STATCOM's, which can more closely emulate the favourable characteristics of synchronous compensators, may present some advantages. But the economics of these devices will be critical to their viability.

When synchronous compensators are to be applied at an inverter, there are certain aspects of the design which are particularly important for voltage stability. The previous section has shown that keeping the AVR in full control is necessary in order to produce an effectively 'strong' dynamic system - in other words, the case using X''_d in the *ESCR* calculation. Furthermore, to maintain control in contingency situations, it will usually be desirable and economic to have some overload capability in the machines, to allow time for corrective

action before more restrictive limits are applied. To ensure a fast-acting control system, the effective time constant of the voltage measurement circuit of the AVR should be low, perhaps 25 milliseconds or less. For modern AVR designs, this should not be a problem. The field-forcing positive-limit may have some affect on stability for more severe disturbances by quickly returning the AC voltage to a safe level. Finally, the contribution of the machine to the fault level should be maximized from the perspective of stability, meaning the lowest realistic total of subtransient reactance plus transformer reactance. Of course, the down side of this is the possible implication on the fault rating of system circuit breakers and other equipment.

From all the foregoing discussion, the impression has no doubt been made that the worst single problem associated with incorporating an HVDC link into low *ESCR* weak-connections or weak AC systems may well involve the interrelated issues of DC power stability and reactive compensation at the inverter. Also, these issues are major problems from both technical and economic perspectives. All this applies to conventional line-commutated converters.

For relatively large power DC links, any requirement for sophisticated compensation equipment such as synchronous compensators or SVCs will represent major capital investment - a significant proportion of the total link cost. This increases the difficulty for conventional HVDC to compete against evolving new technologies in AC transmission systems and other supply alternatives. In some areas, it will also increase the difficulty to compete against alternative energy solutions that may also be aided by the restructuring and deregulation in the electrical industry.

If new DC technology, such as capacitive-commutated-converters or voltage-sourced converters, can eliminate the stability/compensation problems and become more economic, this will greatly enhance the possibility of new, large power HVDC links being applied in relatively weak or moderate AC systems.

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