305

GUIDE FOR APPLICATION OF IEC 62271-100 AND IEC 62271-1

PART 2
MAKING AND BREAKING TESTS

Working Group
A3.11

October 2006

GUIDE FOR APPLICATION OF IEC 62271-100 AND IEC 62271-1

PART 2 – MAKING AND BREAKING TESTS

Working Group A3.11
(Application Guide for IEC 62271-100 and IEC 60694)

Members: F.J. Amon (Brazil), J.-M. Biasse (France), J.Y. Blanc (France), A. Bosma (Sweden), D. Dufournet (France), D. Fuechsle (Switzerland), S.M. Ghufran Ali (United Kingdom), E. Haginomori (Japan), R. Jeanjean (France), S.L. Jones (Australia), S. de A. Morais (Brazil), I.D. Naylor (United Kingdom), J. Pasteau (France), D.F. Peelo (Canada), H. Peters (Germany), J. Reid (United Kingdom), H.-H. Schramm (Germany, convenor), H.M. Smith (USA), S. Théoleyre (France), Z. Vostracky (Czech Rep.), Ch. Wagner (USA), M. Waldron (United Kingdom).

CONTENTS

1 Miscellaneous provisions for breaking tests

The IEC 62271-100 subclauses relevant to this chapter are:

3.7.158 Minimum functional pressure for interruption and insulation

4. 104 Rated operating sequence

5.103 Pressure limits of fluids for operation

6.102 Miscellaneous provisions for making, breaking and switching tests

6.102.3.1 Arrangement of the circuit-breaker for tests – General

6.102.10 Demonstration of arcing times

1.1 Pressure to be used during demonstration of the rated operating sequence during short-circuit type tests

1.1.1 Background

There is a need for a consistent approach to the pressure requirements of hydraulic and pneumatic systems to be used during the demonstration of the short-circuit duties. The present wording of the standard is the result of considerable difficulty attempting to establish common earth or a satisfactory compromise. The requirement remains unclear. This chapter uses the historic approach in an attempt to set a common methodology and to justify its use.

A number of conflicting conditions exist, particularly for the auto-reclose operating sequence O-*t*-CO-*t*'-CO:

- The capability of the circuit-breaker for each short-circuit type-test duty must be demonstrated during performance of the rated operating sequence O-*t*-CO-*t*'-CO;
- Demonstration is by three valid open operations during the sequence O-*t*-CO-*t*'-CO;
- The minimum and maximum arc duration shall be demonstrated during the tests;
- The starting pressure for the O-*t*-CO part of the sequence cannot be less than the pressure that takes account of the pressure consumption of the O-*t*-C to enable the final O to be performed at pressures down to (in practice during testing, at) the circuit-breaker opening lock-out condition;

  NOTE - This O-*t*-CO start pressure is often termed the auto-reclose lock-out setting.
- The circuit-breaker must be able to perform a single O operation at its lock-out condition;
- Such single O operations must demonstrate satisfactory clearance for both the minimum and maximum arc durations;
- Where appropriate, the gas pressure for interruptions shall also be at its lock-out setting.

The combination of events necessary to produce such boundary condition requirements are credible in practice, i.e. lowest gas, lowest operating pressure, minimum and/or maximum arc duration operation, and full short-circuit current rating and as such they should be tested.

Clearly to demonstrate these combined requirements needs more than three operations. There is some assistance here in that prior to starting the demonstration of the rated operating sequence it is now an established requirement to demonstrate the minimum arc duration (6.102.10.2.1.1 of IEC 62271-100). This requires an additional, separate, open operation, which should be performed at the opening lock-out condition. It is here that some divergence of opinion arises amongst the experts, not only concerning whether the above is a credible condition but also the implications for the demonstration of the rated operating

sequence. If this minimum arc duration is repeated for the setting of the **first** O of the rated operating sequence, then the pressure is too low for the O-*t*-CO element. If the pressure is raised then the arc duration is incorrect for that pressure. For some designs such differences are, or may be, significant.

1.1.2 Recommendation

It is recommended that for the convenience of testing and to establish a consistent approach the following combination of operations for the sequence O-*t*-CO-*t'*-CO should be demonstrated:

a) Open at the pressure of the opening lock-out setting to demonstrate the minimum arcing time. An additional open operation is required, with the contact separation retarded by 18^{0} (1/0,8 ms for 50/60 Hz), to prove that the minimum arcing time has been established. This opening operation is designated O_{mm} (open at minimum arc duration and minimum pressure)

   NOTE 1 The additional test is also used during synthetic testing to demonstrate that the arcing is correctly controlled during this re-ignited operation.

b) Sub-sequence O-*t*-CO with the first O at the auto-reclose pressure and with arcing times demonstrating at the first O the minimum arcing time established in a) above and at the second O the maximum arcing time appropriate to the established minimum arcing time of a) above. The maximum O will be designated O_{Mm} (open at maximum arcing time and minimum pressure).

   NOTE 2 The auto-reclose lock-out pressure is that required to enable the final open operation of the auto re-close sequence O-*t*-CO to be performed at a pressure (just) above the opening lock-out value.

c) The final sub-sequence C-*t'*-O should demonstrate the medium arcing time and the pressure for this O will be the opening lock-out value. The pressure for the C will be set accordingly. This medium arcing time O will be termed O_{medm} (open at medium arcing time and minimum pressure).

Where the supplier considers that this is over-testing, because the first O in b) above is requiring an arcing time unrelated to the higher pressure of the auto-reclose lock-out condition that it operates at during the sequence, then additional, separate, operations will be required. These must form part of the same series of tests and prove O_{mm} and possibly O_{Mm} are adequately demonstrated. These should be performed without additional maintenance of the contact system.

For other rated operating sequences e.g. CO-*t*-CO, it remains necessary to demonstrate O_{mm} and O_{Mm}.

For switching operations, e.g. capacitive switching, the standard requirements are clear.

2 Rated and test frequency

The IEC 62271-1 and IEC 62271-100 subclauses relevant to this chapter are:

4.3	Rated frequency
4.4	Rated normal current and temperature rise
4.5	Rated short-time withstand current
4.6	Rated peak withstand current
6.5	Temperature rise tests
4.101	Rated short-circuit breaking current
4.103	Rated short-circuit making current
6.6	Short-time withstand current and peak withstand current tests
6.102.10	Demonstration of arcing times
6.103	Test circuits for short-circuit making and breaking tests
6.106	Basic short-circuit test duties
6.109	Short-line fault tests
6.111	Capacitive current switching tests

2.1 General

Two different frequencies are used in electric power systems. These frequencies are 50 Hz and 60 Hz.

All circuit-breakers have to operate properly for each test duty and the frequencies of 50 and 60 Hz.

The power frequency has an influence on the following tests:

- Temperature rise;
- Short-time withstand current;
- Terminal fault tests;
- Short-line fault test;
- Capacitive current switching.

The different test circuits used during testing also have an influence on the switching performance. These circuits are:

- Direct test circuits;
- Synthetic test circuit with voltage injection;
- Synthetic test circuits with current injection.

2.2 Basic considerations

2.2.1 Temperature rise tests

The maximum temperature rise is dependent on the test frequency and the type of apparatus (GIS or AIS equipment) to be tested.

2.2.2 Short-time withstand current and peak withstand current tests

The short-time withstand current test is characterised by the duration of the short-circuit.

The tolerance of the frequency is ± 10 %, but for convenience of testing a wider tolerance is allowed. IEC 62271-1 contains a cautionary note that care should be taken when interpreting test results when 50 Hz test are used to cover 60 Hz and vice versa.

The highest dynamic stress on the contacts and connections occurs during the peak withstand current test. The peak of the current is determined by the time constant of the network and the rated frequency. IEC 62271-1 specifies two values for the peak factor (k = I_{peak}/i_{sym}) at a time constant of 45 ms. They are: k = 2,5 for 50 Hz and 2,6 for 60 Hz.

NOTE Peak factors higher than 2,6 may be required when different time constants are used. For example, the special cases time constants are covered by a peak factor of 2,7.

2.2.3 Short-circuit making current

The peak of the making current is determined by the time constant of the network and the rated frequency. IEC 62271-100 states the following values for the peak factor (k = I_{peak}/i_{sym}):

- 2,5 for a rated frequency of 50 Hz and a time constant of 45 ms;
- 2,6 for a rated frequency of 60 Hz and a time constant of 45 ms;
- 2,7 for all special cases time constants, independent of the frequency.

2.2.4 Terminal Faults

A higher frequency leads to a shorter arcing window, because the time between two current zeros is reduced correspondingly. For example, when the minimum arcing time of a circuit breaker is 12 ms, the maximum arcing time that has to be demonstrated for single-phase testing at 50 Hz is 21 ms (12 – 1 + 10 ms). At 60 Hz the maximum arcing time is 20,3 ms (12 – 1 + 8,3 ms).

For test-duty T100a, a separate test may be necessary to prove that the operating mechanism has sufficient energy in case of 50 Hz application when the test has been performed using a 60 Hz current source, despite the fact that longer arcing times based on 50 Hz have been tested. The same is applicable for metal enclosed and dead tank circuit-breakers due to higher exhaust energy at longer arcing times, which can influence the phase-to-phase or phase-to-earth insulation.

The ITRV stress for different rated frequencies in live-tank circuit-breaker application is not taken into consideration when:

- the short-line fault test is carried out with a line-side time-delay t_{dL} equal to zero without significant differences in arcing time between short-line fault and terminal fault tests;
- the arcing window covers the corresponding frequency.

In the case that the terminal fault test is tested in a synthetic test circuit with voltage injection and the short-line fault test is not carried out with a line-side time delay equal to zero, the terminal fault test has to be performed with ITRV on live-tank circuit-breakers.

Test duties T100a and T100s performed with lower di/dt, for example in a voltage injection circuit with a 50 Hz current source, are valid for 60 Hz if the short-line fault is tested with a

di/dt representing 60 Hz and a line side time delay equal to zero. In the case that these tests are performed with a 60 Hz current source, they are valid only for 50 Hz if the line side time delay time delay during the short-line fault test is zero and the arcing times corresponding to 50 Hz ($t_{arc\ min}$, $t_{arc\ max}$ = $t_{arc\ min}$ – 1 ms+ 10 ms, $t_{arc\ max}$ – 3 ms).

2.2.5 Short-line fault

For short-line fault tests both the rate-of-decay of the short-circuit current before current zero and the arcing window are important factors. A higher rated frequency means a higher rate-of-rise of the line side TRV. Since the rate-of-rise of the line side TRV influences mainly the thermal interrupting behaviour of a circuit-breaker, it is important that the di/dt in the test report equal to or higher than required for the specified frequency.

For example a 90 % short-line fault test performed at 50 Hz with a line impedance of 450 Ω for a rated short-circuit current of 40 kA results in a line-side rate-of-rise of the TRV of 7,2 kV/μs, whereas the same test performed at 60 Hz would have a 20 % higher rate-of-rise of the line side TRV.

Therefore tests performed at 50 Hz are only valid for 60 Hz provided that the tests are performed with a synthetic test circuit where the rate-of-rise of the current is adjusted to 60 Hz.

If the test is performed at 60 Hz, it is only valid for a rated frequency of 50 Hz provided that the maximum arcing time for 50 Hz is covered. However, this is only possible in synthetic test circuit because any arcing time can be chosen.

2.2.6 Capacitive current switching

When the interrupting performance of a circuit-breaker for different rated frequencies is compared in capacitive switching tests, the only important factor is the recovery voltage as function of time. It is characterised by the voltage peak and the time to peak. Since the withstand capability of a circuit-breaker is a function of time, the higher frequency results in a higher stress on the circuit-breaker at arcing times close to zero. For example, the time to peak for 50 Hz is 10 ms, whereas it is only 8,3 ms in 60 Hz applications.

When interrupting with arcing times longer than the minimum arcing time, the contact gap is wider and therefore the voltage withstand of the circuit-breaker is higher. Maximum arcing time is therefore not an important factor when comparing tests performed at different frequencies.

Different methods are available to produce the correct voltage stress between circuit-breaker contacts, i.e. synthetic capacitive circuits or phase shift circuits in direct test circuits.

2.3 Applicability of type tests at different frequencies

2.3.1 Temperature rise tests

Tests performed at 60 Hz are valid for 50 Hz without any exception.

Tests performed at 50 Hz are valid for 60 Hz as long as the maximum temperature rise of the contacts and connections is below 95 % of the required values.

2.3.2 Short-time withstand current and peak withstand current tests

When testing switchgear and controlgear at 50 Hz, the test is also valid for 60 Hz and vice versa.

Care should be taken when a test based on 50 Hz with a peak factor of 2,5 is used to cover 60 Hz application or any of the special cases time constants.

2.3.3 Short-circuit making current test

A test performed at 50 Hz covers 60 Hz application provided that the peak current is that of the 60 Hz case.

2.3.4 Terminal faults

2.3.4.1 Direct test

Tests performed at 50 Hz can be applied on 60 Hz with the following assumption:

- The short-line fault is performed with a di/dt corresponding to 60 Hz and the line side time delay t_{dL} < 100 ns.

Tests performed at 60 Hz cannot be applied on 50 Hz due to a reduced arcing time window.

2.3.4.2 Synthetic test

The applicability of tests is independent of the frequency of the high current source.

Tests performed at 50 Hz can be applied on 60 Hz when:

- The short-line fault is performed with a di/dt the corresponding to 60 Hz and the line side time delay t_{dL} < 100 ns;
- The tests are performed with an ITRV based on the di/dt of 60 Hz application and if the short-line fault is tested with the rated line side time delay (200 ns and 500 ns, respectively).

Tests performed at 60 Hz can be applied on 50 Hz as long as:

- the arcing window is covered;
- evidence is provided to demonstrate the sufficient drive energy;
- evidence of the dielectric behaviour in T100a is provided for metal enclosed and dead tank circuit-breakers.

2.3.5 Short-line fault

2.3.5.1 Direct test

Tests performed at 60 Hz can only be used for 50 Hz application as long as the arcing window is covered.

Tests performed at 50 Hz can never be used for 60 Hz due to the lower di/dt value at current interruption.

2.3.5.2 Synthetic test

Tests performed at 60 Hz can only be used for 50 Hz application as long as the arcing window is covered.

Tests performed at 50 Hz can only be used for 60 Hz if the di/dt value at current interruption is adjusted to 60 Hz independent of the power frequency of the high current source.

2.3.6 Capacitive current switching

Tests performed at 60 Hz are valid for 50 Hz without any exceptions.

Tests performed at 50 Hz are only applicable to 60 Hz if the recovery voltage excursion equals to or exceeds the required 60 Hz curve. This means that a higher test voltage needs to

be used. To fully cover a 60 Hz test with a 50 Hz voltage, this voltage need to be increased with a factor of 1,44 compared to the 60 Hz voltage. Alternatively, a test performed at 50 Hz with a high capacitive voltage factor can be used for 60 Hz application with a lower capacitive voltage factor.

3 Terminal faults

This chapter treats short-circuit currents and their arcing time and the associated transient recovery voltages.

The IEC 62271-100 subclauses relevant to this chapter are:

6.102 Miscellaneous provisions for making, breaking and switching tests

6.104 Short-circuit test quantities

6.106 Basic short-circuit test-duties

6.107 Critical current test

8.101 Guide to the selection of circuit-breakers for service – General

Subclauses of IEC 62271-100 referenced as applicable to the aspects of recovery voltages being considered here:

3.7.152 First-pole-to-clear factor (in a three-phase system)

4.102 Transient recovery voltage related to the short-circuit breaking current

6.103.3 Earthing of test circuit

6.104 Short-circuit test quantities

6.108 Single-phase and double earth fault tests

8.101 Guide to the selection of circuit-breakers for service

3.1 Introduction

This chapter considers the clauses relating to the symmetrical terminal fault conditions. These are encompassed within the requirements for the short-circuit test duties T100s, T60, T30, and T10. The asymmetrical duty T100a and the various short-line fault and out-of-phase duties are considered in other chapters of this guide.

The purpose of this chapter is to provide a background framework for some of these requirements where it may not be clear from the latest revision of the standard, or from readily available text books, how they were derived.

The aspects covered in this chapter are those relating to the short-circuit current, particularly to the arcing time and the voltages, both power frequency and transient recovery voltage (TRV), associated with terminal faults.

The system may be earthed in different ways depending on system voltage and application. The following definitions apply:

solidly earthed (neutral) system

a system whose neutral point(s) is (are) directly earthed (IEV 601-02-25).

effectively earthed neutral system

system earthed through a sufficiently low impedance such that for all system conditions the ratio of the zero-sequence reactance to the positive-sequence reactance (X_0/X_1) is positive and less than three, and the ratio of the zero-sequence resistance to the positive-sequence reactance (R_0/X_1) is positive and less than one. Normally such systems are solidly earthed (neutral) systems or low impedance earthed (neutral) systems.

NOTE For the correct assessment of the earthing conditions not only the physical earthing conditions around the relevant location but the total system is to be considered.

non-effectively earthed neutral system

system other than effectively earthed neutral system, not meeting the conditions given in 3.1.128. Normally such systems are isolated neutral systems, high impedance earthed (neutral) systems or resonant earthed (neutral) systems.

NOTE For the correct assessment of the earthing conditions not only the physical earthing conditions around the relevant location but the total system is to be considered.

3.2 Demonstration of arcing time

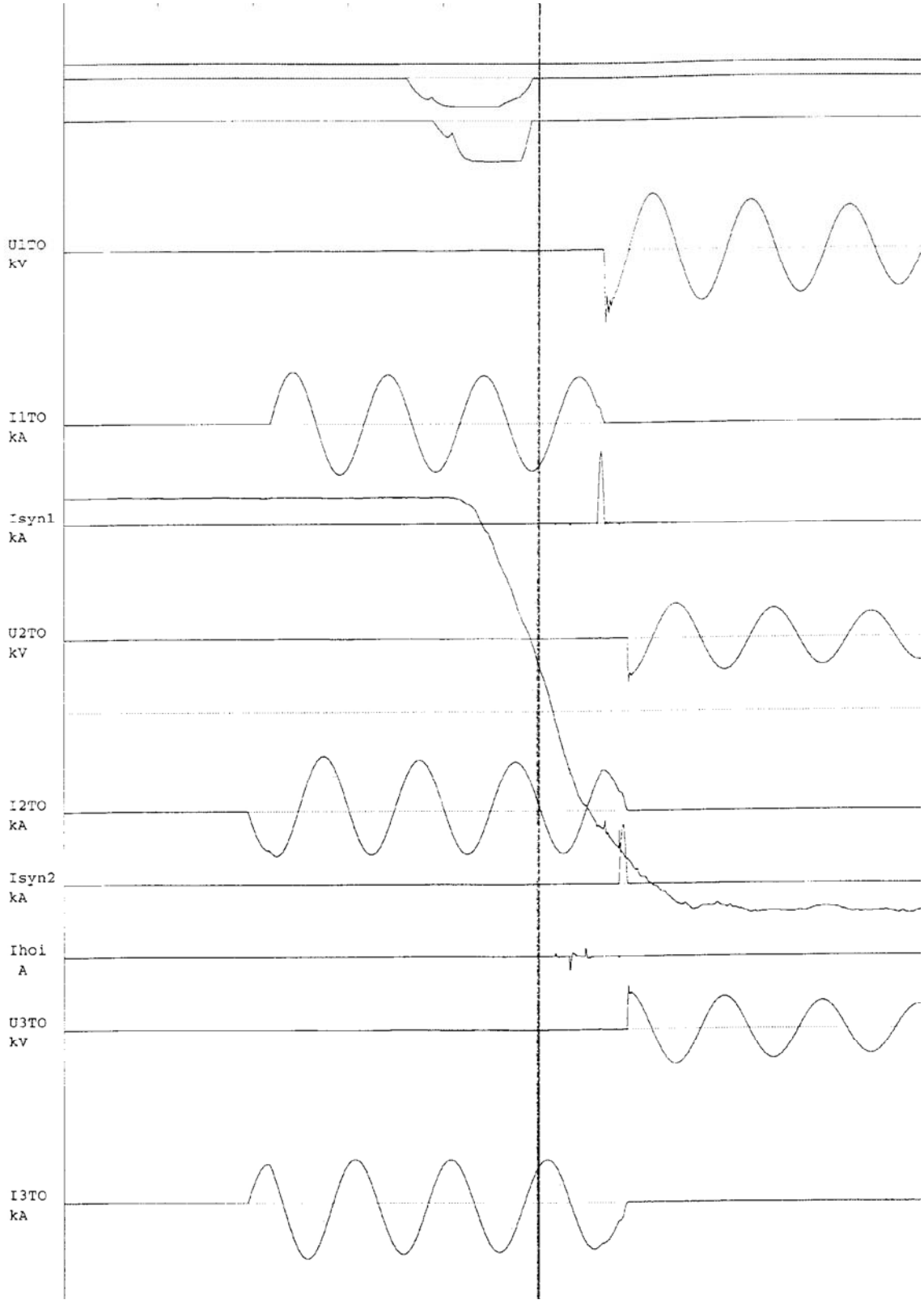
Throughout IEC 62271-100 and related documents the terms arcing time, arcing window and interrupting window are used, especially in relation to the interruption of short-circuit currents. To understand the requirements of the various clauses of IEC 62271-100, such as 6.102.10, it is necessary to understand the meaning of these terms and that of the terms minimum and maximum arcing time in particular.

A circuit-breaker is required to interrupt short-circuit currents regardless of the point on the cycle of power frequency current its interrupter contacts separate mechanically. When this mechanical separation occurs the contacts are said to have parted and when the subsequent arcing ceases, the current is interrupted. The time between contact parting and current interruption in all three phases is the arcing time that is being considered here. Arcing time is measured in milliseconds (ms), or in electrical degrees (e.g. 10,0 ms at 50 Hz and 8,3 ms at 60 Hz are 180°). The shortest arcing time at which the circuit-breaker is able to interrupt is the minimum arcing time.

Depending on the point of contact separation and the particular current, the arcing time of a circuit-breaker will vary between this minimum value and a maximum value. The difference between these values is called the arcing window (or more rarely the interrupting window). Although different designs of circuit-breaker will be capable of interruption over different ranges there is a basic requirement which is applicable to all modern designs of circuit-breaker. In these the minimum arc time is short or relatively short, and in addition, they have limited capability for prolonged arcing as their quenching period is also short.

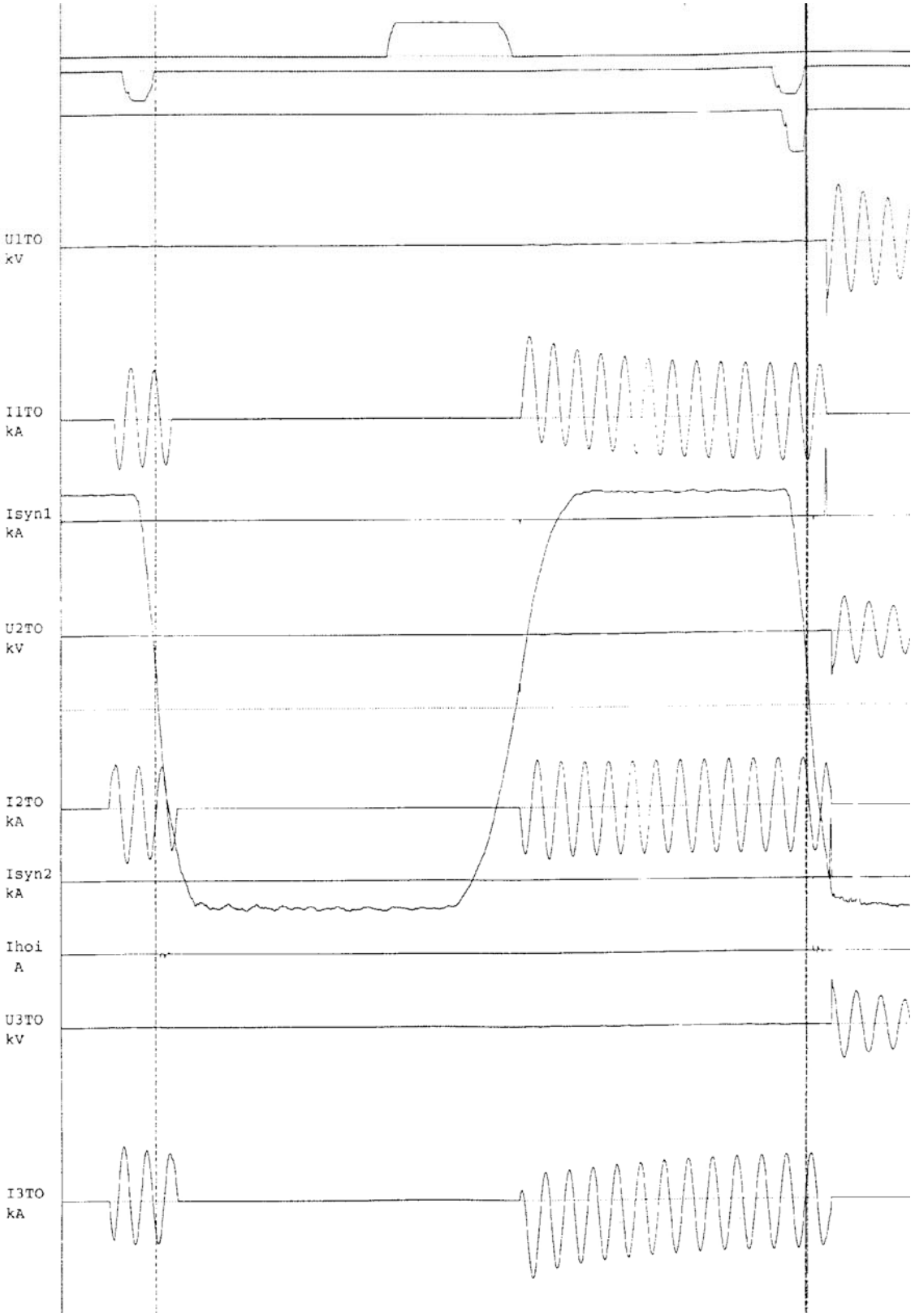
During each test duty series (e.g. T100s or T60) it is necessary to demonstrate this basic arcing window. The minimum and maximum cannot be demonstrated in a single valid test.

In the case of fault interruptions involving three-phases the minimum arcing time is obtained in one of the valid tests of a duty with the first-pole-to-clear and the maximum arcing time is obtained in another valid test with the last pole(s) to clear. See Figure 1 and Figure 2.



Pole 1 is the first-pole-to-clear with minimum arcing time of 13,7ms. O-operation at 50 Hz.

Figure 1 - Three-phase test with a three-phase fault



Poles 2 and 3 are the last-poles-to-clear with a maximum arcing time of 21,6 ms giving an interrupting arcing window of 21,6 – 13,7 = 7,9 ms. The requirement for this test is 150° - 18° = 132° equivalent to 7,3 ms at 50 Hz.

Figure 2 - Demonstration of maximum arcing time: second O of an OCO operation at 50 Hz

For single-phase faults the maximum arcing time is the period to the end of the arcing window of the faulted phase, consisting of the minimum arcing time plus one loop of fault current minus 18°. This 18° is related to a deliberately specified step, of equal duration for 50 Hz and 60 Hz, giving a point of contact separation a short period later than that giving the minimum arcing time. At this setting the arcing time is too short for satisfactory clearance as a minimum, by definition, and an additional loop i.e.180°, has to be endured until the next current zero. Clearance at this later zero gives the maximum arcing time and the end of the arcing window.

This short period is a specified step of 18° as this is the smallest practical value for such a step generally achievable at testing stations being 1 ms at 50 Hz and 0,8 ms at 60 Hz.

3.3 Demonstration of the arcing time for three-phase tests

The arcing time requirement must be demonstrated during the sequence of three valid tests of each of the specified short-circuit test duties (e.g. T100s or T60).

When three-phase symmetrical current tests are to be demonstrated using direct test techniques, the possible arcing times are automatically obtained by changing the setting of contact separation by a duration of 40° between each of the three required opening operations of the operating sequence (6.102.10.1.1 of IEC 62271-100). In this way, taking into account that current passes through zero on one of the phases every 60°, the minimum arcing time is determined with a precision of less than 20°.

For synthetic testing the procedure is defined in IEC 62271-101.

3.4 Power frequency recovery voltage and the selection of the first-pole-to-clear factors 1,0, 1,3 and 1,5

3.4.1 Introduction

The first–pole–to-clear factor (k_{pp}) is a function of the earthing arrangements of the system. As defined in 3.7.152 of IEC 62271-100 it is the ratio of the power frequency voltage across the interrupting pole before current interruption in the other poles, to the power frequency voltage occurring across the pole or poles after interruption in all three poles. For non-effectively earthed neutral systems this ratio is or tends towards 1,5. For rated voltages less than 170 kV such systems are not uncommon, particular within Europe and Japan.

For effectively earthed neutral systems, the realistic and practical value is dependent upon the sequence impedances of the actual earth paths from the location of the fault to the various system neutral points (the ratio X_0/X_1). The value used in IEC 62271-100 is taken to be ≤ 3 (see Equation (1)). The X_0/X_1 value is a standard value confirmed by system studies of various networks. Hence, for rating purposes, IEC 62271-100 considers two values for the three-phase short-circuit condition. These are adequate for the many, different, system earthing arrangements:

a) the non-effectively earthed, to cover all unearthed systems and those with some deliberate additional impedance in the neutral system. A standardised value for k_{pp} of 1,5 is used for all such systems;

b) all effectively earthed systems where it is accepted that some impedance exists. For standardisation purposes the value for k_{pp} used is 1,3.

A third condition does exist, this is where the fault is single-phase in a solidly earthed system and the last-pole-to-clear is considered. For this condition k_{pp} is 1,0.

At transmission voltages there has been an increase in interconnection and transformation particularly in major urban systems. The high number of transformer neutrals connected effectively to earth is causing the value of 1,3 to be questioned. Although this has been

considered, the text of IEC 62271-100 does not take account of these developments. It is important for users with such systems to note that as k_{pp} decreases towards unity the value of the second-pole-to-clear factor will fall. In addition the value of the phase currents will change. The three phases become three independent single-phases each with k_{pp} approaching 1,0. In general the users of such systems are aware of this possibility and of the need to consider the actual system conditions when assessing the suitability of their specified requirements and the test evidence they are offered against these.

Where the ratio of three-phase to single-phase earth fault current is 1,0, k_{pp} is also 1,0. However, although this is normally assumed to be adequately covered by the use of the three-phase requirements and the associated with a k_{pp} of 1,3, it is important that evidence is provided to demonstrate the extended arc condition of the single-phase fault. For a single-phase fault an appropriate full arcing window must be demonstrated.

It should be noted that in accordance with 6.108 of IEC 62271-100 specific recovery voltage conditions are required to demonstrate the ability of a circuit-breaker to clear single-phase and double earth faults.

Regarding earthing of the test circuit, reference is made to 6.103.3 of IEC 62271-100.

3.4.2 Equations for the first, second and third pole-to-clear factors

The equation for the first-pole-to-clear factor:

$$k_{pp} = \frac{3X_0}{X_1 + 2X_0} \qquad (1),$$

where X_0 is the zero sequence, and X_1 the positive sequence reactance of the system.

If $X_0 >> X_1$, as in non-effectively earthed neutral systems then: $\boldsymbol{k_{pp} = 1,5}$

If $X_0 = 3,25 \times X_1$, as in effectively earthed neutral systems then: $\boldsymbol{k_{pp} = 1,3}$

If $X_0 = X_1$, as in a solidly earthed system, then: $\boldsymbol{k_{pp} = 1,0}$

Following interruption of the first-pole-to-clear the remaining two phases form a series circuit with the fault path.

In systems with non-effectively earthed neutrals the second and third phases interrupt in series under the phase-to-phase voltage so that for each pole,

$$k_{pp} = \frac{\sqrt{2}}{3}$$

In systems with effectively earthed neutrals the second pole clears with a factor of,

$$k_{pp} = \frac{\sqrt{3(X_0^2 + X_0 X_1 + X_1^2)}}{X_0 + 2X_1} \qquad (2)$$

Equation (2) can be expressed as a function of the ratio $\alpha = X_0/X_1$:

$$k_{pp} = \frac{\sqrt{3}\sqrt{\alpha^2 + \alpha + 1}}{2 + \alpha}$$

For the third pole-to-clear in a effectively earthed system

$$k_{pp} = 1$$

Table 1 gives k_{pp} for each clearing pole as a function of X_0/X_1 as appropriate.

Table 1 - Pole-to-clear factors for each clearing pole

X_0/X_1	Pole-to-clear factor		
Ratio	**First**	**Second**	**Third**
3,25	1,3	1,27	1,0
1,00	1,0	1,00	1,0

The respective multiplying factors for the peak value of the TRV (u_c) are given in Table 2 of IEC 62271-100. It is important to note that the amplitude factor is the same for each pole. The multiplying factors are as applied to the power frequency voltages.

3.4.3 Standardised values for the second- and third- pole-to-clear factors

IEC 62271-100 has standardised values for the second and third-pole to clear factors for three-phase testing. These are given in Table 2 of IEC 62271-100 and section 3.7 of this guide deals with this topic in relation to demonstration of arcing times for these poles and the appropriate pole factors relevant to each opening pole. It is important to note that on systems where the neutral earthing is solid, both the first-pole-to-clear factor of 1,3 and the values provided in 4.102.3 of IEC 62271-100 for second- and third-pole-to-clear factor, may be significantly different to the actual system requirements. This is likely to be a rare occurrence, generally associated with urban systems where there are numerous effectively earthed transformers in close proximity. Where such differences are significant, the user is generally aware that it may be necessary to consider specifying system specific requirements and tests. The note to 6.103.3 b) of IEC 62271-100 makes reference to this.

Table 2 – Pole-to-clear factors for various types of faults

Type of fault	First-pole-to-clear	Second-pole-to-clear	Third-pole-to-clear
Phase-to-earth	1	-	-
Two-phase not involving earth	Simultaneous opening of both poles: $\frac{\sqrt{3}}{2}$ OR If a pole fails: $\sqrt{3}$	Simultaneous opening of both poles: $\frac{\sqrt{3}}{2}$	-
Two-phase-to-earth	$k_{pp} = \frac{\sqrt{3}\sqrt{\alpha^2+\alpha+1}}{2+\alpha}$ [between $\frac{\sqrt{3}}{2}$ and $\sqrt{3}$] $\alpha = X_0/X_1$	1	-
Three-phase not involving earth	1,5	Simultaneous opening of both poles: $\frac{\sqrt{3}}{2}$ OR If a pole fails: $\sqrt{3}$	Simultaneous opening of both poles: $\frac{\sqrt{3}}{2}$
Three-phase-to-earth in effectively earthed systems	$1{,}5 \times \frac{2\alpha}{1+2\alpha}$ [between 0 and 3/2] $\alpha = X_0/X_1$	$k_{pp} = \frac{\sqrt{3}\sqrt{\alpha^2+\alpha+1}}{2+\alpha}$ [between $\frac{\sqrt{3}}{2}$ and $\sqrt{3}$] $\alpha = X_0/X_1$	1

3.4.4 Combination tests for k_{pp} = 1,3 and 1,5

For T100s tests for a requirement with an first-pole-to-clear factor of 1,3 it is possible to adapt the test procedure during tests for a factor of 1,5. Two alternatives exist:

a) test with k_{pp} 1,5 but ensure the arc window (see 3.2 above) covers the range (180° – dα);

b) test with k_{pp} 1,5 for its normal arc window of (150 - dα) plus an additional test with k_{pp} 1,3 and an arcing time of minimum arc time plus (180- dα). As stated in 3.6 all additional testing of this nature should be performed as CO operations.

3.5 Characteristics of recovery voltage

3.5.1 Values of rate-of-rise of recovery voltage and time delays

The values for the rate-of-rise-of-recovery-voltage (RRRV) for the first-pole-to-clear, and the associated time-delay values, were derived from system studies, supported by system tests performed in and before the mid-1970s. The values adopted (2 kV/μs etc.) have been shown by this work to be adequate for all developed systems, and are generally acceptable for others.

IEC 62271-100 gives multipliers for the RRRV for the second and third poles-to-clear. These values were derived by calculation.

Users with effectively earthed neutral connections may need to consider the RRRV for the three separate poles as these tend to increase with the increase in short-circuit current.

3.5.2 Amplitude factors.

The values of the amplitude factors for T100 and T60 are 1,4 and 1,5 respectively. These values where adopted into IEC 62271-100 as a result of system studies. The values mainly depend on the reflection timings along the lines connected to the source sides, and generally remain acceptable and are used in IEC 62271-100.

3.6 The requirements for performing single-phase tests in substitution for three-phase conditions

Separate procedures exist for tests performed in substitution for three-phase conditions by using a single pole of the circuit-breaker.

The procedure as defined is for circuit-breakers to be installed in systems with non-effectively earthed neutral and separately for those with effectively earthed neutrals, that is where ($X_1/X_0 \leq 3$). The relevant clauses in IEC 62271-100 are 6.102.10.2.1 and 6.102.10.2.2.

Figure 3 provides a graphical representation of the required arcing window for each condition in the case of interruptions with symmetrical currents, as for test duties T10, T30, T60, and T100s. (Note, this also applies to short-line fault and the out-of-phase TEST-duties OP1, OP2). Whether the testing is for three-phase test requirements, or single-phase tests in substitution for the three-phase condition, it is important that the arcing window and associated TRV are demonstrated for the relevant system condition. In the case of a single pole, the three tests of the duty are demonstrated on that single pole, as it is the representative sample of the circuit-breaker, as allowed in clause 6.102.2 of IEC 62271-100.

Although alternative combinations of these requirements are possible using more than three operations, where this is the case it is recommended that these additional operations should be performed as CO-operations to ensure equivalence.

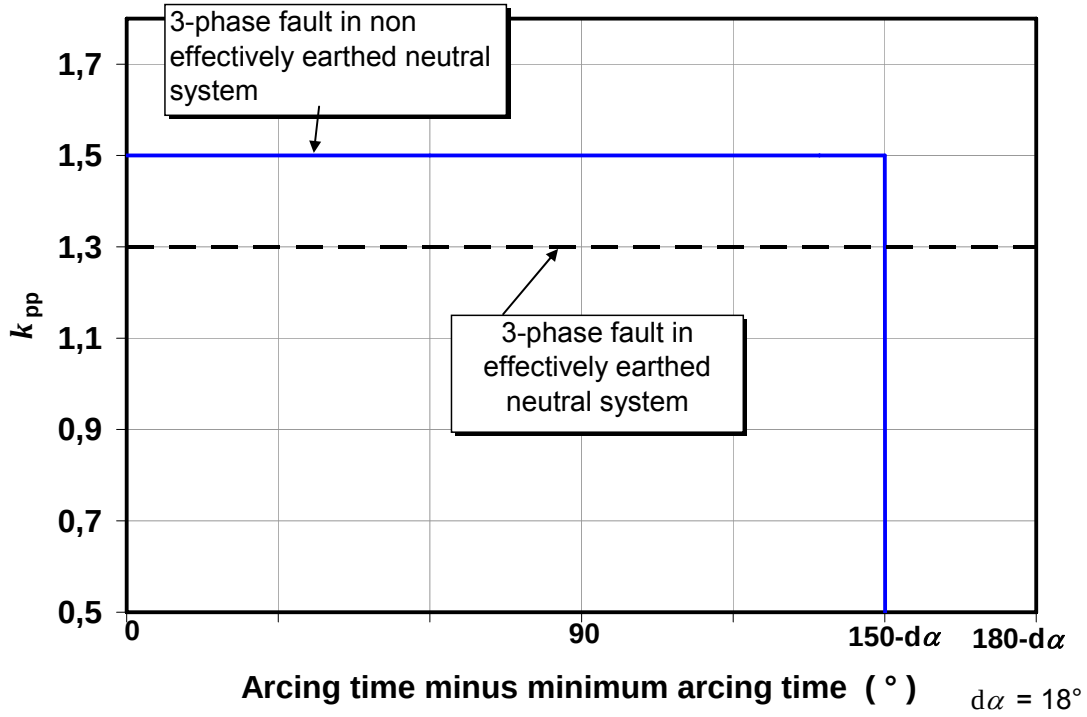


Figure 3 - k_{pp} as a function of arcing time minus minimum arcing time

3.7 Procedure for testing the other clearing poles of a three-phase test-duty by the separation of the test-duties within a test series, taking into account the associated TRV for each pole-to-clear

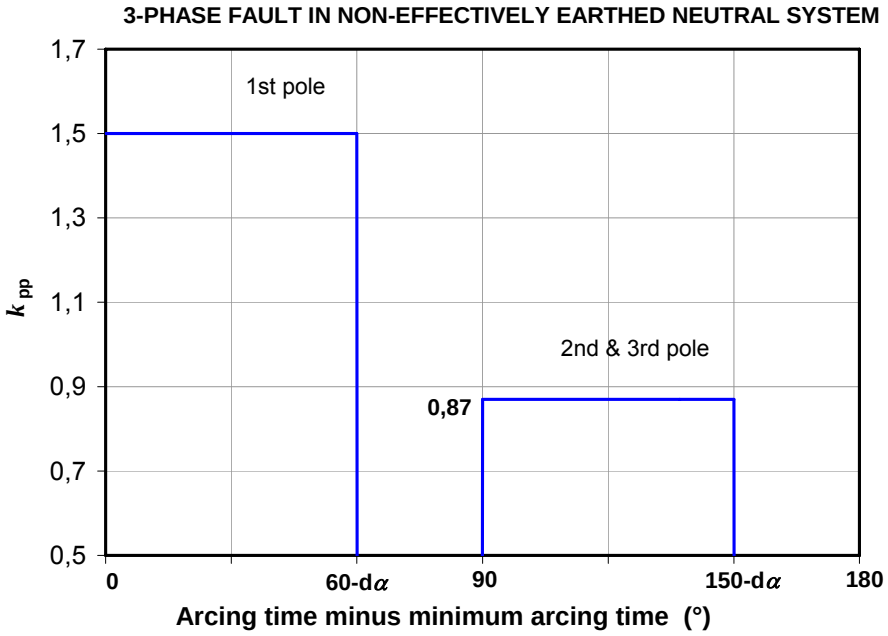
An alternative test procedure is permitted because it is recognised that single-phase tests in substitution for three-phase tests as detailed in 3.6 are more severe than three-phase tests. This is due to the use of the arcing time of the last pole to clear in combination with the TRV of the first-pole-to-clear. (See earlier clauses of this chapter).

Figure 4 and Figure 5 are associated with Table 12 of IEC 62271-100 and are duplicated here for convenience. They give graphical representations of the arcing windows that have to be demonstrated, together with the corresponding values of k_{pp}.

Figure 4 illustrates the case of non-effectively earthed neutral systems and Figure 5 illustrates the case of effectively earthed neutral ($X_0/X_1 \leq 3$) systems.

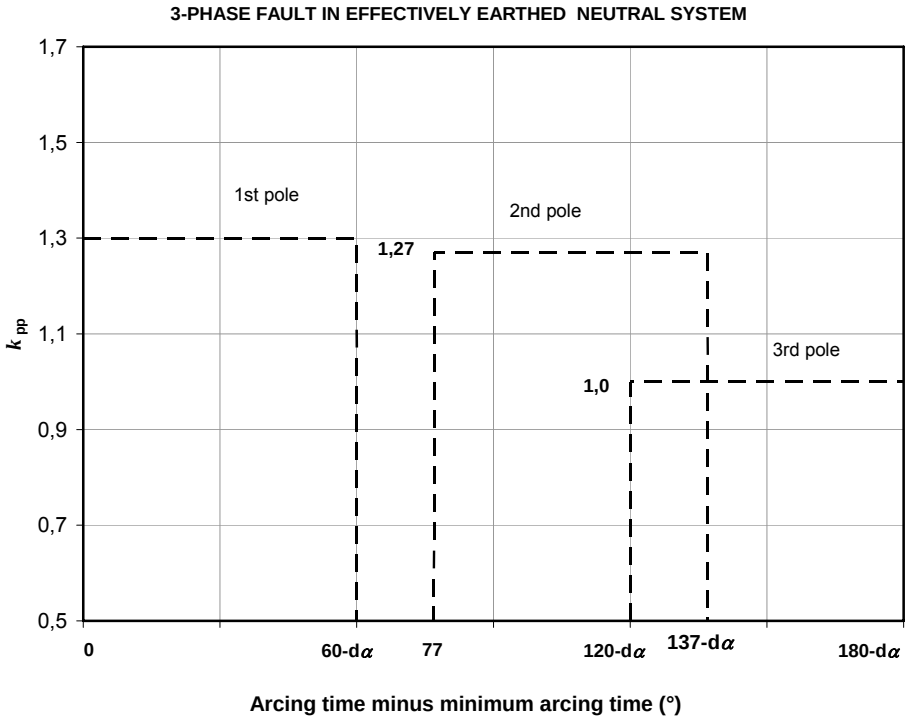
By comparison of Figure 3 with Figure 4 and Figure 5, it can be seen that by performing the duty as a single-phase test in substitution for three-phase tests, the test is more onerous than for three-phase testing. However, in this manner the stresses obtained in three-phase interruptions are fully covered. The number of tests remains at three valid interruptions.

The test procedure according to 6.102.10.2.5 of IEC 62271-100, illustrated by Figure 4 and Figure 5, reproduces exactly the stresses of a three-phase interruption but a greater number of interruptions is required to provide a full demonstration. For k_{pp} = 1,3 nine (not three) tests per test-duty are required and for k_{pp} = 1,5 six (not three) are required. This is because three valid operations are required for demonstration of satisfactory performance for each of the separate phase conditions.



dα=18°

Figure 4 - k_{pp} as a function of arcing time minus minimum arcing time



dα=18°

Figure 5 - k_{pp} as a function of arcing time minus minimum arcing time

3.8 Suitability of a particular short-circuit current rated circuit-breaker for use at an application with a lower short-circuit requirement

Reference is made to 8.101 of IEC 62271-100, with reference to Tables 1a, 1b, 1c, 13 and 14 and the first paragraph of 6.102.1.

The values of short-circuit current ratings of IEC 62271-1 and IEC 62271-100 are taken from the R 10 series of IEC 60059 [2] as given in 4.101.1 of both documents. Subclause 8.101 of IEC 62271-100 states that:

Circuit-breakers which have satisfactorily completed type tests for a combination of rated values (i.e. voltage, normal current, making and/or breaking current) are suitable for any lower rated values (with the exception of rated frequency), without further testing.

The reason for this is related to the combination of the transient-recovery-voltage (TRV) requirements and the current values for the basic short-circuit test duties. This can be demonstrated by using the following example where a circuit-breaker tested for a rated voltage U_r of 420 kV, 50 kA rating is considered for an application requirement of 420 kV, 30 kA.

At 420 kV the T100, T60, T30 and T10 duty TRV values are detailed in Table 14 of IEC 2271-100 and reproduced in an abbreviated form below for convenience.

The circuit-breaker being considered satisfies the TRV peak and rate-of-rise etc. of the duties shown in the upper part of Table 3. Those for the application are shown in a similar form in the lower part of the table and are compared as illustrated by the arrows.

Table 3 - Example of comparison of rated values against application (U_r = 420 kV)

Duty for circuit-breaker (current)	**T100** (50 kA)	**T60** (30 kA)	**T30** (15 kA)	**T10** (5 kA)
TRV peak value	624	669	669	787
Rate of rise	2,0	3,0	5,0	8,9
		↓	↓ ↓	↓ ↓
Duty of application (current)	-	T100 (30 kA)	T60 (18 kA)	T30 (9 kA)	T10 (3 kA)
TRV peak value	-	624	669	669	787
Rate of rise	-	3,0	3,0	5,0	8,9

As can be seen from Table 3, the evidence from the upper part of the table provides significant overlapping evidence for the application shown in the lower part. This is the reason that 8.101 of IEC 62271-100 is acceptable.

A point of caution for users is where the difference between the rating and the requirement is so great that the T10 requirement of the application becomes far removed from the evidence provided by the duty. In such cases discussions may be required with the supplier. These should give consideration to the requirements of 6.107 of IEC 62271-100 regarding critical currents. Additional test evidence may be required.

3.9 Basis for the current and TRV values of the basic short-circuit test-duty T10

This duty is detailed in 6.104.5.5 of IEC 62271-100 and represents a transformer limited fault condition with the circuit-breaker under consideration clearing a fault on the remote side of the transformer. In such circumstances the fault current is limited by the impedance of the transformer to a value, chosen for standardisation purposes, of approximately 10 %. The value of 10 % is historic having been established from system studies and modelling using the typical impedance values of transformers of standardised ratings.

For this duty, the fault-current is restricted by the value of the impedance of the transformer. The TRV is also dominated by the transformer characteristics which give it a (1-cos) wave-shape form. The values given in IEC 62271-100 for amplitude factor, time coordinates and delay line have been established from system studies and modelling during the 1960s and before. The present values are accepted as being adequate for the vast majority of all systems.

It must be recognised that the first-pole-to-clear factor is 1,5 for all rated voltages. As the damping of the TRV oscillation in a high-voltage transformer is less than in a network, an amplitude factor of 1,7 has been standardised except for line systems, with a voltage reduction across the transformer of 0,9 for voltages of 100 kV and above. Thus, the TRV peak u_c for test-duty T10 becomes:

a) for rated voltages below 100 kV

   1) for circuit-breakers in cable systems

      $u_c = k_{pp} \times k_{af} \sqrt{(2/3)} \times U_r$ where k_{af} is equal to 1,7.

   2) for circuit-breakers in line systems

      $u_c = k_{pp} \times k_{af} \sqrt{(2/3)} \times U_r$ where k_{af} is equal to 1,8.

- for rated voltages of 100 kV and above: $u_c = k_{pp} \times k_{af} \sqrt{(2/3)} \times U_r$, where k_{af} is equal to 0,9 × 1,7 = 1,53.

The impedance of some large transformers, and particularly those of present design, have different characteristics to those specified, giving rise to different current and TRV requirements. If users have a specific transformer installation where, by extrapolation between the standard T10 and T30 values, the present characteristics for the controlling circuit-breaker(s) do not adequately cover the site specific requirements, then additional testing may be needed.

3.10 References

[1] IEC 60050 (601): International Electrotechnical Vocabulary - Chapter 601: Generation, transmission and distribution of electricity

[2] IEC 60059: IEC standard current ratings

3.11 Bibliography

E Haginomori et al: TRVs and Fault Clearing Stresses in Extra-high-voltage Radial Networks. Electrical Engineering in Japan Vol. No. 4 1994

A Braun et al. Characteristic Values of the Transient Recovery Voltage for Different Types of Short-circuits in an Extensive 420 kV System. etz-a Volume 97 (1976) pp 489 to 493

P Baltensperger et al.: Transient Recovery Voltage in High Voltage Networks – Terminal Fault. CIGRÉ session paper 13-10, 1968

R G Colclaser Jr., J E Beehler, and T F Garrity. A Field Study of Bus Fault Transient Recovery Voltages. IEEE Trans. PAS 95 (1976), 1769 – 1776.

R Harner and J Rodriguez. Transient Recovery Voltages Associated with Power-system, Three-phase Transformer Secondary Faults. IEEE Transactions, Vol. PAS-91, September/October 1972

P G Parrott: A Review of Transformer TRV Conditions. ELECTRA No. 102 pages 87 – 118.

4 Initial transient recovery voltage (ITRV)

4.1 General

The IEC 62271-100 subclauses relevant to this chapter are:

4.102.2 Representation of TRV

4.102.4 Standard values of ITRV

6.104.5.1 General

6.104.5.2 Test duties T100s and T100a

4.2 ITRV requirements

4.2.1 Basis for specification

Due to travelling waves on the busbar and reflections from the first major discontinuity along the busbar, a high-frequency oscillation occurs which is similar to the one observed on a faulted line under short-line fault conditions. As the busbar is usually on the network side of the circuit-breaker this oscillation, which is called “Initial Transient Recovery Voltage (ITRV)” is superimposed to the very beginning of the terminal fault TRV.

The ITRV is mainly determined by the busbar and line bay configuration of the substation. Compared with the short-line fault, the first voltage peak is rather low, but the time to the first peak is extremely short, that is, within the first 1,5 μs after current zero. Therefore the thermal mode of interruption may be influenced.

CIGRE WG 13-01 studied nearly all the basic network configurations and established the basic considerations with representative figures which served as the basis for ITRV specification [1] [2]:

- the initial part of ITRV depends only on the surge impedance of the connection and on the current;
- based on the dimensions of the busbar and the connections to them a surge impedance of 260 Ω is considered as a good estimate for practical applications with rated voltages up to 550 kV;
- the time to the first peak of ITRV is twice the travelling time of the wave to the main discontinuity. It depends on the dimensions of the substation, which is related to the rated voltage (see Table 4) and thus on the arrangement of the busbar;
- in practice, the main discontinuity is either a division in two branches of the busbar or the presence of a capacitance of more than 1000 pF;
- the velocity of the wave propagation along the busbar was found to be about 260 m/μs.

4.2.2 Applicability

As the ITRV is proportional to the busbar surge impedance and to the current, the ITRV requirements can then be neglected in the following cases:

- for circuit-breakers with a rated short-circuit breaking current of less than 25 kA;
- for circuit-breakers installed in metal enclosed gas insulated switchgear (GIS) because of the low surge impedance;
- for circuit-breakers with a rated voltage below 100 kV because of the small dimensions of the busbars.

4.2.3 Test duties where ITRV is required

As interruption is influenced by ITRV mainly for high values of the short-circuit current, testing under ITRV conditions is required for T100a, T100s and L_{90}.

If the circuit-breaker has a short-line fault rating, the ITRV requirements are considered to be covered if the short-line fault tests are carried out using a line with insignificant time delay, unless both terminals are not identical from an electrical point of view (for instance when an additional capacitance is used).

4.2.4 ITRV waveshape

The ITRV is defined by the voltage u_i and the time t_i. As shown on Figure 12b of IEC 62271-100, reproduced hereafter as Figure 6.

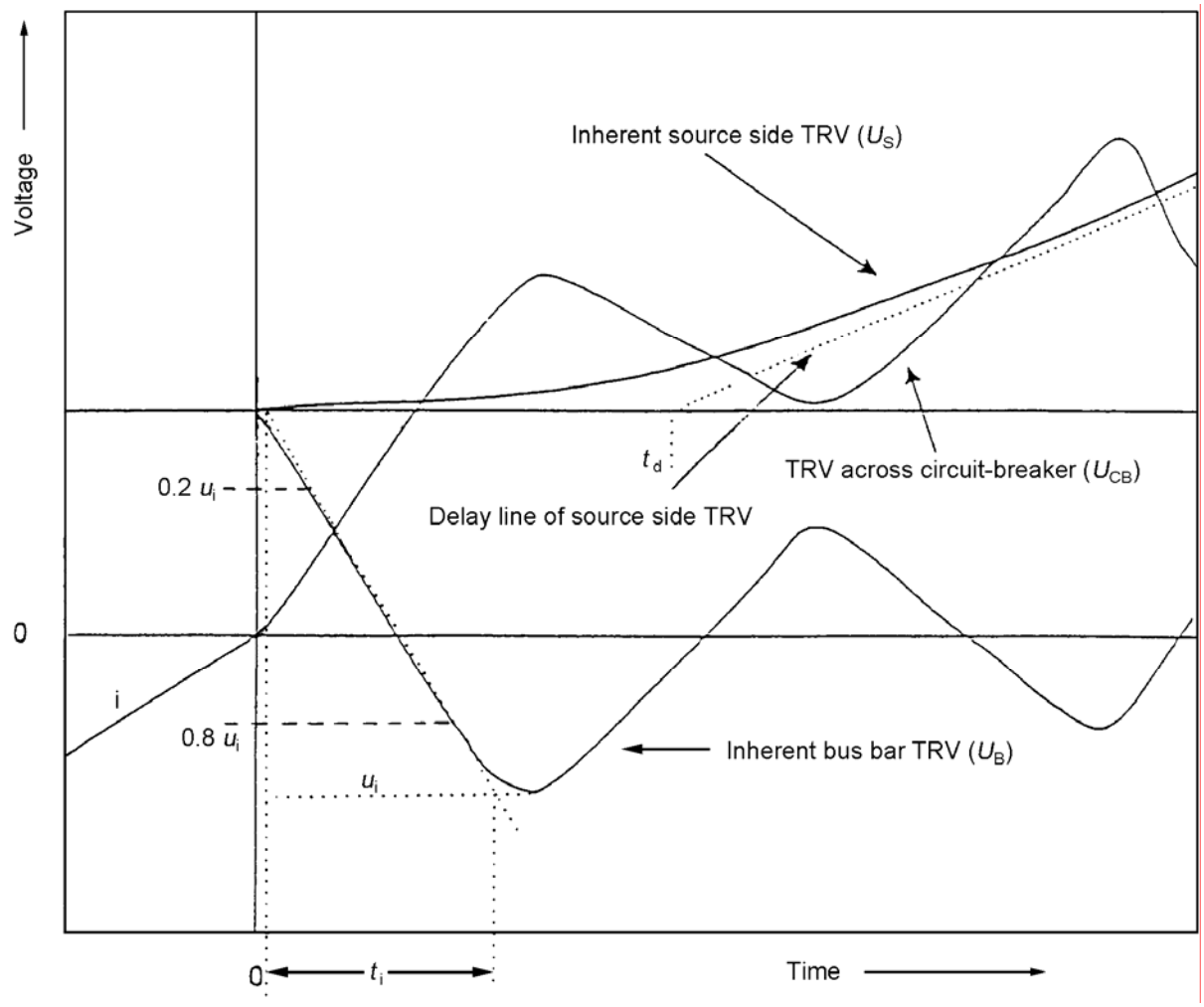


Figure 6 - Representation of ITRV and terminal fault TRV

The rate of rise of the ITRV is dependent on the interrupted short-circuit current and its amplitude depends upon the distance to the first discontinuity along the busbar.

The inherent waveshape shall follow a straight line drawn using the 20 % and the 80 % point of the ITRV peak voltage u_i and the required rate of rise of the ITRV.

4.2.5 Standard values of ITRV

A multiplying factor f_i is used to determine the amplitude of the first peak u_i as function of the r.m.s value of the short-circuit breaking current.

Values of time to peak t_i are given in Table 3 of IEC 62271-100 (reproduced here for convenience of reading as Table 4). These values were developed from the average distances from the breaker to the first discontinuity for the various system voltages [1].

The standard values cover both three-phase and single-phase faults. They are based on the assumption that the busbar, including the elements connected to it (supports, current and voltage transformers, disconnectors, etc.), can be roughly represented by a resulting surge impedance Z_i of about 260 Ω in the case of a rated voltage lower than 800 kV and by a resulting surge impedance Z_i of about 325 Ω in the case of a rated voltage of 800 kV. The relation between f_i and t_i is then:

$$f_i = t_i \times Z_i \times \omega \times \sqrt{2}$$

where

$\omega = 2\pi f_r$ is the angular frequency corresponding to the rated frequency of the circuit-breaker.

Table 4 - Standard values of initial transient recovery voltage - Rated voltages 100 kV and above

Rated voltage	Multiplying factor to determine u_i as function of the r.m.s. value of the short-circuit breaking current I_{sc} [a]		Time
U_r	f_i		t_i
kV	kV/kA		µs
	50 Hz	60 Hz	
100	0,046	0,056	0,4
123	0,046	0,056	0,4
145	0,046	0,056	0,4
170	0,058	0,070	0,5
245	0,069	0,084	0,6
300	0,081	0,098	0,7
362	0,092	0,112	0,8
420	0,092	0,112	0,8
550	0,116	0,139	1,0
800	0,159	0,191	1,1

[a] The actual initial peak voltages are obtained by multiplying the values in these columns by the r.m.s. value of the short-circuit breaking current.

4.3 Testing

4.3.1 ITRV measurement

The ITRV should be handled as for the short-line fault TRV. Consequently it is necessary to measure the inherent ITRV circuit value.

As connections between the ITRV circuit and the supply circuit can also contribute to the initial part of the TRV, the inherent ITRV is that of the complete circuit from the circuit-breaker terminal to the first discontinuity i.e. the delay capacitor. Other contributions from the supply

circuit, apart from ITRV and the normal two or four parameters TRV, must be damped by appropriate RC circuits.

As ITRV is characterized by a very high frequency in the MHz range, caution is recommended when measuring its inherent value. Diodes used in current injection methods must have short characteristic times (duration during which it differs notably from an ideal circuit-breaker), otherwise measurement could show a falsely damped ITRV with reduced RRRV [6].

The inherent waveshape shall mostly follow a straight reference line drawn from the beginning of the ITRV to the point defined by u_i and t_i. The inherent ITRV waveshape shall follow this reference line from 20 % to 80 % of the required ITRV peak value (see Figure 6) Deviations from the reference line are permitted for an ITRV amplitude below 20 % and above 80 % of the specified ITRV peak value.

4.3.2 SLF with ITRV

Where short-line fault duties are to be performed, it may be convenient to combine the ITRV and SLF requirements in the line side circuit.

Figure 7 shows a typical graph of line and source side TRV in the case of line side TRV with time delay and source side with ITRV.

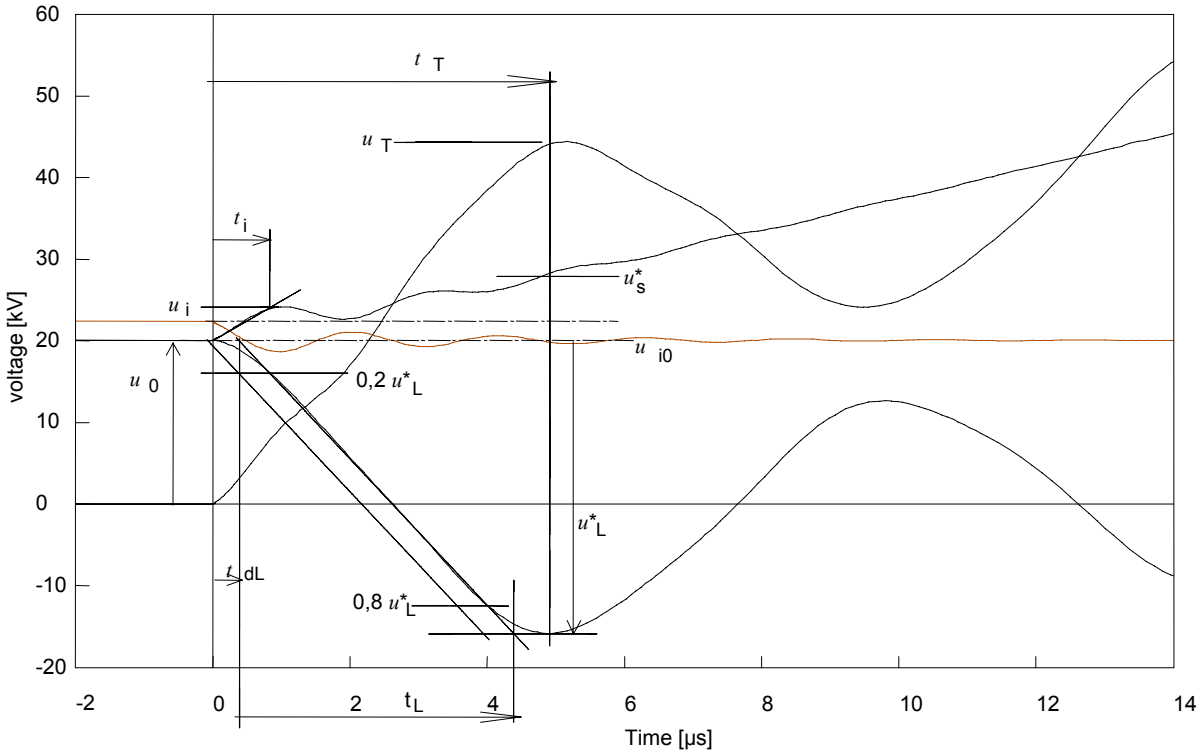


Figure 7 - Typical graph of line side TRV with time delay and source side with ITRV

The first peak voltage across the circuit-breaker (u_T) is equal to sum of the line side TRV (u_L^*) and the source side TRV (u_S^*). Annex A of IEC 62271-100 gives the calculation of these TRVs.

When the ITRV is combined with the transient voltage of a short line having a time delay t_{dL} as specified in Table 4 of IEC 62271-100, the total stress is, for practical considerations, considered to be equal to the stress of a short line with insignificant time delay.

Figure 8 shows a comparison between the inherent TRV specified for SLF with ITRV and the inherent TRV obtained for SLF when a line with insignificant time delay is used, for test duty L_{90} based on 145 kV, 31,5kA.

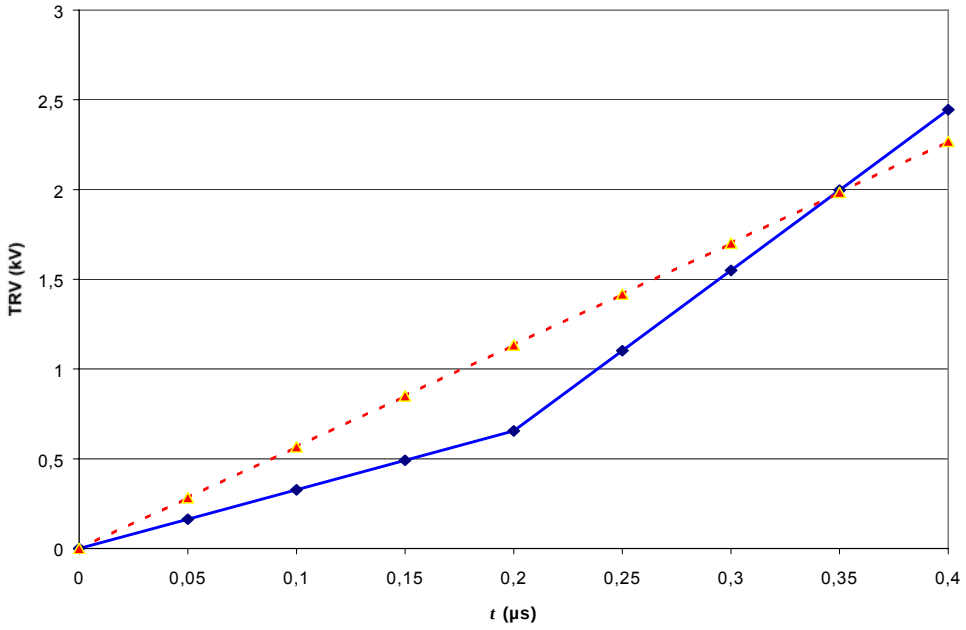


Figure 8 - Comparison of TRV for SLF with time delay and ITRV (solid line) and SLF with insignificant time delay (dotted line), from current zero to the first TRV peak

Further justification of the equivalence can be found in [3].

4.3.3 Unit testing

As for SLF, ITRV circuit inductance must be divided by the number of breaks in series while time t_i is unchanged.

If the circuit breaker has distribution capacitors, one capacitor shall be put in parallel to the unit under test.

4.4 References

[1] G. Catenacci and CIGRE WG13-01, Contribution on the study of the initial part of the Transient recovery Voltage, Electra 46 (1976), p. 39

[2] C.Dubanton, Initial Transient Recovery Voltage, Current Interruption in High-Voltage Networks, Plenum Publishing Corporation, 1978, pp 185 – 203

[3] W.Hermann, K.Ragaller, Interaction between arc and network in the ITRV regime, Current Interruption in High-Voltage Networks, Plenum Publishing Corporation, 1978, pp 205 – 229

[4] B.Calvino et al., Quelques aspects des containtes supportées par les disjoncteurs HT à la coupure d'un court-circuit, CIGRE session paper 13-08 (1974)

[5] C. Guilloux, Y. Therme, P.G. Scarpa: Measurement of post arc current in H.V. circuit breakers. Application to short circuit tests with ITRV. IEEE Trans. on Power Delivery, vol.8 (1993), No.3, pp. 1148-1154

[6] R. Graf: ITRV modification by interaction between SF_6-breaker and the test circuit. CIGRE session paper 13-01 (1976).

5 Short-line faults

5.1 General

The IEC 62271-100 subclauses relevant to this chapter are:

4.105 Characteristics for short-line faults

6.109 Short-line fault tests

Annex A Calculation of transient recovery voltages for short-line faults from rated characteristics

5.2 Short-line fault requirements

5.2.1 Basis for specification

5.2.1.1 General

Short-line fault (SLF) tests are made to prove the capability of a line circuit-breaker to break faults which occur from a few hundred meters up to several km down the line. They are due to numerous causes such as lightning, tree interfering with a line, etc.

These faults are characterised by a high short-circuit current and a rate of rise of the transient recovery voltage (RRRV) which is generally much higher than the values specified for other tests duties. The transient recovery voltage (TRV) applied to the circuit-breaker is a combination of a source side component, with a RRRV comparable to the value required for terminal fault tests, and a high frequency line side component.

The latter is caused by a travelling wave. This is initiated at the moment of current interruption and sent into the line to be reflected at the fault. The reflected wave is of triangular wave-shape and has a high RRRV which is imposed on the circuit-breaker open contacts on the line side.

The RRRV and the amplitude of the line side TRV as well as the magnitude of the short-circuit current depend on the distance of the fault location from the circuit-breaker, as well as the rated voltage and the source-side conditions.

In standardisation it has been found advantageous to define the stress on the circuit-breaker in case of SLF by the relation between the corresponding short-circuit current I_L and the terminal fault current I_{sc} of T100 for the same source-side conditions: For example, in case of the 90 % short-line fault test duty L_{90}: $I_L = 0{,}9 \times I_{sc}$.

L_{90} corresponds to a fault distance of a few hundred meters to less than 2 km, the 75 % short-line fault test duty L_{75} to 1 to 5 km.

An SLF interrupting capability is required for circuit-breakers designed for direct connection to overhead lines in systems having a rated voltage of 52 kV and above and a rated short-circuit current higher than 12,5 kA. This is explained below in the technical comment.

When required, SLF test duties are applicable to all types of circuit-breakers, regardless of their interrupting medium or technology. They must break short-line faults occurring at any practical value of line length. As explained in SLF testing (5.3.2.1) the range of currents

specified is such that critical values for all kinds of interrupting medium and circuit-breaker technologies are likely to be covered.

The procedure to calculate the line side and source side transient recovery voltages under conditions of a short-line fault is described in detail in Annex A of IEC 62271-100.

5.2.2 Technical comment

For rated short-circuit currents lower than or equal to 12,5 kA the requirements, in terms of RRRV and current (or di/dt) are considered to be covered by the basic terminal fault test duties.

For example, during SLF test duty L_{90} a circuit-breaker rated 100 kV, 12,5 kA – 50 Hz would have to withstand a RRRV of 2,25 kV/µs while interrupting 11,25 kA (di/dt = 5 A/µs). Under terminal fault test duty T100 at 100 % of 12,5kA (di/dt = 5,5 A/µs) it is tested to withstand a RRRV of 2 kV/µs.

For voltages lower than 52 kV the situation is discussed in CIGRE Technical Brochure 134 [1] where it is recognised that the majority of connections to line circuits is made via cables, and in these systems SLF tests are generally not necessary. In the case of systems with overhead lines connected directly to the circuit-breaker without any length of cable, it is recommended to verify the SLF interrupting capability of the circuit-breaker.

5.2.3 Single-phase faults

SLF testing of circuit-breakers is based on single-phase faults because these faults are by far the most frequent. In addition, in effectively earthed systems, it corresponds to the condition of the last pole-to-clear which is the more severe condition for a three-phase fault.

This test condition covers also the case of the first-pole-to-clear a three-phase fault in non-effectively earthed systems.

5.2.4 Surge impedance of the line

5.2.4.1 Surge impedance selection

For standardisation purposes a surge impedance of 450 Ω adequately covers all practical values.

5.2.4.2 Technical comment

The surge impedance is a function of many characteristics of a line (diameter, number, spacing, height of conductors), circuit configuration (single or double), earth resistivity and presence/type of earth wire.

For a symmetrical transmission line, this surge impedance is related to the positive and zero sequence surge impedances in the following way:

$$Z = \frac{2Z_1 + Z_0}{3} \qquad (3)$$

with

Z_1 = positive sequence surge impedance;

Z_0 = zero sequence surge impedance.

Typical values are given in Appendix A of this chapter.

Appendix B of this chapter shows that for single circuit arrangements, the surge impedance is maximum when a pole clears when the others are already opened. This is also the case for double circuit constructions.

On a line that uses bundled sub-conductor phase construction, the sub-conductors of a faulted phase are attracted together to constrict the effective diameter of the bundle during fault conditions. This changes the line impedance for that phase during the duration of the fault. This fact has been taken into account when evaluating and standardising the value of surge impedance.

Calculations performed on 420 kV lines have shown that the surge impedance is between 434 Ω and 456 Ω when bundle contraction during fault is considered [2].

Therefore, in the 4th edition of IEC 60056 a single value of 450 Ω was standardised independent of the number of conductors per phase as short-circuit conditions were similar to those of a single conductor line.

Even though values for single conductor lines could be found to be slightly higher, a surge impedance of 450 Ω adequately covers all practical cases because when evaluating SLF parameters only the worst conditions are considered [3].

- three-phase short-line fault at a critical distance;
- it is assumed that the supply has a single-phase short-circuit current equal to 100 % of the rated (3-phase) short-circuit current. In practice this is unlikely to happen as 100 % generation is generally not available and the single-phase short-circuit current is in many cases lower than the three-phase short-circuit current (see 5.3.5);
- in addition it is assumed that the impedance of earth return is negligible, whereas in practice this impedance effectively reduces the short-circuit current and the rate-of-rise of recovery voltage.

5.2.5 Peak voltage factor

5.2.5.1 Definition and selection of value

The peak factor (k) is the ratio of amplitudes of the first peak of the TRV on the line side (u_L*) to the peak voltage at the circuit-breaker terminals prior to interruption (u_0) (see Figure 16 of IEC 62271-100).

As shown hereafter and in Appendix B, the standardised value of 1,6 adequately covers all practical values.

5.2.5.2 Technical comment

The peak factor (k) is given by:

$$k = \frac{u_L^*}{u_0} \qquad (4)$$

The rate of rise of recovery voltage on the line side is equal to the product $Z \times \frac{\mathrm{d}i}{\mathrm{d}t}$,

where

Z surge impedance;

$\frac{\mathrm{d}i}{\mathrm{d}t} = \omega \times I_L \times \sqrt{2}$ current derivative before interruption.

The time to the first peak u_L* is equal to two times the reflection time from the circuit-breaker to the fault point (time necessary for the travelling wave to reach the fault and be reflected back to the circuit-breaker):

$$\frac{2\lambda}{v} = t_L$$

with:

- λ distance from the opening circuit-breaker to the fault;
- v velocity of light.

The rate-of-rise of recovery voltage is then given by:

$$\frac{u_L^*}{t_L} = Z\frac{\mathrm{d}i}{\mathrm{d}t}$$

It follows that the first peak of the line side TRV is given by:

$$u_L^* = Z\frac{\mathrm{d}i}{\mathrm{d}t} \times \frac{2\lambda}{v} \tag{5}$$

$$u_0 = X_L \times \lambda \times I_L\sqrt{2} \tag{6}$$

with X_L line reactance per unit length.

From Equations (4), (5) and (6):

$$k = \frac{2\omega Z}{X_L \times v} \tag{7}$$

$$X_L = \frac{(2L_{1w} + L_{0w})\omega}{3} \tag{8}$$

with

L_{1w} positive sequence power frequency line inductance per unit length;

L_{0w} zero sequence power frequency line inductance per unit length.

$$Z_1 = \sqrt{\frac{L_1}{C_1}} \tag{9}$$

$$v = \frac{1}{\sqrt{L_1 C_1}} \tag{10}$$

with

L_1 high-frequency positive sequence line inductance per unit length

C_1 high-frequency positive sequence line capacitance per unit length

From Equations (9) and (10):

$$\frac{Z_1}{v} = L_1 \qquad (11)$$

Combining Equation (7) with Equation (3), (8) and (11) gives:

$$k = \frac{2L_1(2 + \frac{Z_0}{Z_1})}{2L_{1w} + L_{0w}} \qquad (12)$$

If the high-frequency inductance L_1 is equal to the power frequency inductance of the line L_{1w}, Equation (12) simplifies to:

$$k = \frac{2(2 + \frac{Z_0}{Z_1})}{2 + \frac{L_{0w}}{L_{1w}}} \qquad (13)$$

if $\frac{L_{0w}}{L_{1w}} = 3$ is assumed for high-voltage networks,

$$k = 0{,}4(2 + \frac{Z_0}{Z_1}) \qquad (14)$$

In practice the high frequency inductance L_1 is lower than the power frequency value L_{1w}, and losses which are always present have been neglected in the calculation. For these reasons the peak factor obtained by Equation (13) is a conservative value.

Appendices A and B of this chapter give values of peak factors calculated for HV networks 72,5 kV to 550 kV. All the values obtained are equal or lower than 1,55. The specified value of 1,6 is therefore conservative.

5.2.6 Rate-of-Rise of Recovery Voltage (RRRV) factor "*s*"

The RRRV on the line side is given by $Z\frac{\mathrm{d}i}{\mathrm{d}t}$ or $Z \times \omega \times I_{\mathrm{L}}\sqrt{2}$. For practical applications it is sometimes useful to express the RRRV as follows:

RRRV $= s \times I_{\mathrm{L}}$, with $s = Z \times \omega\sqrt{2}$ and $\omega = 2\pi f_r$

For rated frequencies (f_{r}) of 50Hz and 60Hz, and with Z= 450 Ω, the RRRV factor s is then equal to:

f_{r} = 50 Hz s = 0,20 kV/μskA

f_{r} = 60 Hz s = 0,24 kV/μskA

5.2.6.1 Operating sequence

SLF is mainly a single-phase fault on a line. During network operation the fault is cleared by a circuit-breaker performing its rated operating duty: an auto-reclosing duty as usual for overhead line networks.

In order to reproduce service conditions, IEC 62271-100 requires circuit-breakers to perform their rated operating duty during testing.

5.3 SLF testing

5.3.1 Test voltage

As SLF tests are based on single-phase faults, the test voltage is equal to the phase to earth voltage i.e. the rated voltage divided by $\sqrt{3}$, with a first-pole-to-clear factor k_{pp} = 1,0.

5.3.2 Test duties

5.3.2.1 General

The severity of SLF tests depends on the position of the fault along the line length as it determines the magnitude of the current (and di/dt) and the transient recovery voltage characteristics: RRRV (proportional to di/dt) and first peak value (proportional to the reflection time from the circuit-breaker to the fault). Circuit-breakers must break short-line faults with any practical values of line length corresponding to fault currents ranging from tens of percent to about 90 % of the rated short-circuit current.

For example for a 145 kV, 40 kA, 60 Hz circuit-breaker, a short-line-fault test at 90 % of the rated short-circuit current corresponds in practice to a fault on the line occurring 330 m away from the circuit-breaker.

The critical percentage of short-circuit current is dependent on the interrupting medium of the circuit-breaker.

An arc in SF_6 has a very short time constant (less than 0,5 µs) i.e. its resistance or conductance changes rapidly during the transient recovery period. Therefore interruption is affected by the very high frequencies of TRV met in L_{90} test duty and the associated high values of the short-circuit current [4].

An arc in high pressure air has a longer time constant (typically 10 times the value in SF_6), so interruption is mostly affected by the lower frequencies and higher amplitudes met in L_{75}.

Other technologies such as oil or vacuum circuit-breakers have proved to be insensitive to short-line fault conditions, as long as they have the corresponding terminal fault breaking capability.

In order to cover the possible critical values of short-circuit current, two ranges of currents are specified for short-line fault tests, in percentage of the rated short-circuit current:

test duty L_{90} with 90 % (-0 %, +2 %) of I_{sc};

test duty L_{75} with 75 % (-4 %, +4 %) of I_{sc}.

If there is a significant increase of arcing time when the current is reduced from 90 % I_{sc} to 75 % I_{sc}, an additional series of tests with 60 % (± 5 %) I_{sc} is required to confirm that there is no critical current in the 60 % to 75 % region.

5.3.2.2 Technical comment

Compared to terminal fault conditions and assuming the same source side impedance as in the case of a 100 % terminal fault (T100) the short-circuit current in a short-line fault is lower as the line between circuit-breaker and fault introduces an additional impedance into the total circuit.

Standard values of the current I_L related to line length are specified corresponding to a reduction of the a.c. component of the rated short-circuit current to 90 % (L_{90}) and 75 % (L_{75}).

In IEC 62271-100 the line length has been standardised.

As the line length represented in a test may differ from the standardised value, within a tolerance given in Annex B of IEC 62271-100, the short-circuit current during tests may vary in the following ranges:

L_{90}: I_L = 90 % of I_{sc} (line length = standardised value)

I_L = 92 % of I_{sc} (line length = standardised value - 20%)

L_{75}: I_L = 71 % of I_{sc} (line length = standardised value + 20%)

I_L = 79 % of I_{sc} (line length = standardised value - 20%)

In cases (see c) of 6.109.4 of IEC 62271-100) where a test duty L_{60} is required:

L_{60}: I_L = 55 % of I_{sc} (line length = standardised value + 20%)

I_L = 65 % of I_{sc} (line length = standardised value - 20%)

These values are derived from calculations given in Appendix C of this chapter.

5.3.3 Test current asymmetry

5.3.3.1 General

The test current is symmetrical at contact separation (with a d.c. component less than 20 %) because the most severe condition is obtained in the thermal phase of interruption when the current derivative ($\frac{di}{dt}$) and the RRRV ($Z\frac{di}{dt}$) are maximum.

5.3.3.2 Technical comment

It is recognised that lightning strikes are the most likely events leading to a short-line fault. As these are random events in relation to the point on the voltage cycle they will generally lead to asymmetrical currents. However the d.c. component of this current decreases more rapidly for a line fault than for other faults due to the high value of resistance in the earth return circuit. Therefore for the most likely system condition giving SLF, although asymmetrical at initiation, will approach the symmetrical condition or at least a low degree of asymmetry, by the time of current interruption by the circuit-breaker.

Based on the above SLF breaking tests need not be asymmetrical. As a result the simpler test regime of symmetrical testing has been standardised on for this duty.

SLF breaking tests with asymmetrical currents are also not required because when compared with symmetrical conditions, the $\frac{di}{dt}$ at current zero and RRRV (= $Z\frac{di}{dt}$) applied on circuit-breakers are reduced.

5.3.4 Line side time delay

The local capacitance always present in a substation between the circuit-breaker and the line introduce a time delay t_{dL} in the initial part of the line side TRV. This capacitance represents the typical capacitance that can be met in actual networks. It is for example introduced by supports and stray capacitance of the connection between the circuit-breaker and the faulted line.

For rated voltages equal and lower than 170 kV, the time delay t_{dL} is standardised to 0,2 µs.

For rated voltages equal to and higher than 245 kV, it is standardised to 0,5 µs.

These values correspond to a line side phase to earth capacitance C_{dL} equal to 445 pF and 1110 pF, respectively.

NOTE In order to cover the ITRV requirement, where it is specified on the supply side (see 6.104.5.2 and 6.109.3 of IEC 62271-100), the SLF tests are generally performed with an insignificant time delay (less than 0,1 µs) on the line side. ITRV specification is not applicable to circuit-breakers in Gas Insulated Substations.

5.3.5 Supply side circuit

5.3.5.1 Supply side circuit definition

The short-circuit impedance of the supply side circuit is such that the rated short circuit current is obtained in terminal fault conditions. This is due to the fact that the single-phase short-circuit current is assumed to be equal to the three-phase short-circuit current.

The supply side RRRV is equal to the RRRV specified for three-phase faults.

The supply side TRV is adjusted to obtain the crest value according to the first-pole-to-clear factor 1,0 and amplitude factor 1,4. The RRRV of 2,0 kV/µs is retained. The time parameters (t_3 or t_1 and t_2) are adjusted accordingly.

5.3.5.2 Technical comment

System studies have shown that the supply side RRRV is, as a first approximation, equal to the RRRV defined for three-phase faults [5]. Such an approximation is justified as the RRRV is equal to the product $Z\frac{\mathrm{d}i}{\mathrm{d}t}$, with the supply side surge impedance Z and the current derivative ($\frac{\mathrm{d}i}{\mathrm{d}t}$) having similar values for single-phase and three-phase conditions.

Generally speaking the supply side RRRV for single-phase faults is slightly lower than for three-phase faults. This has been supported by TRV studies in 420 kV networks [5]. However, as there is a large scatter of values, the RRRV for a single phase terminal fault, corresponding to the supply side TRV in the case of a short-line fault, has been standardised to be the same value 2 kV/µs for rated voltages equal or higher than 100 kV as defined for three-phase faults.

During a SLF breaking operation, the voltage at the circuit-breaker terminals at current zero is equal to the voltage drop on the faulted line and is not zero as would be the case under terminal fault conditions. It follows that the TRV voltages on the supply side during SLF interruption are accordingly lower than the inherent values defined previously.

During test duties L_{90} and L_{75}, and neglecting the influence of the circuit-breaker, the source side TRV peak is reduced by a factor 1,36/1,4 and 1,30/1,4, respectively. The derivation of TRV peak values is explained in Annex A of IEC 62271-100.

5.4 Additional explanations on SLF

5.4.1 Surge impedance evaluation

5.4.1.1 General

The surge impedance is the ratio of the TRV slope ($\frac{\mathrm{d}u}{\mathrm{d}t}$ or RRRV) divided by the current derivative $\frac{\mathrm{d}i}{\mathrm{d}t}$. The RRRV is defined as the slope between the points corresponding to 20 % and 80 % of the line side TRV peak of the inherent test circuit response.

5.4.1.2 Technical comment

In the case of very short lines between the opening circuit-breaker and the fault, with t_L < 5 t_{dL}, the wave shape of the line side TRV is deformed and cannot be compared to a triangular shape with an initial time delay.

The curves presented in Appendix D to this chapter show that for a correct evaluation of the surge impedance it is necessary to define the rate of rise of the line side recovery voltage as the slope between the points corresponding to 20 % and 80 % of the peak voltage, as in this region the shape is not influenced by the time delaying capacitance.

Although the previous 10 % to 90 % method leads also to correct values where $t_L \geq 5t_{dL}$, this 20 % to 80 % method is generalised for the evaluation of inherent line side TRVs in the 1st edition of IEC 62271-100.

5.4.2 Influence of additional capacitors on SLF interruption

5.4.2.1 General

Additional capacitance connected between the circuit-breaker terminals (grading capacitor or capacitor used to assist the interruption) or line-to-earth, has two effects:

- it decreases the oscillation frequency and the RRRV of the line side TRV;
- it increases the time delay of the line side TRV.

Both effects tend to ease the interruption, and capacitors are sometimes used to increase the short-line fault breaking capability of circuit-breakers.

Historically resistors where used in air-blast circuit-breakers resistors to reduce the RRRV and facilitate the interruption. RRRV is reduced by a factor $\frac{R}{R+Z}$ where R is the resistor value and Z the surge impedance of the line.

5.4.2.2 Reduction of the line side RRRV by a phase to earth capacitor

As SF_6 circuit-breakers are more sensitive to the initial part of the TRV (first μs) the use of additional capacitors has proved to be more efficient.

When capacitors mounted across the circuit-breaker terminals are used to meet a SLF breaking capability, caution is recommended as high values of capacitance could lead to ferro-resonance with electromagnetic instrument transformers connected between the circuit-breaker and a de-energised line or connected to a supposedly de-energised bus.

If the capacitor is connected phase to earth on the line side, the reduction of the line side RRRV can be estimated by a simple calculation:

Definitions:

C_{add} additional line-to-earth capacitance;

L line inductance;

Z line surge impedance;

C_L total line capacitance = $\frac{L}{Z^2}$;

C_e equivalent line capacitance.

The equivalent line capacitance C_e is defined as the capacitance which, together with the inductance L, gives the line frequency of oscillation:

$$f_{\mathrm{L}} = \frac{1}{2\pi\sqrt{LC_{\mathrm{e}}}} \qquad (15)$$

The period of oscillation is equal to $\frac{2u_{\mathrm{L}}^{*}}{\left(\frac{\mathrm{d}u}{\mathrm{d}t}\right)_{\mathrm{L}}}$ with:

$u_{\mathrm{L}}^{*} = 2X_{\mathrm{L}} \times I_{\mathrm{L}}\sqrt{2}$ and $\left(\frac{\mathrm{d}u}{\mathrm{d}t}\right)_{\mathrm{L}} = Z \times \omega \times I_{\mathrm{L}}\sqrt{2}$

It follows that:

$$f_{\mathrm{L}} = \frac{Z \times \omega}{4X_{\mathrm{L}}} \qquad (16)$$

From (15) and (16):

$$C_{\mathrm{e}} = \frac{4L}{\pi^2 \times Z^2} = \frac{4C_{\mathrm{L}}}{\pi^2} = 0{,}4C_L \qquad (17)$$

If an additional capacitance is added at the line entrance, the RRRV on the line side is reduced in the same manner as the line frequency of oscillation:

$$\frac{\mathrm{d}u}{\mathrm{d}t} = Z \times \omega \times I_{\mathrm{L}}\sqrt{2}\,\frac{2\pi\sqrt{LC_{\mathrm{e}}}}{2\pi\sqrt{L(C_{\mathrm{e}} + C_{\mathrm{add}})}}$$

Using (17) gives:

$$\frac{\mathrm{d}u}{\mathrm{d}t} = Z \times \omega \times I_{\mathrm{L}}\sqrt{2}\,\frac{\sqrt{C_{\mathrm{L}}}}{\sqrt{C_{\mathrm{L}} + 2{,}5C_{\mathrm{add}}}}\text{, or } \frac{\mathrm{d}u}{\mathrm{d}t} = Z \times \omega \times I_{\mathrm{L}}\sqrt{2}\sqrt{\frac{C_{\mathrm{L}}}{C_{\mathrm{L}} + 2{,}5C_{\mathrm{add}}}} \qquad (18)$$

with $C_{\mathrm{L}} = \frac{L}{Z^2}$

Equation (18) can be used in practice to estimate the effect of a phase-to-earth capacitance C_{add} on the line side rate of rise of recovery voltage.

The method presented in Appendix D of this chapter can also be used to evaluate the effect of a capacitance on the line side TRV in more detail. The time delay t_{dL} is calculated by taking into account the total capacitance on the line side, i.e. line capacitance plus additional capacitance from the circuit-breaker (see Figure 9).

The reduction of the line side RRRV by a phase to earth capacitor is especially important to be reproduced in synthetic testing where the capacitor must be installed in parallel to the line. If, for practical reasons the capacitor is connected in parallel to the circuit-breaker, then its value shall be calculated (by Alternative Transient Program or equivalent) to produce an equivalent TRV.

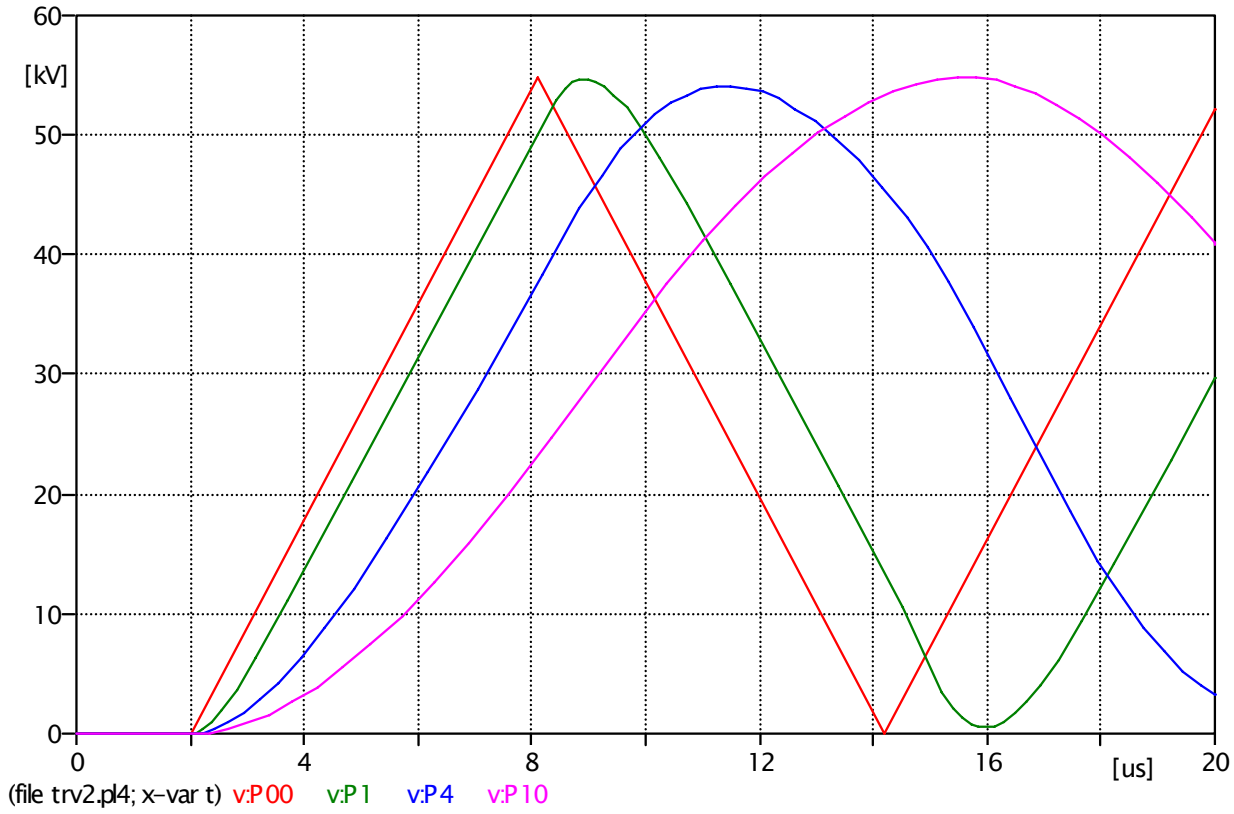


Figure 9 - Effects of capacitor size on the short-line fault component of recovery voltage
Fault 915 m from circuit-breaker
Parallel capacitance C_{add} = 0 – 1,11 – 4,44 and 11,1 nF

5.4.2.3 Influence of the location of phase-to-earth capacitors

In a substation it can be advantageous to take into account the existing phase-to-earth capacitances between the circuit-breaker and the line (such as cables, GIS bus, CVTs) in order to define the necessary additional value of the phase-to-earth capacitor which has to be delivered with the circuit-breaker. However caution is recommended if the circuit-breaker is to be moved to a different location.

For maximum effectiveness the capacitor should be close to the circuit-breaker terminal.

CVTs due to their inherent capacitance have an influence on the TRV, but as shown in Figure 10, taken from [6], caution is necessary because to be of benefit they shall be close enough to the circuit-breaker to influence current interruption. Figure 10 shows that if the capacitor is located too far from the circuit-breaker, the time delay of the recovery voltage is decreased and the amplitude of the first voltage jump is increased, both effects resulting in a lowering of the benefit of the capacitance to the circuit-breaker interruption capability.

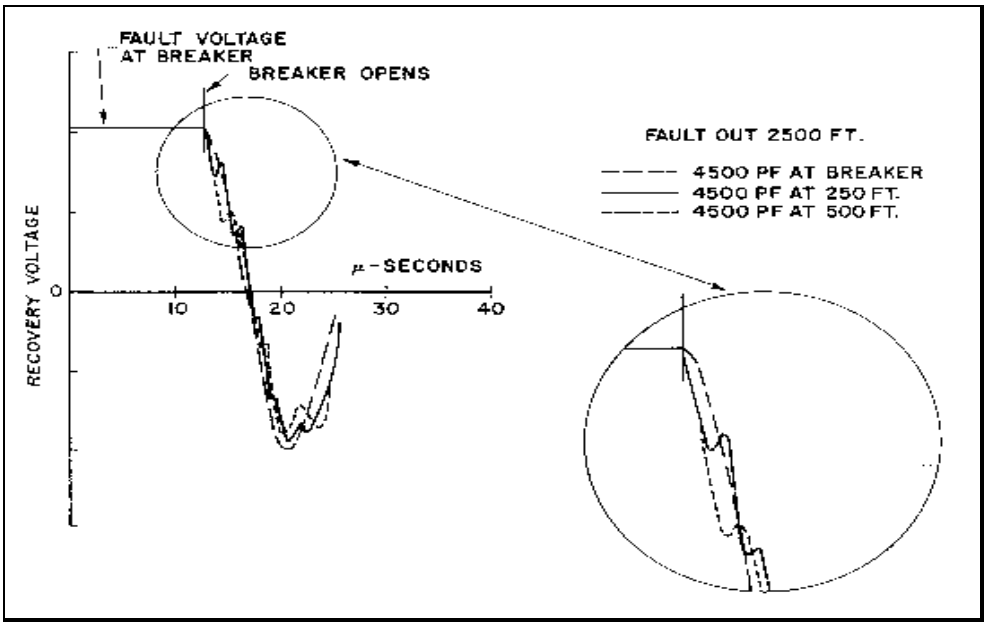


Figure 10 - Effect of capacitor location on short-line fault component of transient recovery voltage. Fault 760 m from circuit-breaker. Capacitor 0 – 76 m – 152 m from circuit-breaker

5.4.2.4 Relative influence of phase to earth and parallel capacitors

When circuit-breakers are fitted with capacitors between terminals (grading capacitors for example) the frequency of the line side oscillation is reduced in a similar way as with a phase to earth capacitor, but the effect of a given value of capacitance is different as the TRV is affected on both sides of the circuit-breaker. A lower value of capacitor is needed to obtain a given reduction of the TRV if it is connected between the terminals instead of phase-to-earth.

Figure 11 shows the inherent TRV obtained during a L_{90} test duty on a 145 kV, 50 kA, 60 Hz circuit-breaker with an additional capacitor of 3 nF connected phase-to-earth (curve 1: maximum slope from the instant of interruption = 6,91 kV/μs) or between terminals (curve 2: maximum slope from the instant of interruption = 6,18 kV/μs).

As the effects of parallel (between terminals) or phase-to-earth capacitors are not the same, it is important to indicate in the type test report the position of any additional capacitor. The relevant capacitance is the one measured at the circuit-breaker line side terminal. The capacitance used for measurements is already taken into account in the adjustment of the line side TRV.

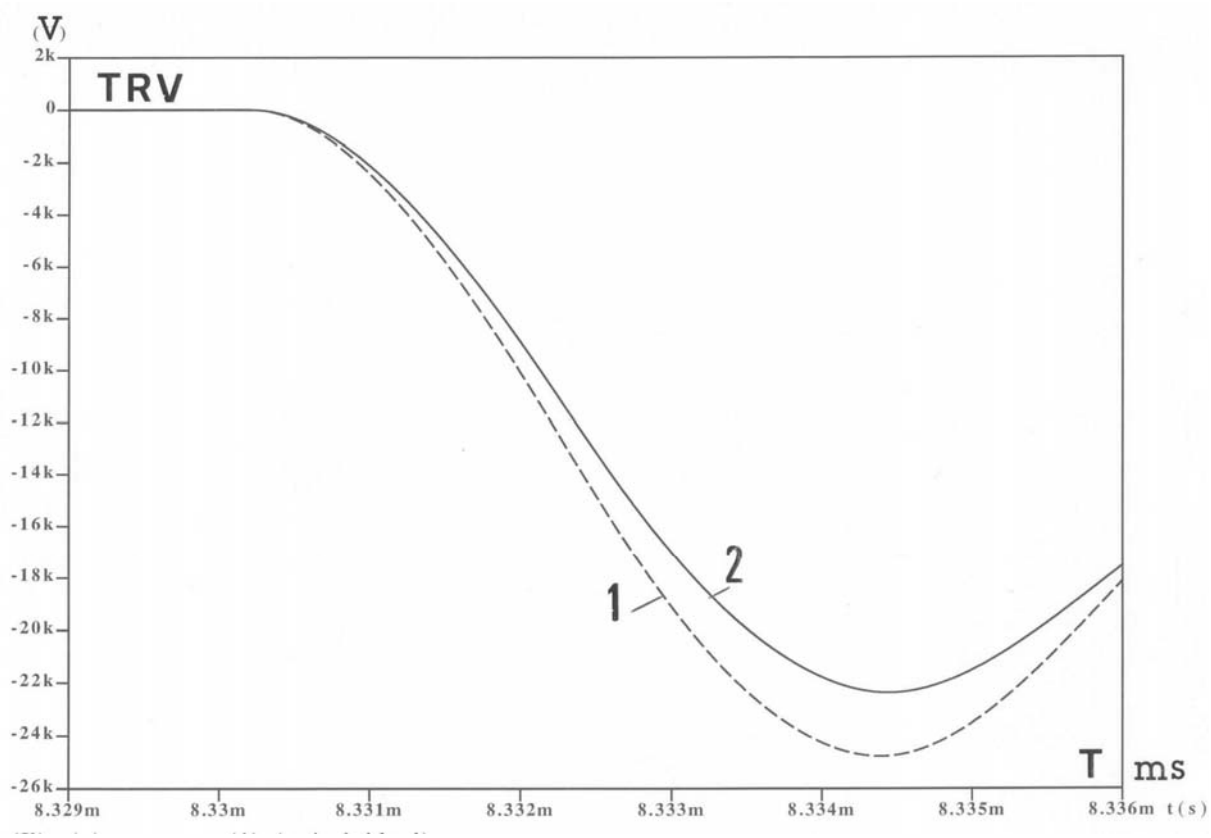


Figure 11 - Inherent TRV obtained during a L_{90} test duty on a 145kV, 50kA, 60Hz circuit-breaker with an additional capacitor of 3 nF connected phase-to-earth (curve 1) or between terminals (curve 2)

5.5 References

[1] CIGRE Technical Brochure 134.

[2] Ch. Dubanton, G. Gervais, Van Nielen. Surge impedance of overhead lines with bundle conductors during short-line faults, Electra N°17, April 1971

[3] Dr H.Meyer, Chairman of CIGRE Study Committee 3. Communication dated 19th August 1963 to the Central Office of the IEC, regarding short-line fault problems; 17A (CIGRE)1, September 1963.

[4] CIGRE WG 13-01. Practical application of arc physics in circuit-breakers. Survey of calculation methods and application guide, Electra N°118, May 1988

[5] A.Braun, K.H. Hinterthür, H.Lipken, B.Stein, O.Völcker. Characteristic values of the transient recovery voltage for different types of short circuits in an extensive 420kV system, ETZ-a vol 97 (1976) pp 489 to 493

[6] R.G.Colclaser, L.E.Berkebile & D.E.Buettner. The effect of capacitors on the short line fault component of TRV; IEEE Trans. Power Apparatus and Systems Vol. PAS 90, N°02 March-April 1971, pp. 660-669

5.6 Bibliography

ANSI/IEEE Standards C37.04 (IEEE Standard Rating Structure for AC High-Voltage Circuit-Breakers), Clause 5.11.4.2; and C37.09 (IEEE Standard Test Procedure for AC High-Voltage Circuit-Breakers), Clause 4.6.5.4

A. Greenwood. Electrical Transients in Power Systems (book), 2nd Edition, John Wiley & Sons Inc. 1991, Chapter 9.7.3

C. H. Flurscheim (Ed.). Power circuit breaker theory and design (book), Peter Peregrinus Ltd., 2nd Edition 1982, Chapter 3.3.2

E. Bolton, D. Birthwhistle, P. Bownes, M.G. Dwek, G.W. Routledge. Overhead-line parameters for circuit-breaker application, Proc. of the IEE, power, vol. 120, No. 5, 1973, pp 561 to 573

R.G. Colclaser, Jr., J.E. Beehler, T.F. Garrity. A field study of the short-line fault component of transient recovery voltage, IEEE Trans. Power Apparatus and Systems, Vol. PAS-94, No. 6, 1975, pp. 1943 to 1953

U. Habedank, R. Kugler. Theoretical and experimental studies of the critical line length for the interruption of short-line faults, IEEE Trans. Power Apparatus and Systems, Vol. PAS 100, July 1981, pp 3345-3357

B.Thorén. Short-line faults. Elteknik 9 (1966) N°2 (February)

Appendix A

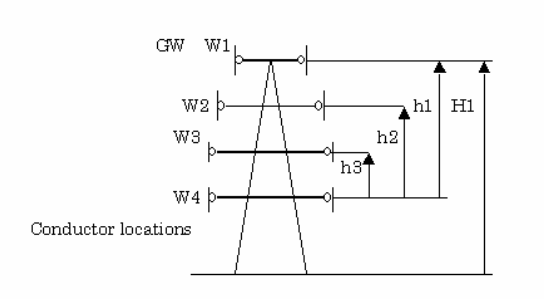
Comparison of surge impedances

Table A.1 - Comparison of typical values of surge impedances for a single-phase fault (or third pole to clear a three-phase fault) and the first pole to clear a three-phase fault

U_r (kV)	**123**		**245**		**420**	
s (mm^2)	120	300	340	2×240	4×240	4×402
d (mm)	15,7	24,2	28,1	2×21,7	4×21,7	4×27,7
Z_1 (Ω)	375	350	365	300	240	235
Z_0 (Ω)	680	655	585	465	450	445
peak factor k (p.u.)	1,55	1,55	1,52	1,43	1,41	1,34
Z single-phase fault (Ω)	476	452	438	355	310	305
Z 1st pole to clear a three-phase fault (Ω)	440	414	416	340	284	279

Appendix B

Surge impedances and peak factors of transmission lines in Japan



Voltage (kV)	500/550		275/300		154/168		66/72
Tower dimensions (m)							
H1	79,5		52		45,8		28
h1	36,5		24,2		14,8		11
h2	29		15,2		8,6		7,5
h3	14,5		7,6		4,3		3,5
W1	29		13,4		0		0
W2	22,4		12,6		7		4,5
W3	23,2		13,4		7		9,4
W4	24		14,2		7		6
Tower interval (m)	333		333		333		333
Earth wire earthing (Ω)							
- at towers	10		10		10		10
- at substation	1		1		5		5
Conductors							
Section area (mm^2)	810	410	810	410	810	410	410
Diameter (cm)	3,84	2,85	3,84	2,85	3,84	2,85	2,85
DC resistance (Ω/km)	0,0374	0,0738	0,0374	0,0738	0,0374	0,0734	0,0738
Number per phase	4	4	4	2	2	1	1
Spacing (cm)	50 (12,5)**		50 (12,5)**		50 (12,5)**	--	--
Earth wire							
Section area (mm^2)	150		120		90		70
Diameter (cm)	2,00		1,75		1,2		1,05
DC resistance (Ω/km)	0,224		0,277		0,86		1,12
Number	2		2		1		1
Surge impedance/Amplitude factor							
1st	364/1,28	369/1,29	324/1,15	371/1,21	328/0,95	409/1,19	410/1,19
2nd	374/1,32	379/1,31	338/1,20	384/1,25	345/1,00	425/1,23	421/1,22
3rd	389/1,37	393/1,37	356/1,26	401/1,31	367/1,06	447/1,30	441/1,28
4th	392/1,38	396/1,38	360/1,27	406/1,32	376/1,09	455/1,32	448/1,30
5th	397/1,40	402/1,40	369/1,30	414/1,35	392/1,14	471/1,37	455/1,32
6th	405/1,43	409/1,43	381/1,35	424/1,38	416/1,21	491/1,42	467/1,36

- calculations were done by applying EMTP – LINE CONSTANTS.
- 4th, 5th and 6th values correspond to 1st, 2nd and 3rd values on single circuit lines respectively.
- similar values are reported from other international users with this type of line construction.

** average space during attraction by short-circuit

Appendix C

Calculation of actual percentage of SLF breaking currents

The line reactance corresponding to the standardised line length can be calculated with

$$X_{\text{L,stand}} = \frac{1 - \dfrac{I_{\text{L,stand}}}{I_{\text{sc}}}}{\dfrac{I_{\text{L,stand}}}{I_{\text{sc}}}} \times X_{\text{source}}$$

with:

$I_{\text{L,stand}}$ short-line fault breaking current corresponding to the standardised line length;

$X_{\text{L,stand}}$ line reactance corresponding to the standardised line length;

X_{source} reactance corresponding to the rated short-circuit breaking current.

If the reactance of the actual line differs from the reactance corresponding to the standardised line length within the tolerances of -20 % for L_{90} and ±20 % for L_{75} and L_{60}, as stated in 6.109.2 of IEC 62271-100, the related current values can be calculated as follows:

$$I_{\text{L,act}} = \frac{U_{\text{r}}}{\sqrt{3}\,(X_{\text{L,act}} + X_{\text{source}})}$$

with:

$I_{\text{L,act}}$: short-line fault breaking current corresponding to the actual line length;

$X_{\text{L,act}}$: line reactance corresponding to the actual line length.

The actual line length is calculated considering the standardised line length and the percentage deviation of the actual line length from the standardised one:

$$l_{\text{act}} = l_{\text{stand}}\left(1 + \frac{d}{100}\right)$$

with

l_{stand}: standardised line length;

l_{act}: actual line length

d: deviation of the actual line length from the standardised one in percent.

The actual line reactance is calculated using the following equation:

$$X_{\text{L,act}} = X_{\text{L,stand}} \times \frac{l_{\text{act}}}{l_{\text{stand}}} = X_{\text{L,stand}}\left(1 + \frac{d}{100}\right)$$

The actual percentage short-line fault breaking current $I_{\text{perc,act}}$ is determined by the following equation:

$$I_{\text{perc,act}} = \frac{I_{\text{L,act}}}{I_{\text{sc}}} \times 100 = \frac{I_{\text{perc,stand}}}{1 + \frac{d}{100} \times \left(1 - \frac{I_{\text{perc,stand}}}{100}\right)}$$

In Table C.1 the actual percentage short-line fault breaking currents are stated for each standardised short-line fault breaking current $I_{\text{perc,stand}}$ taking the maximum tolerances for the line length into account.

Table C.1 - Actual percentage short-line fault breaking currents

Standardised short-line fault breaking current $I_{\text{perc,stand}}$ (%)	**Deviation** d (%)	**Actual short-line fault breaking current** $I_{\text{perc,act}}$ (%)
90	-20	91,8
90	0	90
75	-20	78,9
75	+20	71,4
60	-20	65,2
60	+20	55,5

Appendix D

TRV with parallel capacitance

The short-line fault TRV from an idealised distributed parameter line is known as a triangular wave shape. In the Laplace domain, this can be written as follows:

$$\mathrm{TRV}(s) = \frac{\omega IZ}{s^2}(1 - 2\mathrm{e}^{-t_\mathrm{L} s}) \qquad \text{(D.1)}$$

where

- t_L time to peak without capacitance
- ω angular frequency of the breaking current
- I breaking current peak
- Z surge impedance
- s Laplace operator

The equation is valid for $0 \le t \le 2t_\mathrm{L}$. If the TRV for $t > 2t_\mathrm{L}$ is required, Equation (D.1) should be replaced by the following:

$$\mathrm{TRV}(s) = \frac{\omega IZ}{s^2}(1 - 2\mathrm{e}^{-t_\mathrm{L} s} + 2\mathrm{e}^{-t_\mathrm{L} s} + ...) \qquad \text{(D.2)}$$

In order to introduce damping of the wave, the term $2\mathrm{e}^{-t_\mathrm{L} s}$ in Equation (D.1) should be replaced by $2\mathrm{e}^{-kt_\mathrm{L} s}$, where k < 1,0.

The TRV can be represented by the product of the breaking (= injection) current and the impedance, also in the Laplace domain. The injection current in the Laplace domain can be approximated such as:

$$\frac{\omega I^2}{s} \quad \text{(corresponding to } \omega It \text{ in the time domain)}$$

Then the impedance of the distributed parameter line in Laplace domain is:

$$Z(1 - 2\mathrm{e}^{-t_\mathrm{L} s}) \qquad \text{(D.3)}$$

The lumped capacitance impedance in the Laplace domain is represented by:

$\frac{1}{Cs}$, where C = capacitance

The capacitance value includes both the lumped capacitance at the circuit-breaker terminal side producing the inherent t_dL of the line and the additional capacitance, if any.

Connecting the two impedances represented by Equations (D.2) and (D.3) in parallel, the following equation is obtained for the total impedance in the Laplace domain:

$$\frac{Z(1-2e^{-t_L s})}{Cs(\frac{1}{Cs}+Z-2Ze^{-t_L s})} = \frac{Z(1-2e^{-t_L s})}{(1+t_{dL}s)-2t_{dL}se^{-t_L s}} \qquad (D.4)$$

where $t_{dL} = ZC$.

t_{dL} is applicable also for conditions with parallel additional capacitances.

The product of the injection current ($\omega I/s^2$) and the impedance (D.4) is the TRV with parallel capacitance in the Laplace domain:

$$\omega IZ \times \frac{1}{s^2} \times \frac{(1-2e^{-t_L s})}{(1+t_{dL}s)-2t_{dL}se^{-t_L s}}$$

$$= \omega IZ\left[\frac{1}{s^2}\times\frac{1}{1+t_{dL}s} - \frac{1}{s^2}\cdot\frac{2e^{-t_L s}}{(1+t_{dL}s)^2} + ...\right]$$

$$= \omega IZ\left[\frac{1}{s^2} - \frac{t_{dL}}{s} + \frac{t_{dL}^2}{1+t_{dL}s} - 2e^{-t_L s}\left(\frac{1}{s^2} - \frac{2t_{dL}}{s} + \frac{2t_{dL}^2}{1+t_{dL}s} + \frac{t_{dL}^2}{(1+t_{dL}s)^2}\right)\right] \qquad (D.5)$$

The second line of Equation (D.5) is valid for $t_L \le t \le 2t_L$ only.

By reversal Laplace transformation process, SLF TRV with parallel capacitance in time domain is calculated as follows:

$0 \le t \le t_L$:

$$TRV_1(t) = \omega IZ\left[t + t_{dL}\left(e^{-\frac{t}{t_{dL}}} - 1\right)\right] \qquad (D.6)$$

$t_L \le t \le 2t_L$

$$TRV_2(t) = TRV_1(t) - 2\omega IZ\left[t'\left(e^{-\frac{t'}{t_{dL}}} + 1\right) + 2t_{dL}\left(e^{-\frac{t'}{t_{dL}}} - 1\right)\right] \qquad (D.7)$$

with $t' = t - t_L$

Using equations (D.6) and (D.7), the correct waveshapes of SLF TRVs with line inherent t_{dL} and for conditions with additional parallel capacitance can be calculated.

For cases $t > 2t_L$, Equation (D.2) instead of Equation (D.1) should be applied. When damping is introduced, $2ke^{-t_L s}$ should be used instead of $2e^{-t_L s}$ in Equation (D.1) as mentioned before. The total calculation process is then slightly modified.

For every case, with or without parallel capacitance, the peak value of the TRV is quasi equal to ωIZt_L. Dividing Equations (D.6) and (D.7) by ωIZt_L, gives the following equations.

$$\mathrm{TRV}(10) = \frac{t_{dL}}{t_L}\left[\frac{t}{t_{dL}} + \left(e^{-\frac{t}{t_{dL}}} - 1\right)\right] \qquad \text{(D.8)}$$

$$\mathrm{TRV}(20) = \mathrm{TRV}(10) - \frac{2t_{dL}}{t_L}\left[\frac{t'}{t_{dL}}\left(e^{\frac{-t'}{t_{dL}}} + 1\right) + 2\left(e^{\frac{-t'}{t_{dL}}} - 1\right)\right] \qquad \text{(D.9)}$$

The TRV wave shape given by Equations (D.8) and (D.9) can be normalised such that the peak value is unity and time unit is in t_{dL}. The parameter is t_L/t_{dL}. Figure D.1 shows the results of a calculation for t_L/t_{dL} = 4,0. Multiplying the Y-axis value by ωIZt_L and X-axis value by t_{dL}, the actual wave shape is obtained.

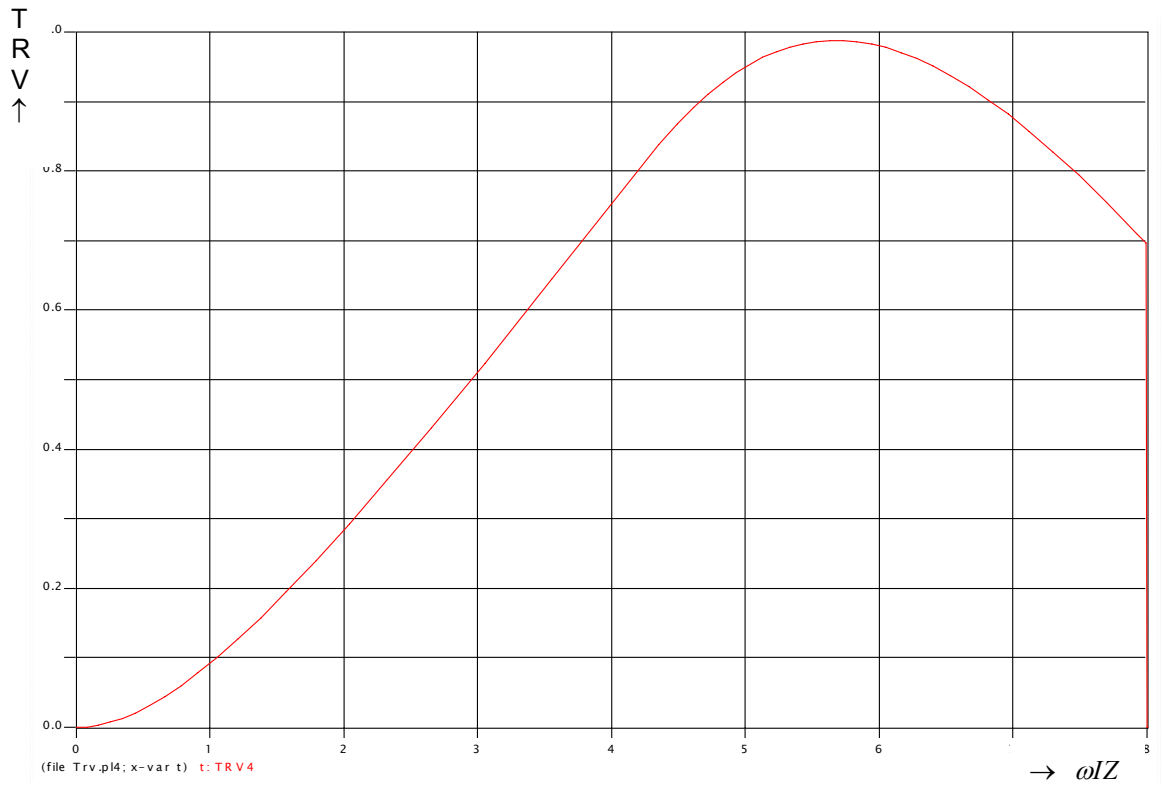


Figure D.1 - TRV vs. ωIZ as function of t/t_{dL} when t_L/t_{dL} = 4,0

6 Out-of-phase switching

The IEC 62271-100 subclauses relevant to this chapter are:

4.106 Rated out-of-phase making and breaking current

6.110 Out-of-phase making and breaking tests

6.1 Reference system conditions

Although the out-of-phase switching condition is a rare occurrence, two cases are considered to illustrate the background to the standard requirements of IEC 62271-100.

A Instability of a system in service, due to overloading, load rejection, or other major disturbance such as that caused during a severe storm, etc.;

B Erroneous switching operation during synchronizing.

6.1.1 Case A

The system conditions illustrated above are often considered in power system stability studies. In such events, as the parts of the system separate the out-of-phase occurs across an impedance in a system, where it can be assumed a heavy load current exists. Out-of-phase breaking is initiated by a protective system detecting the voltage phase angle difference across the impedance and sending a tripping signal to the associated circuit-breakers. The first to open of these will experience the out-of-phase condition. Studies indicate that during such disturbances, the phase angles of the individual generators scatter so that it is unlikely that the two sections will have a simple, uniform phase angle between them. Also, a densely connected part of a system, can rarely be separated to be out-of-phase with the rest of the system.

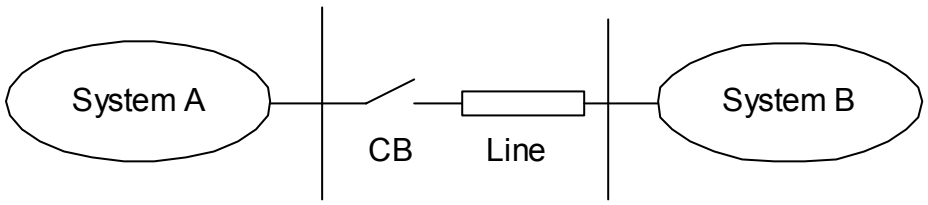


Figure 12 - Typical system of out of phase breaking for case A

Figure 12 is a representation of a separating system where a line is the link between the two separate parts, i.e. system A and system B. The connecting line (or impedance such as a transformer) exists in between. Each of system A and B is considered to be corresponding to a system operating at its T30 to T60 short-circuit level.

Cases where the short-circuit power of both systems A and B correspond to T100 can be considered exceptional.

Cases with a weak sub-system on one side can be considered covered by case B with regard to TRV parameters.

6.1.2 Case B

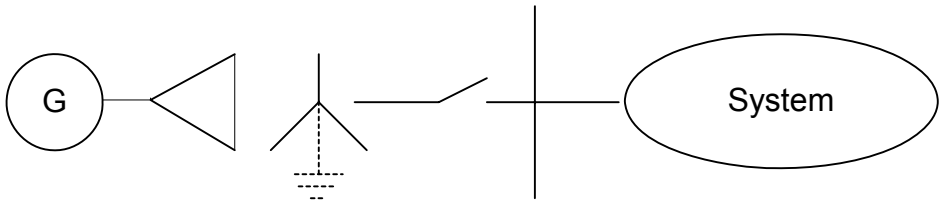


Figure 13 - Typical system of out of phase breaking for Case B

Synchronizing between relatively strong systems can be considered a rare case and is covered by case A with regard to TRVs.

A more typical system layout for synchronising is shown in Figure 13, where a generator interfaces with a system via a step up transformer. The right-hand side system short-circuit power can be considered to be corresponding to a T60 level. In such systems, a synchronizing operation is mostly performed at the high-voltage side of the step-up transformer. Typical characteristics are:

- generator sub-transient reactance is 0,3 p.u.;
- step-up transformer reactance is 0,1 p.u.

Present day maximum ratings of generator units are in the order of 600 MVA and 1300 MVA for 245 kV and 550 kV, respectively. Introducing, also, the short-circuit reactance of the system, the out-of-phase breaking current is taken to be in the order of 6 kA at the most.

The following points are also to be considered:

- due to the connection of the transformer windings, i.e., Δ on the LV side and Y on the HV side, for solidly earthed systems, the zero sequence reactance of the generator side is far lower than that of positive sequence, i.e. ca. 25 %. Therefore the pole-to-clear factor is maximum for the 3rd pole, and is 1,0;
- the recovery voltage of the generator after the fault current has been cleared is heavily damped, giving a damping factor in the order of 0,8;
- statistically a 180 degree out-of-phase condition very rarely occurs in practice and an additional factor of 0,8 can be introduced.

6.2 TRV parameters introduced into Tables 1b and 1c of IEC 62271-100

As rated TRV parameters in Tables 1b, 1c and 1d of IEC 62271-100, system requirements and experiences based on circuit-breaker characteristics and other duties, i.e. terminal faults, etc., are to be considered.

6.2.1 Case A

6.2.1.1 Breaking current

The breaking current listed is 25 % of the rated short-circuit breaking current.

As shown before, actual out-of-phase occurs between the portions of a system via a certain impedance. As already noted, it is unlikely that a perfect 180 degree of out-of-phase will ever occur. The value 25 % is taken to cover the majority of cases.

6.2.1.2 First-pole-to-clear factor

A first-pole-to-clear factor of 2,0/2,5 is specified by IEC 62271-100 for effectively/non-effectively earthed systems, respectively.

Theoretical maximum values are 2,6/3,0, based on IEC 62271-100, but as shown before, under out-of-phase conditions, stability studies have shown that the phase angles of the individual generators are scattered. A factor of 0,8 can safely be introduced. Furthermore, the majority of today's effectively earthed systems have a first-pole-to-clear factor of 1,15 at the most. Therefore, the values of 2,0/2,5 are considered to be more than sufficient.

6.2.1.3 Amplitude factor

An amplitude factor of 1,25 is specified by IEC 62271-100.

Theoretical maximum value can be 1,4. However, due to the statistical displacement between the timings of the TRV peaks of the two parts of the system, a factor of $1/\sqrt{2}$ could be introduced to the two randomly over-swinging parts, i.e.:

$$(2 + 2 \times 0{,}4 \times 1/\sqrt{2})/2 = 1{,}28$$

Considering the higher value of the first-pole-to-clear factor, the value 1,25 is appropriate.

6.2.1.4 RRRV

The rate-of-rise of recovery voltage is specified by IEC 62271-100 as 1,54 kV/μs or 1,67 kV/μs depending on the earthing conditions.

As the 90 percentile values, it has already been established that the typical values are: 3,0 kV/μs on both sides (based on the two systems running at 60 % of their respective ratings) and 25 % of the rated short-circuit breaking current of the circuit-breaker. From these values, the maximum RRRV value is derived as follows:

$$2 \times 3{,}0 \times 25/60 = 2{,}5 \text{ kV/}\mu\text{s}$$

Statistically the RRRV value is influenced by phase angle and breaking current. A factor of 0,6 to 0,7 can be introduced and the present values of 1,54/1,67 kV/μs can be retained.

u_1 = 0,75×($\sqrt{2}/\sqrt{3}$)×U_r×(first-pole-to-clear factor)

- The value depends on the system layout and is common to other breaking duties, i.e. T100, T60, etc.
- The factor 0,75 was agreed between IEC SC 17A and the IEEE PES Switchgear Committee as a harmonised value.

t_1 = u_1/RRRV;

u_c = ($\sqrt{2}/\sqrt{3}$)×U_r×(first-pole-to-clear factor)×(amplitude factor);

The t_2 value mainly depends on the system scale and is to be common to the other duties, i.e. T100, T60, etc. The value specified for T100 is satisfactory as system requirement. Laboratory experience shows that the t_2 value introduces no significant influence on circuit-breaker performance.

Like the RRRV condition above, the case of direct connection to a line can be excluded for t_d values. The value of t_d also depends on the system layout and, based on experience, the T60 time delay in can be applied as rated value with no detriment.

6.2.2 Case B

Simulation calculations have been performed and the results are shown in, Figure 14, Figure 15 and Figure 16. In this study a 1500 MVA synchronous generator (at present the highest capacity available) is connected to a 550 kV system through a step-up transformer. The 550

kV system has a short-circuit current of 30 kA. The generator parameters used here are the actual parameters as supplied by the manufacturer:

sub-transient reactance	ca. 0,3 p.u.
transformer short-circuit reactance	ca. 0,1 p.u.

The following conditions apply:

- two parameter TRV waveshape;
- generator/transformer side contribution is predominant for the TRV across the circuit-breaker terminals due to higher voltage drop in these reactances;
- due to the step-up transformer winding connections (∆/Y on the generator side/HV side, respectively), the positive sequence reactance is four times the zero sequence reactance. Hence the third-pole-to-clear sees a maximum TRV of 1,0 p.u. (as for a solidly earthed system);
- the generator side recovery voltage just after current interruption shows significant damping (in the order of 0,7 – 0,8) and then gradually recovers to the original value;
- the calculation was done for a 180 degrees of out-of-phase condition. Due to the statistically rare occurrence of this condition, a factor of 0,8 has been introduced.

From these, the following parameters are introduced for case B.

6.2.2.1 First-pole-to-clear factor (third-pole-to-clear for effectively earthed system)

In Table 14 of IEC 62271-100 the first-pole-to clear factor is listed as 1,3/1,9 and is obtained as follows:

For effectively earthed systems 2×1,0×0,8×0,8 = ca. 1,3;

For non-effectively earthed systems 2×1,5×0,8×0,8 = ca. 1,9.

6.2.2.1.1 Amplitude factor

The amplitude factor specified by IEC 62271-100 is 1,5.

An arbitrary factor of 0,9 is introduced as in the case of T10, considering voltage drop in the transformer/generator, non-pure simple swing waveshape, etc.

u_c = ($\sqrt{2}/\sqrt{3}$)×U_r×first-pole-to-clear factor×amplitude factor;

t_3 = 2×(t_3 for T10).

The capacitance value of the HV side of the transformer is the same as in case of T10. The reactance together with that of the generator is about four times of the transformer. The effect of the low-voltage side capacitance is not significant. Therefore the TRV frequency is about 50 % of that of the transformer itself.

6.2.2.1.2 RRRV

The RRRV is equal to u_c/t_3

$t_{d\,=}$ 2×(t_d for T10)

Using the approach used for t_3 above.

6.2.2.1.3 Conclusion for case B

For effectively earthed systems, TRV parameters are well covered by those of T10. Specifying TRVs for case B is not necessary.

For non-effectively earthed systems, u_c is higher than that of T10, but not higher than for case A. In actual systems of the voltage class applying non-solid earthing, it is necessary to consider the multi-frequency TRV wave shapes, and the voltage drop portion in the generator/transformer reactance, etc. Hence lower u_c and/or RRRV are probable. Based on that TRV ratings for case B are not considered necessary.

6.2.3 TRV parameters for out-of-phase testing

As mentioned before and from laboratory experience, t_2, t_d and t' values are viewed as less dominant on out-of-phase breaking phenomena provided the other test duties (T10 to T100, SLF, etc.) are performed. For rating purposes, the t_2 value is that of T100s as specified in Tables 1a, 1b, 1c and 1d. However, for convenience of testing, and since the influence of t_2 is not considered critical, the testing values given in Tables 14a and 14b extend this value up to two times that for T100s.

System requirement basis is considered appropriate.

t_d, t' Lowest side values as used for T60

Again the system basis is used.

Figure 14, Figure 15 and Figure 16 represent a typical simulation result for a case B study.

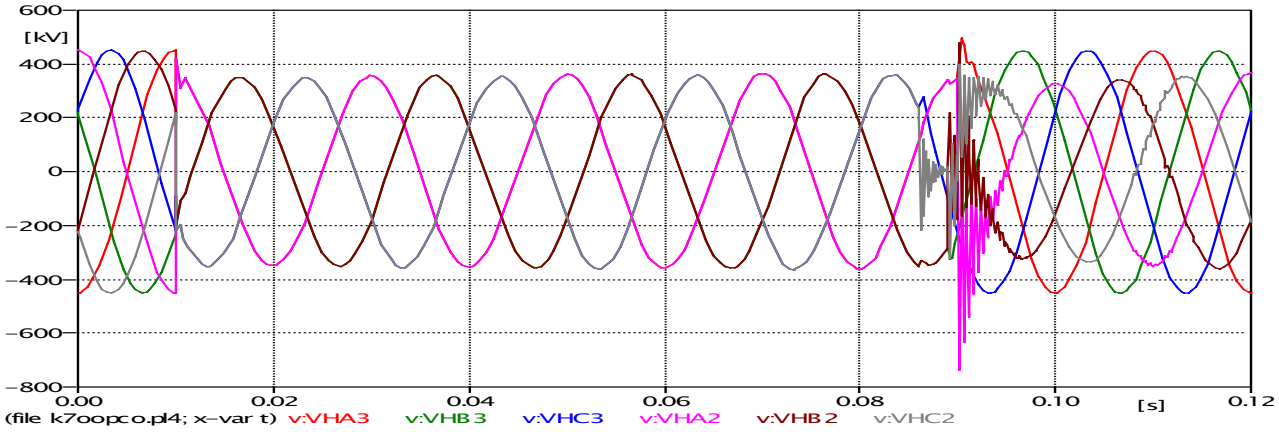


Figure 14 - Voltage on both sides during CO under out-of-phase conditions

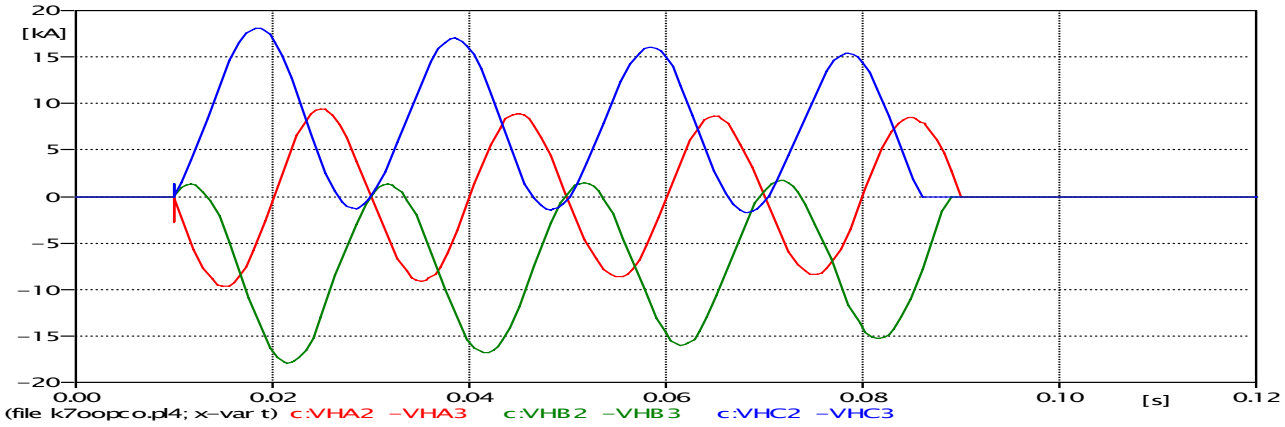


Figure 15 - Fault currents during CO under out-of-phase

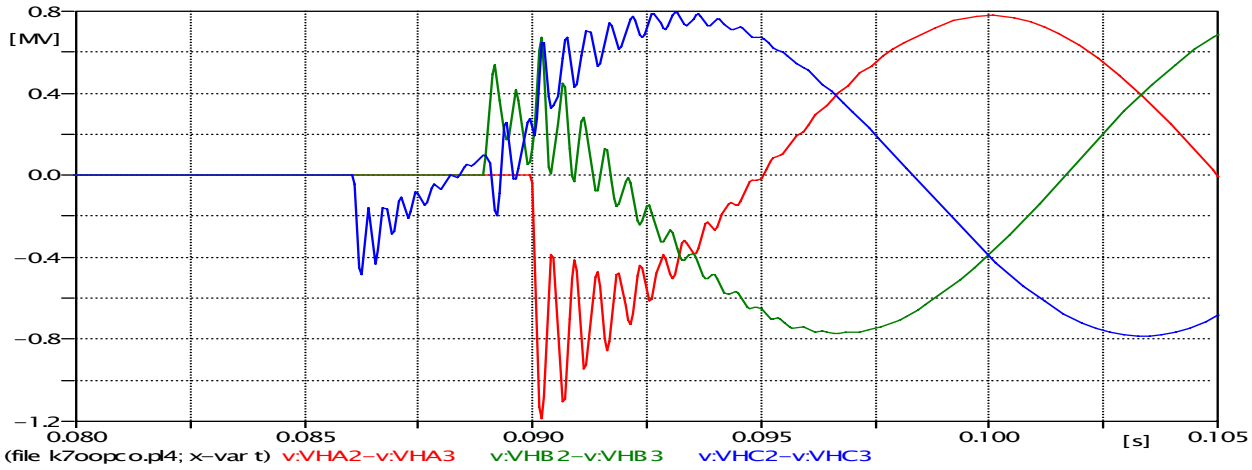


Figure 16 - TRVs for out-of-phase clearing (enlarged)

7 Double earth fault

7.1 General

The IEC 62271-100 subclause relevant to this chapter is:

6.108 Single-phase and double-earth fault tests

7.2 Basis for specification

This test requirement is limited to applications in non-effectively earthed systems.

In non-effectively earthed neutral systems, circuit-breakers shall be capable of clearing single-pole the short-circuit currents which may occur in case of double earth faults i.e. earth faults on two different phases, one of which occurs on one side of the circuit-breaker and the other one on the other side.

Such a situation can occur if, after a single phase to earth fault, the two other phases stay energised long enough to allow another fault to earth to happen on another phase. This situation is unlikely to happen if the healthy phases are opened in a relatively short time after the occurrence of the initial fault. However it may be provoked by the voltage elevation on healthy phases that is produced by the first fault to earth.

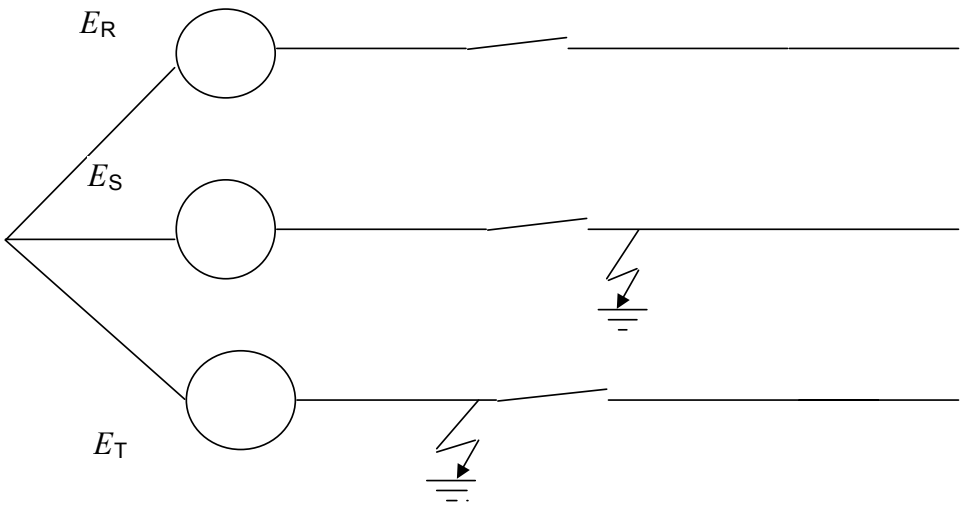


Figure 17 - Representation of a system with a double earth fault

Figure 17 illustrates the case where a fault is present in phase S. Due to the voltage elevation on the healthy phases a fault develops on the other side of the circuit-breaker in phase T. The total fault current needs to be interrupted by pole S.

From Figure 17 it can be seen that one pole of the circuit-breaker is required to interrupt a short-circuit under phase-to-phase voltage. As the recovery voltage is higher than in other terminal fault test duties, this breaking condition could be more severe than a terminal fault T100 condition, but, as explained in appendix A, the short-circuit current is only 87 % of the rated short-circuit current.

This condition is not covered by test duty T100 and since it has a low probability of occurrence, IEC 62271-100 requires only one breaking test to be performed. When this

standard was established it was considered that it is only necessary to test with the most severe condition of arcing time i.e. with a long arcing time corresponding to a high energy content of the arc and with a moving contact position close to the fully open position.

7.3 Short-circuit current

The calculation of the short-circuit current is detailed in appendix A.

A symmetrical current is specified in testing, as in test duty T100s, because a symmetrical condition leads to the highest TRV peak possible when compared to the value specified for test duty T100.

7.4 TRV

The RRRV is as specified for the supply side circuit of SLF single-phase test duties (2 kV/µs) because the TRV frequency is similar. As the short-circuit current is lower than rated, the RRRV should be slightly reduced, but for standardisation purposes it is kept at 2 kV/µs.

TRV values are determined accordingly. Taking into account the harmonisation of TRV values with IEEE/ANSI, TRV parameters are as follows:

- first reference voltage $u_{1,sp}$ = 0,75 $U_r\sqrt{2}$
- time $t_{1,sp}$ = $t_1 \times u_{1,sp}/u_1$
- peak voltage $u_{c,sp}$ = 1,4$U_r\sqrt{2}$
- time $t_{2,sp}$ = t_2

u_1, t_1, and t_2 are given in Tables 1a, 1b and 1c of IEC 62271-100.

Appendix A

Determination of the short-circuit current in the case of a double-earth fault

Figure A.1 shows a schematic representation of the fault case illustrated in Figure 17.

Phase supply voltage is E.

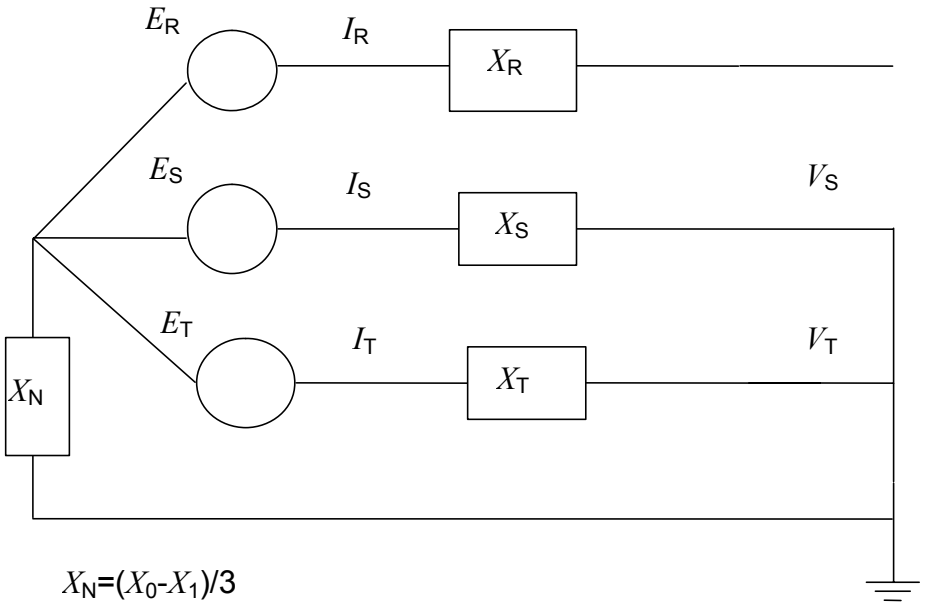


Figure A.1 - Representation of circuit with double-earth fault

The use of symmetrical components leads to the following equations:

$I_R = 0 \rightarrow \quad I_1 + I_2 + I_0 = 0$

$V_S = 0 \rightarrow \quad V_0 + a^2 V_1 + a V_2 = 0$

$V_T = 0 \rightarrow \quad V_0 + a V_1 + a^2 V_2 = 0$

with

$a = e^{j2\pi/3} = -1/2 + j\sqrt{3}/2$

$$V_1 = E - X_1 I_1 \qquad \text{(A.1)}$$

$$V_2 = - X_2 I_2 \qquad \text{(A.2)}$$

$$V_0 = - X_0 I_0 \qquad \text{(A.3)}$$

this gives:

$-X_0 I_0 + a^2(E - X_1 I_1) - a X_2 I_2 = 0$

$-X_0 I_0 + a(E - X_1 I_1) - a^2 X_2 I_2 = 0$

$I_1 + I_2 + I_0 = 0$

or,

$$a^2 X_1 I_1 + a X_2 I_2 + X_0 I_0 = a^2 E \quad \text{(A.4)}$$

$$a X_1 I_1 + a^2 X_2 I_2 + X_0 I_0 = a E \quad \text{(A.5)}$$

$$I_1 + I_2 + I_0 = 0 \quad \text{(A.6)}$$

Multiplying Equation (A.5) with a and subtracting Equation (A.4) leads to:

$$(1 - a) X_2 I_2 + (a - 1) X_0 I_0 = 0 \quad \Rightarrow \quad X_2 I_2 = X_0 I_0 \quad \text{(A.7)}$$

Multiplying Equation (A.4) with a and subtracting Equation (A.5) leads to:

$$X_1 I_1 (1\text{-}a) + (a\text{-}1) X_0 I_0 = (1\text{-}a) E \quad \Rightarrow \quad X_1 I_1 - X_0 I_0 = E \quad \text{(A.8)}$$

A system of 3 equations with 3 unknown is obtained:

$$I_1 + I_2 + I_0 = 0 \quad \text{(A.9)}$$

$$X_2 I_2 = X_0 I_0 \quad \text{(A.10)}$$

$$X_1 I_1 - X_0 I_0 = E \quad \text{(A.11)}$$

Resolution of equations:

$$I_1 + \frac{X_0 I_0}{X_2} + I_0 = 0$$

$$I_0 \times \frac{X_2 + X_0}{X_2} = -I_1 \qquad I_0 = -\frac{I_1 X_2}{X_2 + X_0}$$

$$X_1 I_1 + \frac{X_0 X_2}{X_2 + X_0} \times I_1 = E \text{, or } I_1 \left(X_1 + \frac{X_0 X_2}{X_2 + X_0} \right) = E \qquad \Rightarrow I_1 = \frac{E}{X_1 + \frac{X_0 X_2}{X_2 + X_0}} \quad \text{(A.12)}$$

$$\text{and } I_0 = -\frac{I_1 X_0}{X_2 + X_0} \quad \text{(A.13)}$$

$$I_2 = -I_1 - I_0 = -\frac{I_1 X_0}{X_2 + X_0} \quad \text{(A.14)}$$

The current in phase S is given by:

$I_S = I_0 + a^2 I_1 + a I_2$ with $a = e^{j2\pi/3} = -1/2 + j\sqrt{3}/2$

From (A.13) and (A.14), and with the standard hypothesis $X_2 = X_1$:

$$I_S = -\frac{X_1 I_1}{X_1 + X_0} + a^2 I_1 - a \frac{X_0 I_1}{X_1 + X_0}$$

$$\frac{I_S}{I_1} = \frac{-X_1 + a^2 X_1 + a^2 X_0 - a X_0}{X_1 + X_0} = \frac{-X_1 \left(3/2 + j\sqrt{3/2}\right) - j X_0 \sqrt{3}}{X_1 + X0}$$

Using the equation for I_1 given in (A.12), the current for the double earth fault (I_{def}) is then:

$$I_{\text{def}} = I_{\text{S}} = \frac{-E\sqrt{3}}{X_1 + 2X_0}\left(\frac{\sqrt{2}}{2} + \frac{\text{j}}{2} + \text{j}\frac{X_0}{X_1}\right)$$

For non-effectively earthed networks X_0 >> X_1, which gives:

$$I_{\text{def}} = -\frac{E\sqrt{3}}{X_1 + 2X_0} \times \text{j}\frac{X_0}{X_1} = -\text{j}\frac{E\sqrt{3}}{2X_1}$$

The three-phase short-circuit is given by $I_{\text{sc}} = E/X_1 \rightarrow I_{\text{def}} = -\text{j}\frac{\sqrt{3}}{2} I_{\text{sc}}$, or $\left|I_{\text{def}}\right| = 0{,}87\left|I_{\text{sc}}\right|$.

8 Switching of capacitive currents

8.1 General

Capacitive currents are encountered in the following cases:

- switching of no-load overhead lines;
- switching of no-load cables;
- switching of capacitor banks;
- switching of filter banks.

Interruption of capacitive currents is generally a light duty for a circuit-breaker, because the currents are normally a few hundred amperes. There is however a risk that restrikes will occur, which may lead to undesirable overvoltages or high frequency transients affecting the power quality in the network. Restrikes may also cause damage to the breaking unit.

Energisation of capacitive loads may lead to overvoltages or high currents. Two such cases are the switching of parallel capacitor banks and the switching of no-load lines.

Type testing is designed to be representative of the service conditions up to the point of either clearing, reigniting or restriking. Because the actual value of overvoltage and transient response is totally system dependent, tests cannot replicate these effects. By providing a means of assessing the likelihood of restrike occurrence the user can determine what best suites their application. It is assumed that since capacitor switching is not the only source of overvoltage, other protection systems are employed and in the case of unacceptable power quality for sensitive electronic equipment a sufficiently low number of likely events are selected. A separate study of actions relative to power quality on energisation must also be made.

In the selection of the rating for the circuit-breaker for capacitive current switching the following needs to be considered:

a) application, i.e. overhead line, cable, capacitor bank or filter bank;

b) power frequency of the network;

c) earthing situation of the network;

d) presence of single or two phase-to-earth faults.

From the application the restrike performance class of the circuit-breaker can be determined (C1 or C2) as well the mechanical endurance class (M1 or M2). The earthing situation of the network, presence of single and two phase-to-earth faults are important factors that determine the recovery voltage across the circuit-breaker which, in its turn, determines the test voltage of the circuit-breaker.

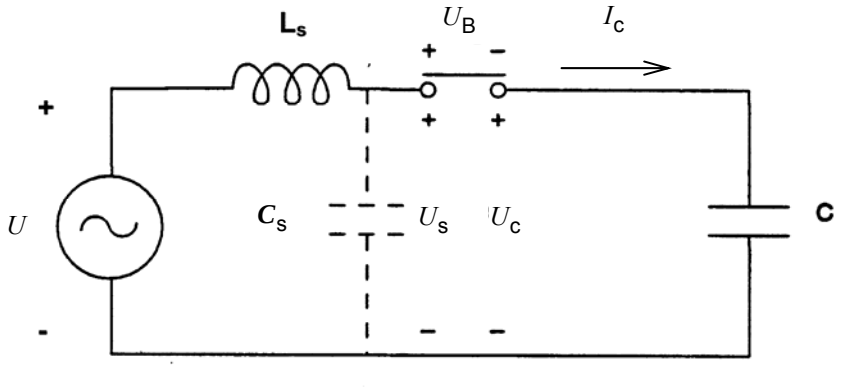
In the following clauses the general theory of capacitive current switching is given as well as the application and testing considerations.

8.2 General theory of capacitive current switching

8.2.1 De-energisation of capacitive loads

8.2.1.1 Capacitor banks

The single-phase equivalent circuit shown in Figure 18 may be used to illustrate the conditions when de-energising a capacitor bank.



C	capacitive load (capacitor bank)	U_c	voltage across the capacitor bank (r.m.s.)
C_s	source side capacitance	I_c	capacitive current (r.m.s.)
U	source voltage (r.m.s.)	U_s	voltage on source side of the circuit breaker (r.m.s.)
U_B	voltage across the circuit breaker (r.m.s)	L_s	source inductance

Figure 18 - Single-phase equivalent circuit for capacitive current interruption

8.2.1.1.1 Capacitive current

The capacitive current I_c flowing in the circuit is given by the following equation:

$$I_c = \frac{\omega_s C \times U}{1-\omega^2 L_s C} = \frac{\omega_s C \times U}{1-\frac{\omega_s^2}{\omega_i^2}} \qquad (19)$$

with

$\omega_s = 2\pi f_s$, where f_s is the system frequency in Hz

$\omega_i = \frac{1}{\sqrt{L_s C}} = 2\pi f_i$, where f_i is the inrush current frequency in Hz (see also 8.2.2.1)

With ω_i >> ω_s, Equation (19) transforms to $I_c = \omega_s C \times U$

8.2.1.1.2 Recovery voltage

Figure 19 shows the current and voltage shapes at interruption.

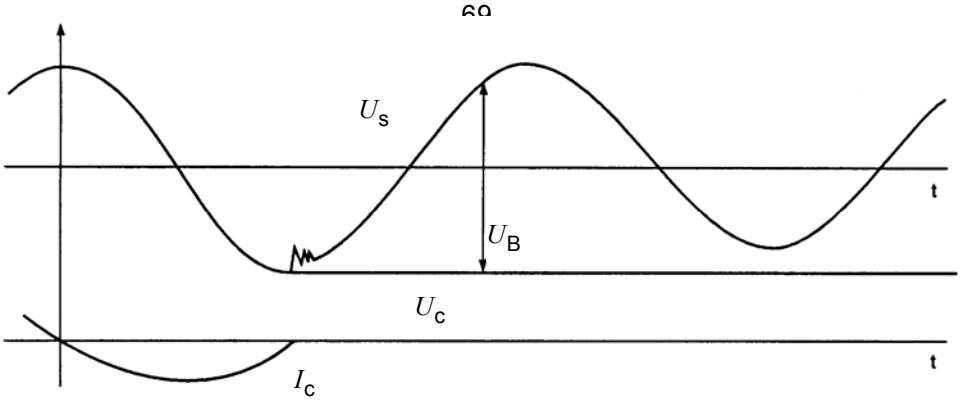


Figure 19 - Voltage and current shapes at capacitive current interruption

After interruption of the current, the supply side voltage U_s will be more or less unaffected. There is only a minor decrease in amplitude, associated with the disappearance of the capacitive load. The transition to the new amplitude value is associated with a slight oscillation, the frequency of which is determined by L_s and C_s.

From the moment the current is interrupted, the charge of the capacitor bank C is trapped. The voltage U_c will therefore remain constant at the value it had at current zero (namely the peak value of the supply voltage).

Together with the low current amplitude to be interrupted, the low initial rate-of-rise of the recovery voltage makes it relatively easy for the circuit-breaker to interrupt. Some circuit-breakers may interrupt even if the current zero would occur immediately after contact separation. Half a cycle after current zero, the recovery voltage has risen to an amplitude of twice the peak value of the supply voltage. Consequently, a rated frequency of 60 Hz is more severe than 50 Hz. The circuit-breaker may then not be able to withstand the high value of the recovery voltage across a relatively small contact gap. Dielectric breakdown may occur between the contacts and current would start to flow again.

Figure 20 shows current and voltage wave shapes in a case where voltage breakdown occurs relatively close to the recovery voltage peak. The load side voltage will swing up to a voltage that ideally (without damping present) reaches three times the supply voltage peak u_p. The oscillation frequency of the current and voltage after the breakdown is determined by L_s and C (assuming $C \approx C_s$). The circuit-breaker may easily interrupt the current again at one of its current zeros, with the result that the voltage across the capacitor may attain a new constant value, perhaps higher than before. Further breakdowns associated with even higher overvoltages across the load may then occur (see also Figure 21).

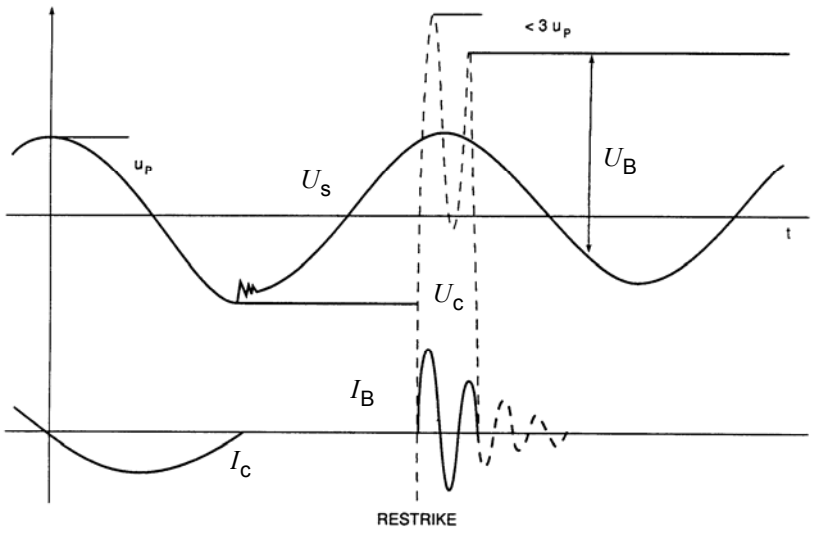


Figure 20 - Voltage and current wave shapes in the case of a restrike

Voltage breakdowns at capacitive current interruption are divided into two categories:

1. Reignitions.
   Voltage breakdown during the first 1/4 cycle following current interruption.
2. Restrikes.
   Voltage breakdown 1/4 of a cycle or more following current interruption.

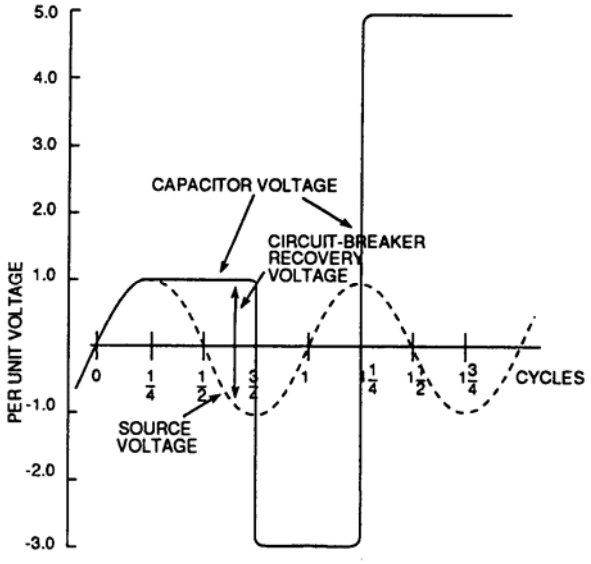
Another phenomenon, which has been observed predominantly on vacuum circuit-breakers, may occur during capacitive current and short-circuit breaking current tests, but also at lower currents and voltages. This phenomenon is known as a Non Sustained Disruptive Discharge, or NSDD.

An NSDD is defined as follows:

non-sustained disruptive discharge (NSDD)
disruptive discharge associated with current interruption, that does not result in the resumption of power frequency current or, in the case of capacitive current interruption does not result in current at the natural frequency of the circuit

NOTE Oscillations following NSDDs are associated with the parasitic capacitance and inductance local to or of the circuit-breaker itself. NSDDs may also involve the stray capacitance to earth of nearby equipment.

For details concerning NSDDs, refer to Chapter 13 of Part 1 of this Application Guide.



Key

1 p.u. is the peak value of the phase-to-earth voltage

Figure 21 - Voltage build-up by successive restrikes

Restrikes will lead to overvoltages across the capacitive load (maximum 3 p.u. for a single restrike, where 1 p.u. is the peak value of the phase-to-earth voltage) while reignitions will not produce any overvoltages (theoretically max. 1 p.u.). Reignitions are acceptable, but they may cause power quality problems, as they represent a temporary short-circuit.

In reality there are no restrike-free circuit-breakers. It would take an infinite number of test shots to verify this. For this reason the concept of restrike performance was introduced IEC 62271-100.

When interrupting small capacitive currents, some circuit-breaker types may exhibit current chopping. Current chopping is a distortion of the current prior to current zero and is usually caused by the high arc voltage. Different types of circuit-breakers have varying degrees of current chopping.

Current chopping will cause an interruption prior to the current zero of the power frequency current. This also means that the trapped charge on the capacitive load will not be at its peak, which results in a lower recovery voltage peak and a lower stress on the contact gap of the circuit-breaker.

The recovery voltages in three-phase circuits are more complicated than in the single-phase case. shows as an example the recovery voltage of the first-pole-to-clear in a case with a non-effectively earthed capacitive load. The recovery voltage initially has a shape that would lead to a peak value equal to three times the supply voltage peak (dotted line). When the two last poles interrupt 90 degrees after the first, there is however, a discontinuity in the slope and the final peak value for the first pole-to-clear is 2,5 times the supply voltage peak (see also 8.2.1.4).

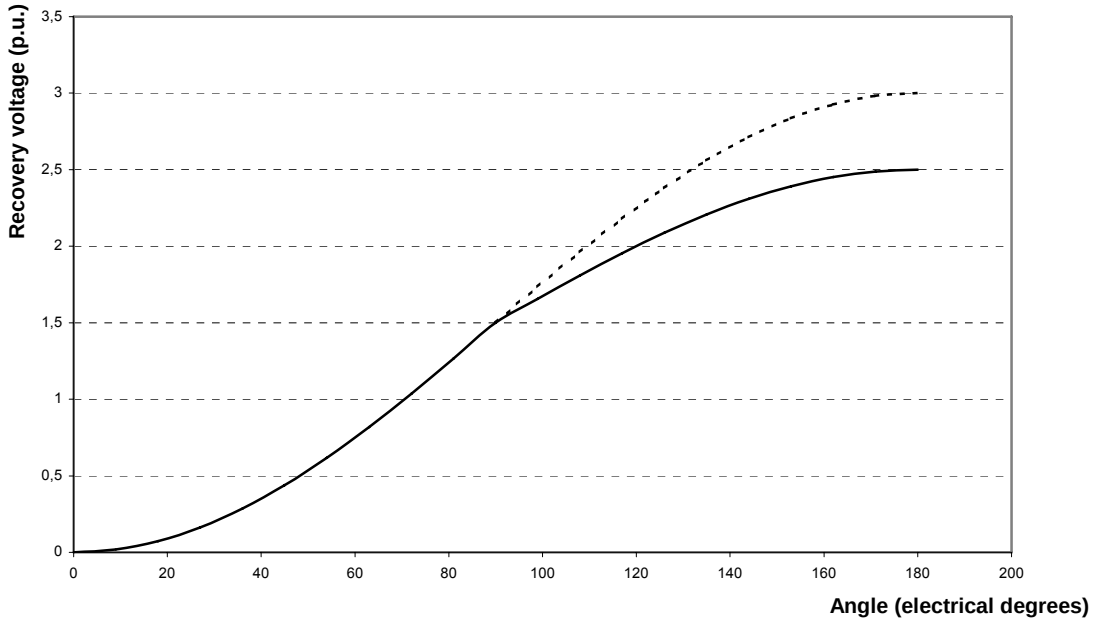


Figure 22 - Recovery voltage of the first-pole-to-clear at interruption of a three-phase non-effectively earthed capacitive load

8.2.1.2 No-load cables

8.2.1.2.1 Cable charging current

The cable charging current is a function of the following characteristics:

- system voltage;
- cable geometry;
- insulation dielectric constant;
- cable length.

The shunt capacitive reactance can be obtained from the cable manufacturer, or if the physical constants of the cable are known, the shunt capacitive reactance can be calculated [1]. For single-conductor and three-conductor shielded cables (for the different three-conductor cable configurations see Figure 24 and Figure 25) the shunt capacitive reactance can be written as:

$$X_c = \frac{0{,}3495}{f_s \varepsilon_r} \ln \frac{r_i}{r_c} \quad (\text{M}\Omega \text{ per phase per km, see footnote } 1) \qquad (20)$$

where

f_s = system frequency, in Hz

ε_r = dielectric constant of cable dielectric material, in F/m

r_i = inside radius of shield, in mm

r_c = conductor radius, in mm

---

1 When using the quantity MΩ per phase per km, it should be remembered that the shunt capacitive reactance in MΩ for more than 1 km decreases because the capacitance increases. For more than 1 km of line, therefore, the value of shunt capacitive reactance as given above should he divided by the number of km of line.

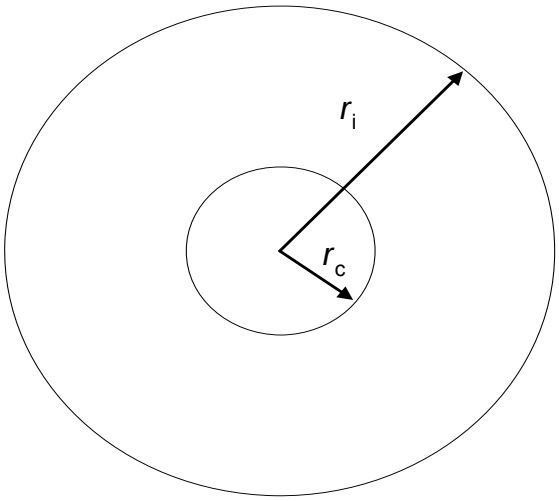


Figure 23 – Cross-section of a high-voltage cable

Using the capacitive reactance, the cable charging current can be calculated and compared with the rated cable charging current of the circuit-breaker given in IEC 62271-100. If the calculation exceeds the rating, the manufacturer should be consulted. Before an application can be made, the inrush current rating should also be checked (see 8.3.11.1).

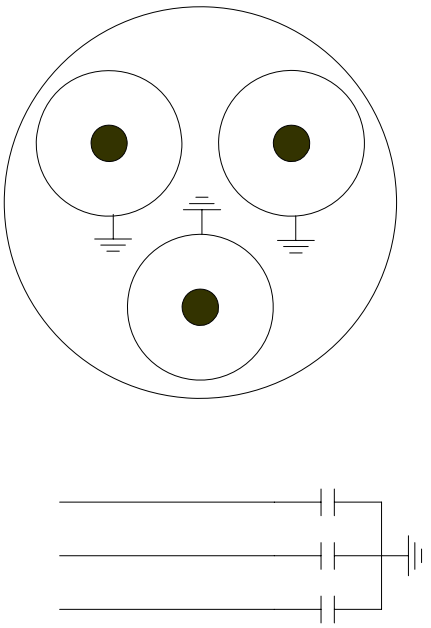


Figure 24 – Screened cable with equivalent circuit

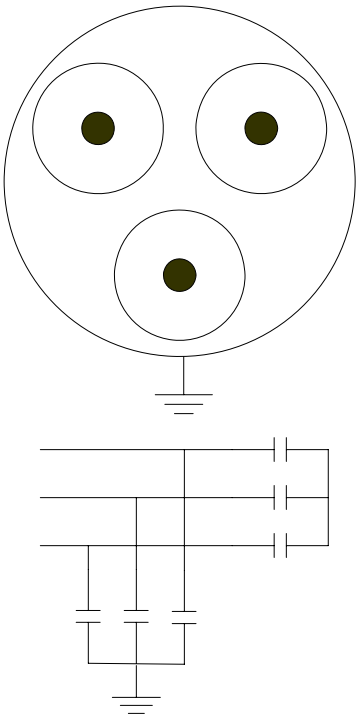


Figure 25 – Belted cable with equivalent circuit

8.2.1.2.2 Recovery voltage

The recovery voltage is equal to that of a capacitor bank (see 8.2.1.1.2).

8.2.1.3 No-load overhead lines

8.2.1.3.1 Uncompensated overhead lines

8.2.1.3.1.1 Line charging current

A no-load overhead line can generally be represented by a capacitance. In the case of short lines (< 200 km) this capacitance can be considered concentrated, but in the case of long lines it must be considered distributed. Typical capacitance values vary from 9,1 nF/km per phase for single conductor overhead lines to 14 nF/km per phase for four-conductor bundle overhead lines (see also [2]).

8.2.1.3.1.2 Recovery voltage

Overhead lines have capacitance both between phases and to earth. Figure 26 shows the peak value of the recovery voltage in the first pole-to-clear as a function of the capacitance ratio C_1/C_0 (positive to zero sequence capacitance). It has been assumed that the amplitude approaches 3 p.u. This is the case without capacitance to earth and delayed interruption of the second phase. An example of the voltages in such a case is given in Figure 22. The other extreme, $C_1 = C_0$, is the case where each phase has capacitance to earth only. The recovery voltage peak is then 2 p.u. as in a single-phase case.

Overhead lines typically have C_1/C_0 ratios in the order of 2,0. In this case Figure 26 shows that the recovery voltage peak is approximately 2,4 p.u.

While Figure 22 and Figure 26 assume a delayed interruption of the second phase, when the second and third phases interrupt 90° after the first, the maximum recovery voltage peak is 2,4 p.u. one half cycle after interruption (see 8.2.1.4). This assumes that $C_1 = 2C_0$. This is the differential voltage of the source and line sides, including the effects of coupled voltage on the first-pole-to clear.

When the characteristics of the voltage in service (shape and peak value) are deviating from those of the test voltage, the restrike probability may increase. For example, if the line is compensated, the line side component is not a trapped voltage resulting from the trapped charge, but a voltage oscillating with a frequency determined by the compensating reactors and the line side capacitance (see 8.2.1.3.2).

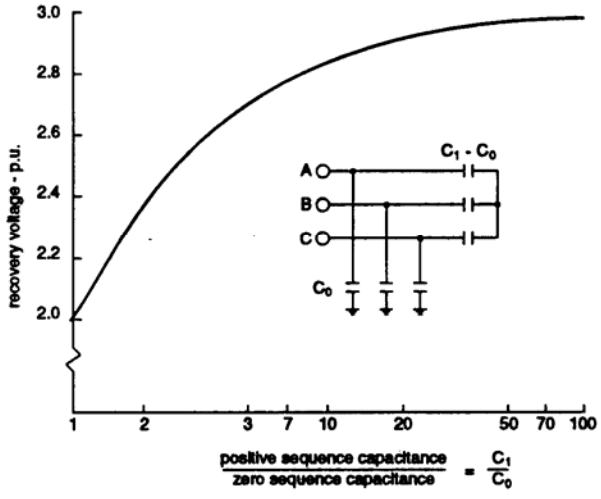


Figure 26 - Recovery voltage peak in the first-pole-to-clear as a function of C_1/C_0, delayed interruption of the second phase

If the C_1/C_0 ratio is greater than 2, higher voltages may be coupled to the first pole-to-clear, resulting in increased probability of restrike. In this case the manufacturer should also be consulted since circuit-breaker designs are sensitive to both current magnitude and recovery voltage waveshapes.

8.2.1.3.2 Compensated overhead lines

Long overhead lines are often compensated with shunt reactors to reduce the charging current of the line. The compensation factor (k_L) of an overhead line is given by the ratio of the capacitive reactance ($X_{C,line}$) to the inductive reactance ($X_{L,\ reactor}$) of the compensating reactor, in equation:

$$k_L = \frac{X_{C,line}}{X_{L,reactor}} \tag{21}$$

If $X_{L,\ reactor} > X_{C,\ line}$, the line is undercompensated, a line with $X_{L,\ reactor} < X_{C,\ line}$ is called overcompensated.

8.2.1.3.2.1 Line charging current

The compensated line charging current is given by $I_{Lc} = I_c^{'}(1-k_L)$

where

I_{Lc} line charging current of the compensated line

I_c' line charging current of uncompensated line

k_L compensation factor

Assuming a line compensated at 60 % (i.e. k_L = 0,60), the line charging current is

I_{Lc} = I_c' (1-0,6) = 0,4I_c', or 40 % of the uncompensated value.

8.2.1.3.2.2 Recovery voltage

If the line is compensated, the line side component of the recovery voltage is no longer a d.c. voltage, but an oscillation of which the frequency is determined by the compensating reactor and the line capacitance.

The resonant frequency is approximated by:

The resonant frequency is approximated by:

$$f_L \approx \frac{1}{2\pi\sqrt{LC}} = f_s\sqrt{\frac{X_{C,line}}{X_{L,reactor}}} = f_s\sqrt{k_L} \tag{22}$$

f_L resonance frequency of the compensated line (Hz)

L inductance of the reactor (H)

C total capacitance of the line (F)

f_s system frequency (Hz)

k_L compensation factor

In other words: the resonance frequency of a compensated line is dependent on the degree of compensation. Since the compensation usually is less than 1, this resonance frequency is

less than the system frequency, resulting in a reduction of the recovery voltage. Typical current and voltage waveshapes are given in Figure 27.

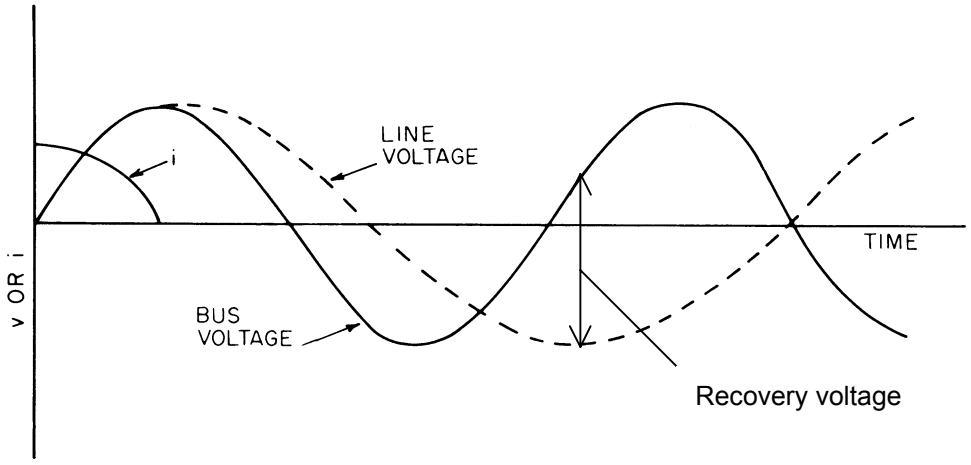


Figure 27 - Typical current and voltage relations for a compensated line

The first half-cycle of recovery voltage is, for this example, as shown in Figure 28. Compensation thus results in a decrease of the probability of restrike at a particular current. Under these conditions improved performance may result, the circuit-breaker becoming restrike-free or possibly able to interrupt higher values of charging current. The manufacturer should be consulted on applications which markedly alter the recovery voltage.

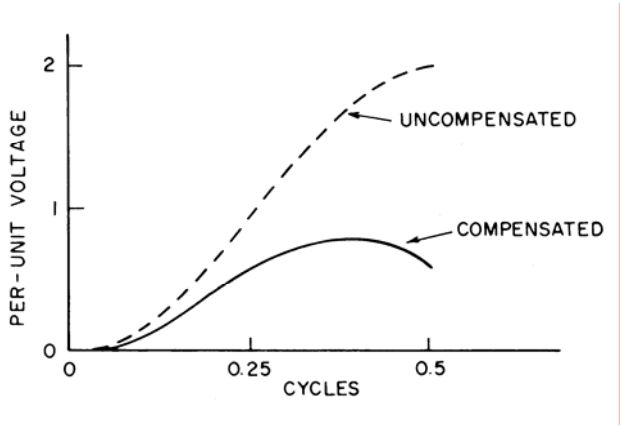


Figure 28 - Half cycle of recovery voltage

8.2.1.3.3 Switching the charging currents of long overhead lines

Very long overhead lines in excess of 300 km, even those of simple construction type, present a special case not covered by the requirements of subclause 6.111.7 of IEC 62271-100 or its notes. Where such long lines are to be switched, consideration should be given to the higher value of peak TRV present on interruption. Some idea of the ability of a particular circuit-breaker for making and breaking of this requirement can be gained by considering any out-of-phase switching evidence which may exist. Such evidence will usually provide adequate demonstration of the elevated TRV and although the current values for the out-of-phase duty are higher than the charging current of the line, they may be considered comparable for the purposes of providing background evidence for this special duty. However, such limited evidence as the out-of-phase evidence cannot be considered satisfactory for demonstration purposes for an overhead line switching duty. For full compliance, evidence will be required to satisfy the capacitive current switching requirements of subclause 6.111 of IEC 62271-100, but to the elevated values required by the specific application.

Some users may be concerned about rare or occasional switching operations from one end on a series of long lines. This can occur during the early development stages of a system when intermediate substations may not be fully equipped or may even be by-passed. In such cases it may be appropriate to consider the out-of-phase capability in relation to the combined load presented by the series of lines. If satisfactory for the current and voltage conditions then specific testing for the severe capacitive current switching duty of IEC 62271-100 would not be necessary at the enhanced levels of the extended line. They would be required for the switching duty of the individual lines of the series, as normal. There is an obvious risk associated with such operation and this acceptance of the out-of-phase evidence is only possible if the operating regime for such an extended line length condition is infrequent. Infrequent operation is often likely to be the case for such development stages of a system.

8.2.1.4 Voltage factors for capacitive current switching tests

Depending on the capacity of a high-power laboratory, capacitive current switching tests may be performed as three-phase tests or single-phase tests. For the higher voltages (362 kV, 420 kV, 550 kV and 800 kV) unit tests are sometimes made.

Especially when single-phase tests are made to cover three-phase application, the test voltage shall reflect the application of the circuit-breaker in the field. One of the factors influencing this is the earthing situation of the network. The other is the presence of single or two-phase faults.

Subclause 6.111.7 of IEC 62271-100 gives the following voltage factors for single-phase test voltage (see Table 5). The test voltage measured at the circuit-breaker location prior to interruption shall not be less than the rated voltage $U_r/\sqrt{3}$ and the voltage factors given in Table 5.

Table 5 – Voltage factors for single-phase capacitive current switching tests

Voltage factor k_c	Application
1,0	Tests corresponding to normal service in solidly earthed neutral systems without significant mutual influence of adjacent phases of the capacitive circuit, typically capacitor banks with solidly earthed neutral and screened cables.
1,2	Test on belted cables and line-charging current switching [1)] corresponding to normal service conditions in solidly earthed neutral systems with mutual influence of adjacent phases of the capacitive circuit for rated voltages 52 kV and above.
1,4	- breaking during normal service conditions in systems having a non-effectively earthed neutral including screened cables [1)]; - breaking of capacitor banks non-effectively earthed neutral; - test on belted cables and line-charging current switching [2)] corresponding to normal service conditions in effectively earthed systems for rated voltages less than 52 kV; - breaking in the presence of single or two-phase to earth faults in systems having a solidly earthed neutral.
1,7	Tests corresponding to breaking in non-effectively earthed systems in the presence of single or two-phase to earth faults [3)].
1) When a significant capacitance to earth on the source side is present, the factor will be reduced. 2) Under the condition that the line can be replaced partly of fully by a concentrated capacitor bank. 3) The factor 1,7 is derived from the fact that the healthy phase sees the phase-to-phase voltage.	

Notes to Table 5:

a) The voltage factors for line-charging current switching tests of 1,2 and 1,4 are applicable to single-circuit line construction. Requirements for multiple overhead line constructions may be greater than these factors.

b) The 1,4 factor is a compromise and is valid for breaking of capacitive currents in non-effectively earthed systems, where the second and third pole-to-clear interrupt 90° after the first.

c) When the non-simultaneity of contact separation in the different poles of the circuit-breaker exceeds 1/6th of a cycle of rated frequency, it is recommended to raise the voltage factor or to make only three-phase tests. Such circuit-breakers fall outside the scope of the standard.

The voltage factor 1,4 is explained as follows (see Figure 29):

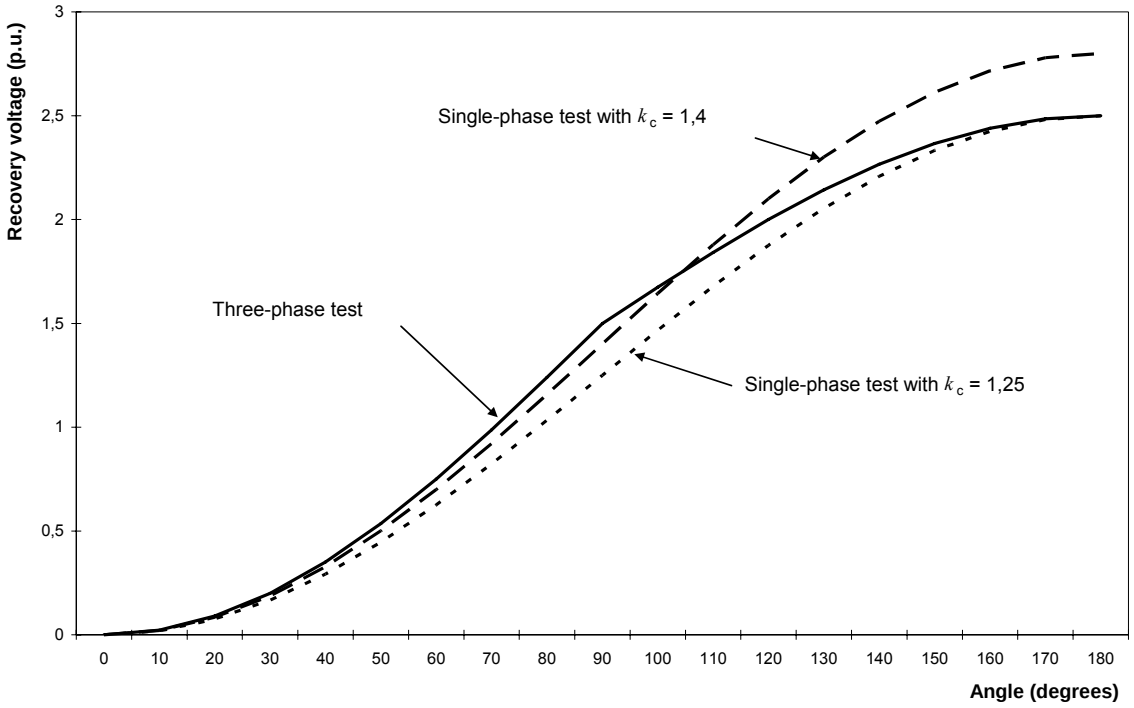


Figure 29 – Recovery voltage on first-pole-to-clear for three-phase interruption: capacitor bank with isolated neutral

When the current in the first pole is interrupted, the voltage across the circuit-breaker will rise as if the voltage factor would have been 1,5. When the second and third pole interrupt 90° later, there is a discontinuity and the recovery voltage across the first pole-to-clear will follow a 1-cos wave with a voltage factor of 1,25. The recovery voltage is indicated by the solid line in Figure 29. By using a voltage factor of 1,25 (dotted line in Figure 29), the initial portion of the recovery voltage across the first pole is not adequately covered. Using a voltage factor of 1,5 will result in a too high stress. A voltage factor of 1,4 as indicated by the dashed curve in Figure 29 is a compromise that adequately covers the actual recovery voltage.

Careful consideration should be given to these voltage factors when circuit-breakers are relocated to other parts of the system where the application is different from that of the original location.

The voltage factors specified in Table 5 are associated with single circuit line constructions and are chosen to accommodate all known physical arrangements of the conductors of such circuits. Note a) to Table 5 indicates that switching in the case of multiple overhead line constructions which have parallel circuits may require a voltage factor greater than 1,2 and 1,4. This is because such circuits are likely to have an enhancement to the line side residual voltage following interruption. This is associated with the coupling (pick-up) from the parallel circuit and may add a power frequency peak voltage of up to 0,2 p.u. This is dependent upon the geometry of the conductor systems of the two circuits.

In addition, the effect of these changes on the line side voltage, following interruption by the first-pole-to-clear, does affect the shape of the TRV across that opening pole. Consideration of this may require additional testing if the existing factor does not adequately cover the combined effects. Alternatively, the higher of the given values, e.g. 1,4 for 1,2, can be selected to encompass the specific waveshape.

On occasion utilities have specified a voltage factor of 1,3 instead of 1,2 for their double circuit lines.

8.2.2 Energisation of capacitive loads

Energisation of capacitive loads is usually associated with transient voltages and currents. Those transients are the following:

- inrush currents;
- overvoltages caused by the system response to the voltage dip when energising capacitor banks (see 8.2.2.1);
- overvoltages caused by travelling waves on transmission lines and cables.

In this section the phenomena associated with energisation of capacitor banks, lines and cables is treated.

8.2.2.1 Capacitor banks

Since the use of capacitor banks for compensation purposes is increasing, it is common that more than one capacitor bank is connected to the same bus. This has no influence on the conditions at interruption. The current at closing, however, is affected to a high degree. Two different situations may occur:

a) The capacitor bank is energised from a bus that does not have other capacitor banks energised. This is called single (isolated) capacitor bank switching.
b) The capacitor bank is energised from a bus that has other capacitor banks energised. This is called back-to-back capacitor bank switching.

The conditions for isolated and back-to-back capacitor bank switching are given in 8.2.2.1.1 and 8.2.2.1.2. Even energized capacitor banks in nearby substations may contribute to the inrush current such that a back-to-back situation occurs.

Especially the second case may give rise to an inrush current of very high amplitude and frequency which sometimes has to be limited in order not to be harmful to the circuit-breaker, the capacitor banks and/or the network. The magnitude and frequency of this inrush current is a function of the following:

- applied voltage (point on the voltage wave at closing);
- capacitance of the circuit;
- inductance in the circuit (amount and location);
- any charge on the capacitor bank at the instant of closing;
- any damping of the circuit due to closing resistors or other resistances in the circuit.

It is assumed that the capacitor bank is discharged prior to energisation. This is a reasonable assumption, as capacitor units are fitted with discharging resistors that will discharge the capacitor bank. Typical discharge times are in the order of 5 minutes.

The transient inrush current to a single (isolated) bank is less than the available short-circuit current at the capacitor bank terminals. It rarely exceeds 20 times the rated current of the capacitor bank at a frequency that approaches 1 kHz. Since a circuit-breaker must meet the making current requirements of the system, transient inrush current is not a limiting factor in single (isolated) capacitor bank applications.

When capacitor banks are switched back-to-back, that is, when one bank is switched while another bank is connected to the same bus, transient currents of prospective high magnitude and with a high natural frequency may flow between the banks on closing of the circuit-breaker. The effects are similar to that of a restrike on opening. This oscillatory current is limited only by the impedance of the capacitor bank and the circuit between the energised bank or banks and the switched bank. This transient current usually decays to zero in a fraction of a cycle of the system frequency. In the case of back-to-back switching, the component supplied by the source is at a lower frequency and so small it may be neglected.

8.2.2.1.1 Single (or isolated) capacitor bank

A bank of shunt capacitors is considered single (isolated) when the inrush current on energisation is limited by the inductance of the source and the capacitance of the bank being energised. A capacitor bank is also considered single (isolated) if the maximum rate of change, with respect to time, of transient inrush current on energising an uncharged bank does not exceed the maximum rate of change of the symmetrical short-circuit current at the voltage at which the current is applied. The limiting value is equal to

$$\left(\frac{\mathrm{d}i_{\mathrm{i}}}{\mathrm{d}t}\right)_{\max} = \omega_{\mathrm{s}} I_{\mathrm{sc}} \sqrt{2} \qquad (23)$$

where

$\frac{\mathrm{d}i_{\mathrm{i}}}{\mathrm{d}t}$ rate of change of inrush current, A/s

I_{sc} rated r.m.s short-circuit current, in A

$\omega_{\mathrm{s}} = 2\pi f_{\mathrm{s}}$ system frequency, in rad/s and f_{s} is the power frequency, in Hz

The single-phase equivalent of a circuit where two capacitor banks are connected to a busbar is shown in Figure 30. L_1 and L_2 represent the stray inductance (or stray inductance plus additional damping inductance). The inductance L_{s} of the supply network will be several orders of magnitude higher than L_1 and L_2.

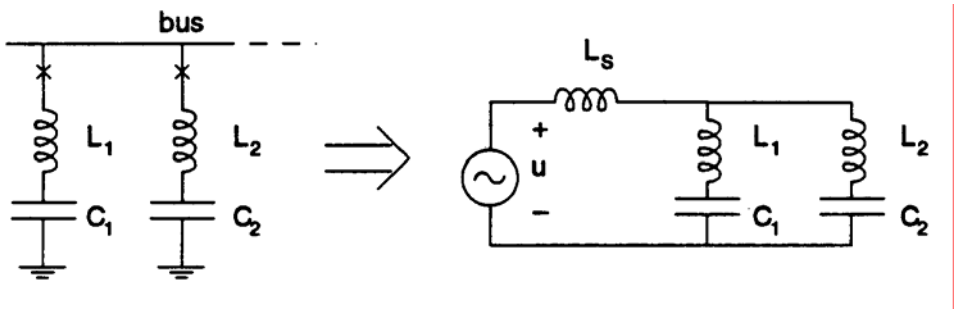


Figure 30 - Parallel capacitor banks

The case of energising a single (isolated) capacitor bank is equal to energisation of C_1 when C_2 is not connected in the circuit described in Figure 30. The circuit consists then of the source inductance L_{s} in series with the capacitor bank C_1. L_1 can be disregarded here, since $L_{\mathrm{s}} >> L_1$. In this case, the peak of the inrush current ($i_{\mathrm{i\ peak}}$) and inrush current frequency (f_{i}) are limited by the source impedance L_{s}.

Assuming that bank #1 is to be connected to the busbar and bank #2 is not connected, the following equations apply:

$$i_{\mathrm{i}} = \hat{u}\sqrt{\frac{C_1}{L_{\mathrm{s}}}}\sin\omega_{\mathrm{i}}t \tag{24}$$

and

$$f_{\mathrm{i}} = \frac{1}{2\pi\sqrt{(L_{\mathrm{s}} + L_1)C_1}} \tag{25}$$

where

i_{i} inrush current, in A

$\hat{u}$ peak of the source voltage, in V

$\omega_{\mathrm{i}} = 2\pi f_{\mathrm{i}}$ angular inrush frequency in rad/s, where f_{i} is the inrush current frequency, in Hz

with $L_{\mathrm{s}} >> L_1$, the frequency of the inrush current is:

$$f_{\mathrm{i}} = \frac{1}{2\pi\sqrt{L_{\mathrm{s}}C_1}} \tag{26}$$

The highest inrush current peak is obtained when switching the capacitor bank at the peak of the supply voltage.

$$i_{\mathrm{i\,peak}} = u\sqrt{2}\sqrt{\frac{C_1}{L_{\mathrm{s}}}} \tag{27}$$

With $I_{\mathrm{sc}} = \frac{u}{\omega_{\mathrm{s}}L_{\mathrm{s}}}$ and $I_1 = \omega_{\mathrm{s}}uC_1$, Equations (26) and (27) transform to

$$f_{\mathrm{i}} = f_{\mathrm{s}}\sqrt{\frac{I_{\mathrm{sc}}}{I_1}} \tag{28}$$

and

$$i_{\mathrm{i\,max}} = \sqrt{2}\sqrt{I_{\mathrm{sc}}I_1} \tag{29}$$

where

f_{s} power frequency, in Hz

I_{sc} short-circuit current of the source, in A (r.m.s.)

I_1 current through capacitor bank 1, in A (r.m.s.)

$i_{\mathrm{i\,max}}$ maximum peak of the inrush current

In the three-phase case the same equations may be applied. The voltage u is then the phase-to-earth voltage.

8.2.2.1.2 Back-to-back capacitor bank

The inrush current of a single (isolated) bank will be increased when other capacitor banks are connected to the same bus.

If in Figure 30 bank #1 is connected to the busbar and bank #2 is to be connected, the inrush current associated with the charging of bank #2 is supplied by bank #1 (back-to-back switching). As stated in 8.2.2.1, capacitor bank #2 is discharged prior to energisation. The peak and frequency of the inrush current are now limited by L_1 and L_2, in equation:

$$i_{\text{i peak}} = u\sqrt{2}\sqrt{\frac{C_{\text{eq}}}{L_{\text{eq}}}} \tag{30}$$

with

$$C_{\text{eq}} = \frac{C_1 C_2}{C_1 + C_2} \tag{31}$$

and

$$L_{\text{eq}} = L_1 + L_2 \tag{32}$$

This can reach extreme values since the magnitude of L_{eq} can be arbitrarily small.

The frequency of the inrush current is now:

$$f_{\text{i}} = \frac{1}{2\pi\sqrt{L_{\text{eq}} C_{\text{eq}}}} \tag{33}$$

Inserting Equations (31) and (32) in Equations (30) and (33) gives the following equation for the inrush current peak and frequency:

$$i_{\text{i peak}} = u\sqrt{2}\sqrt{\frac{I_1 I_2}{u\omega_{\text{s}} L_{\text{eq}}(I_1 + I_2)}} = \sqrt{2}\sqrt{\frac{u I_1 I_2}{\omega_{\text{s}} L_{\text{eq}}(I_1 + I_2)}} \tag{34}$$

$$f_{\text{i}} = \frac{1}{2\pi}\sqrt{\frac{\omega u(I_1 + I_2)}{L_{\text{eq}} I_1 I_2}} = \frac{1}{2\pi}\sqrt{\frac{2\pi f_{\text{s}} u(I_1 + I_2)}{L_{\text{eq}} I_1 I_2}} \tag{35}$$

In Equations (34) and (35) it is assumed that $I_1 = \omega_{\text{s}} C_1 u$ and $I_2 = \omega_{\text{s}} C_2 u$ (see also 8.2.1.1.1)

Connecting bank C_{n+1} with *n* banks in parallel that are already connected:

$$L' = \frac{1}{\frac{1}{L_1} + \frac{1}{L_2} + \ldots\ldots \frac{1}{L_n}} \tag{36}$$

and

$$C' = C_1 + C_2 + \ldots\ldots + C_n \tag{37}$$

To obtain the inrush current peak and frequency can be done by using Equation (30) and substituting C_1 by C' and C_2 by C_{n+1} in Equation (32). L_{eq} can be obtained by substituting L_1 by L' and L_2 by L_{n+1} in Equation (33).

$C_{\text{eq}} = \frac{C' \times C_{n+1}}{C' + C_{n+1}}$ and $L_{\text{eq}} = L' + L_{n+1}$

With $L_1 = L_2 = ... = L_{n+1} = L$ and $C_1 = C_2 = ... = C_{n+1} = C$, $L' = L/n$ and $C' = nC$,

$$i_{\text{i peak}} = u\sqrt{2}\,\frac{n}{n+1}\sqrt{\frac{C}{L}} \tag{38}$$

and

$$f_{\text{i}} = \frac{1}{2\pi\sqrt{LC}} \tag{39}$$

In a three-phase case the same equations may be applied. The voltage u is then the rated phase-to-earth voltage $U_{\text{r}}/\sqrt{3}$.

In this case Equations (34) and (35) transform to:

$$i_{\text{i peak}} = \sqrt{2}\sqrt{\frac{10^3 U_{\text{r}} I_1 I_2}{2\pi f_{\text{s}}\sqrt{3}\times 10^{-6} L_{\text{eq}}(I_1+I_2)}} = 13556\sqrt{\frac{U_{\text{r}} I_1 I_2}{f_{\text{s}} L_{\text{eq}}(I_1+I_2)}} \approx 13\,500\sqrt{\frac{U_{\text{r}} I_1 I_2}{f_{\text{s}} L_{\text{eq}}(I_1+I_2)}} \tag{40}$$

and

$$f_{\text{i}} = \frac{1}{2\pi}\sqrt{\frac{2\pi f_{\text{s}} 10^3 U_{\text{r}}(I_1+I_2)}{\sqrt{3}\times 10^{-6} L_{\text{eq}} I_1 I_2}} \approx 9.5\sqrt{\frac{f_{\text{s}} U_{\text{r}}(I_1+I_2)}{L_{\text{eq}} I_1 I_2}} \tag{41}$$

where

f_{i}	inrush current frequency	(kHz)
f_{s}	system frequency	(Hz)
I_1, I_2	capacitor bank currents	(A, r.m.s.)
$i_{\text{i peak}}$	inrush current peak	(A)
U_{r}	rated voltage	(kV)
L_{eq}	equivalent inductance	(μH)

Typical amplitudes of the inrush currents for back-to-back energisation of capacitor banks are several kA with frequencies of 2 - 5 kHz. Typical values are given in Table 5 of IEC 62271-100. Capacitors can normally withstand amplitudes up to 100 times their charging current.

If the inrush current amplitude and frequency exceed those stated in Table 5 of IEC 62271-100, it may be necessary to limit them. This can be done by insertion of additional series inductance in the circuit, or by using pre-insertion resistors (see section 8.2.2.6). Another possibility is to use controlled switching.

8.2.2.2 Cables

A circuit-breaker may be required to energise a no-load cable during its normal operating duties. Prior to energisation the cable is usually at earth potential, but can have a trapped charge from a previous switching operation. A cable may be switched from a bus that does not have other cables energised (single or isolated cable) or against a bus that has one or more cables energised (back-to-back).

8.2.2.3 Single (isolated) cable

A cable is defined as single (isolated) if the maximum rate of change, with respect to time, of transient inrush current on energising an uncharged cable does not exceed the rate of change of current associated with the maximum symmetrical interrupting current. This limiting value is numerically equal to

$$\left(\frac{\mathrm{d}i_{\mathrm{i}}}{\mathrm{d}t}\right)_{\max} = \omega_{\mathrm{s}}\sqrt{2}\,I_{\mathrm{sc}} = 2\pi f_{\mathrm{s}}\sqrt{2}\,I_{\mathrm{sc}} \qquad (42)$$

where

$\left(\frac{\mathrm{d}i_{\mathrm{i}}}{\mathrm{d}t}\right)_{\max}$ maximum rate of change of inrush current in A/s

I_{sc} rated r.m.s. short-circuit current, in A

$\omega_{\mathrm{s}} = 2\pi f_{\mathrm{s}}$ system frequency in rad/s, where f_{s} is the power frequency in Hz

By this definition it is possible to have cable circuits which are physically back-to-back, but are considered single (isolated) for application purposes provided a large inductance is located between the two cable circuits. The inductance must be large enough so that by itself it would limit fault current to a value less than or equal to the circuit-breaker rating.

8.2.2.4 Back-to-back cables

Cables are considered switched back-to-back if the maximum rate of change of transient inrush current on energising an uncharged cable exceeds that specified for a single (isolated) cable.

8.2.2.5 Cable inrush current

The energisation of a cable by the closing of a circuit-breaker will result in a transient inrush current. The magnitude and rate of change of this inrush current is a function of the following:

- applied voltage (including the point on the voltage wave at closing);
- cable surge impedance;
- cable capacitive reactance;
- inductance in the circuit (amount and location);
- any charges on the cable at the instant of closing;
- any damping of the circuit because of closing resistors or other resistance in the circuit.

The transient inrush current to a single (isolated) cable is less than the available short-circuit current at the circuit-breaker terminals. Since a circuit-breaker must meet the making current requirements of the system, transient inrush current is not a limiting factor in isolated cable applications.

When cables are switched back-to-back (that is, when one cable is switched while other cables are connected to the same bus), transient currents of high magnitude and initial high rate of change may flow between cables when the switching circuit-breaker is closed or restrikes on opening. This surge current is limited by the cable surge impedances and any inductance connected between the energised cable(s) and the switched cable. This transient current usually decays to zero in a fraction of a cycle of the system frequency. During back-to-back cable switching, the component of current supplied by the source is at a lower rate of change and so small that it may be neglected.

A typical circuit for back-to-back cable switching is shown in Figure 31. The inductances L_1, L_2, and L_{bus} between the cables are often very small with respect to the inductance L_s of the source. In many cases they will be less than 1 % of the source inductance. They consist of the inductances from the cables to the circuit-breakers, the circuit-breaker inductances, and the bus inductance of the current path. Values of inductance depend upon the physical configuration and are hence site specific and unable to be standardised. However, a representative range is 0,66 to 1,0 μH per phase per m.

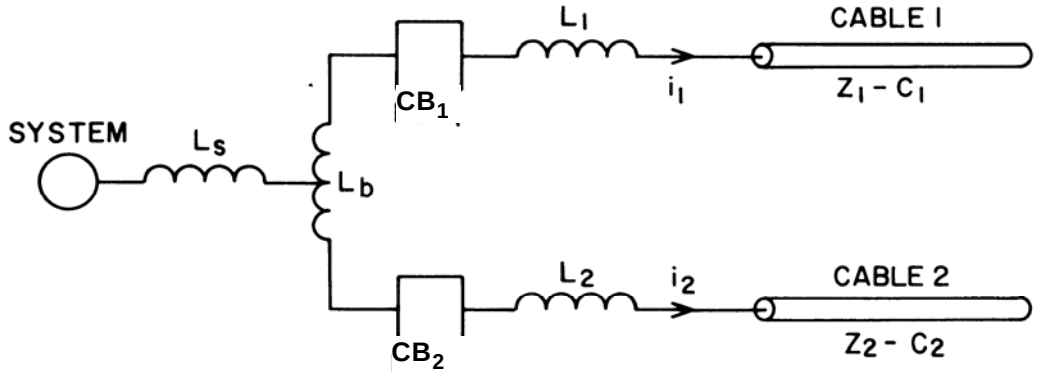


Figure 31 - Typical circuit for back-to-back cable switching

CB_1 circuit-breaker

CB_2 circuit-breaker, open for single (isolated) cable switching, closed for back-to-back switching

L_S source inductance

L_1, L_2 inductance between cables 1 and 2 and bus

Z_1, Z_2 surge impedance of cables 1 and 2

C_1, C_2 capacitance of cables 1 and 2

L_b inductance of bus connecting the cables

8.2.2.5.1 Single (isolated) cable

In switching a single (isolated) cable, if the source inductance is greater than 10 times the cable inductance, the cable can be represented as a capacitor. Otherwise, under transient conditions the cable can be represented by its surge impedance. An expression for surge impedance [3] is given for single-conductor and three-conductor shielded cables by

$$Z = \sqrt{\frac{L}{C}} = \frac{138}{\sqrt{\varepsilon}} \log\left(\frac{r_2}{r_1}\right) \qquad (43)$$

where

Z = surge impedance, in Ω

L = distributed inductance of cable, in H

C = distributed capacitance of cable, in F

ε = dielectric constant of cable dielectric material

r_2 = inside radius of sheath, in mm

r_1 = outside radius of conductor, in mm

Typical values of ε range from 2,3 (polyethylene) to 4 (fluid impregnated paper); a typical value for Z is 50 Ω.

To calculate the inrush current for a single cable, Figure 31 may be used, with Z_2 = 0.

$$i_{\mathrm{i}}(t) = \frac{E_{\mathrm{m}} - E_{\mathrm{t}}}{Z_1}\left[1 - \exp(-\frac{Z_1}{L}t)\right] \qquad (44)$$

with $i_{\mathrm{i\,peak}} = \dfrac{E_{\mathrm{m}} - E_{\mathrm{t}}}{Z_1}$

E_{m} crest of applied voltage

E_{t} trapped voltage on cable being switched

f_{s} source frequency (power frequency)

i_{i} inrush current

$i_{\mathrm{i\ peak}}$ peak of the inrush current

Z_1 cable surge impedance

L source inductance

The initial rate-of-rise (di/dt at t = 0) of the inrush current is $\dfrac{E_{\mathrm{m}} - E_{\mathrm{t}}}{L}$. For application purposes i_{peak} should be compared to the value given in Table 5 of IEC 62271-100.

The cable inrush current is not oscillatory in the usual frequency-related sense, but the initial slope can be used to determine an equivalent frequency which can be compared with the rated inrush frequency. In general,

$$\left(\frac{\mathrm{d}i_{\mathrm{i}}}{\mathrm{d}t}\right)_{\mathrm{r}} = 2\pi f_{\mathrm{ir}} I_{\mathrm{ir}} \qquad (45)$$

where

$\left(\dfrac{\mathrm{d}i_{\mathrm{i}}}{\mathrm{d}t}\right)_{\mathrm{r}}$ rate-of-change of rated inrush current in A/s

f_{ir} rated inrush current frequency

I_{ir} rated peak inrush current

The equivalent frequency f_{eq} for a cable inrush current is then obtained as follows:

$2\pi f_{\mathrm{eq}} I_{\mathrm{ir}} = \dfrac{E_{\mathrm{m}} - E_{\mathrm{t}}}{L}$ which gives $f_{\mathrm{eq}} = \dfrac{E_{\mathrm{m}} - E_{\mathrm{t}}}{2\pi L I_{\mathrm{ir}}}$ and for proper circuit-breaker application, f_{eq} should be less than the rated inrush current frequency.

8.2.2.5.2 Back-to-back cable inrush current

Neglecting the source contribution, back-to-back cables can be represented as shown in Figure 32.

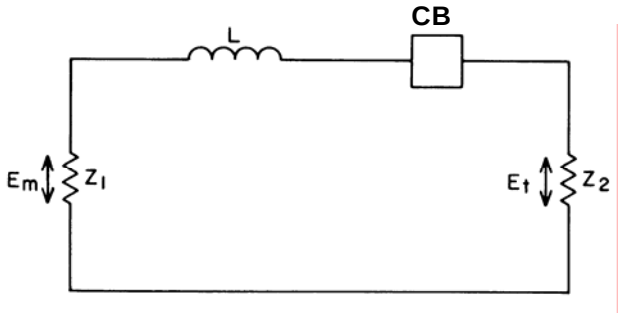


Figure 32 - Equivalent circuit for back-to-back cable switching

Key	
E_m	Crest of applied voltage
E_t	Trapped voltage on cable being switched
Z_1, Z_2	Cable surge impedance
L	Total inductance between cable terminals
CB	Circuit-breaker

The initial pulse of current has a front expressed as

$$i(t) = \frac{E_m - E_t}{Z_1 + Z_2}\left[1 - \exp(-\frac{Z_1 + Z_2}{L}t)\right] \quad (46)$$

Assuming that the $L/(Z_1 + Z_2)$ time constant is less than 1/5 of the travel time of the cable out and back, the initial crest of the inrush current is then $(E_m - E_t)/(Z_1 + Z_2)$, which for application should be less than the rated peak inrush current.

The inrush current when energising a cable with another already connected to the bus is given by

$$i_{ipeak} = \frac{E_m - E_t}{Z_1 + Z_2} \quad (47)$$

and

$$f_{eq} = f_s\left[\frac{E_m - E_t}{\omega(L_1 + L_2)I_{ir}}\right] \quad (48)$$

The inrush current when energising a cable with an equal cable already connected to the bus is given by

$$i_{ipeak} = \frac{E_m - E_t}{2Z} \quad \text{(A/s)} \quad (49)$$

and

$$f_{eq} = f_s \left[\frac{E_m - E_t}{\omega(L_1 + L_2) I_{ir}} \right] \quad \text{(Hz)} \qquad (50)$$

Differentiating the expression for the current at t = 0, will give the maximum initial rate of change of the inrush current, in equation

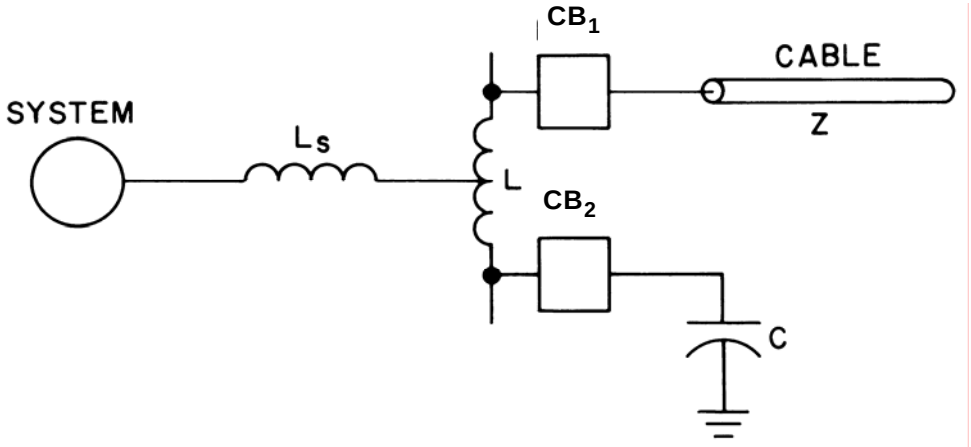
$$\left(\frac{di}{dt} \right)_0 = \frac{E_m - E_t}{L} \quad \text{(A/s)} \qquad (51)$$

This can reach extreme values since the magnitude of L can be arbitrarily small.

Additional inductance may be added in series with the inductances making up L to meet the rated inrush frequency requirement.

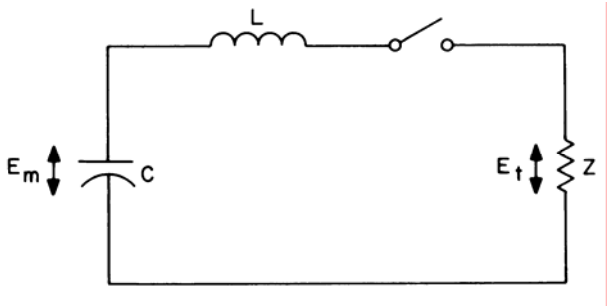
8.2.2.5.3 Alternate Configurations

Other combinations of circuit elements can produce inrush currents associated with cable switching. For example, a cable can be switched from a bus which has a capacitor bank connected as shown in Figure 33. The inrush current can be calculated using the equivalent circuit of Figure 34.



Key	
CB_1	Cable circuit-breaker
CB_2	Capacitor bank circuit-breaker
L_S	Source inductance
L	Total inductance between bank and cable
Z	Cable surge impedance
C	Capacitance of bank

Figure 33 - Bank-to-cable switching circuit



Key

E_m	crest of applied voltage
E_t	trapped voltage on cable being switched
Z	cable surge impedance
L	circuit inductance between bank and cable
C	capacitance of bank

Figure 34 - Equivalent bank-to-cable switching circuit

The maximum initial rate of change of current is given by the expression

$$\left(\frac{\mathrm{d}i}{\mathrm{d}t}\right)_0 = \frac{E_m - E_t}{L} \quad \text{(A/s)} \qquad (52)$$

and, as before, is limited by the loop inductance L. The equivalent frequency is determined as in 8.2.2.5.1, and required adjustments can be made by increasing the value of L (e.g. insertion of a reactor).

The form of the inrush current is a function of the circuit parameters which, in the equivalent circuit, form a series RLC circuit. Using standard methods of analysis, the maximum peak inrush currents are

$$\frac{Z^2}{4} = \frac{L}{C} \qquad i_{\text{ipeak}} = 0{,}368\frac{E_m - E_t}{Z} \qquad (53)$$

$$\frac{Z^2}{4} < \frac{L}{C} \qquad i_{\text{ipeak}} \approx \frac{E_m - E_t}{\sqrt{L/C - Z^2/4}}\left[\exp\left(-\frac{Z\pi}{4L}\frac{1}{\sqrt{L/C - Z^2/4}}\right)\right] \qquad (54)$$

$$\frac{Z^2}{4} > \frac{L}{C} \qquad i_{\text{ipeak}} = \frac{E_m - E_t}{\sqrt{L/C - Z^2/4}}\left[\exp(-\alpha t_m) - \exp(-\beta t_m)\right] \qquad (55)$$

where

$$t_m = \frac{\ln \alpha/\beta}{\alpha - \beta} \qquad (56)$$

$$\alpha = \frac{Z}{L} - \sqrt{\frac{Z^2}{L^2} - \frac{4}{LC}} \qquad (57)$$

$$\beta = \frac{Z}{L} + \sqrt{\frac{Z^2}{L^2} - \frac{4}{LC}} \qquad (58)$$

For application, the peak inrush current should be checked against the capability of the circuit-breaker in question.

Many other combinations of banks, cables, and lines will occur in practice. For example, a cable may be used to exit from a substation and then connect to an overhead line after a short distance. One possible approach when considering circuits of this type is to compare the relative contributions of the cable and the line. For short cable runs this circuit could be considered the equivalent of a line with a capacitor to earth replacing the cable. Similar simplifications can be used for other configurations.

8.2.2.6 Energisation and re-energisation of overhead lines

When an overhead line is switched onto an energised network, a voltage wave is imposed on the line. The resulting phenomena are similar to those of energising a cable. The imposed wave will be reflected at the far end of the line and when the line is open at the far end (or terminated by a high impedance load for high frequencies), the reflected wave results in doubling of the amplitude as shown in Figure 35.

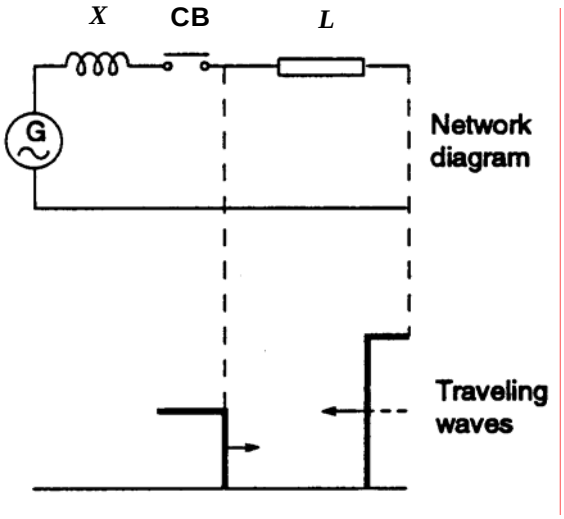


Figure 35 - Energisation of no-load lines: basic phenomena.

An even higher voltage is obtained when the line has a trapped charge before being energised and the circuit-breaker happens to close at an instant when the polarity of the network voltage is opposite to that of the voltage that was present on the line. The voltage on the line can, after reflection of the wave, theoretically be up to three times the network voltage. This situation can occur in conjunction with auto-reclosing of a line.

Even higher voltages can develop on a three-phase line, when the three circuit-breaker poles are not closing simultaneously. A wave on one phase will then generate induced waves on the other phases and under unfavourable circumstances this can lead to a further rise in voltage on another phase.

An efficient way of reducing the overvoltages during energisation and re-energisation of no-load lines is to equip the circuit-breaker with pre-insertion resistors to ensure that the closing takes place in two stages. A pre-insertion resistor is a device that connects a resistor in series with the overhead line at a predetermined time before the closing of the main contacts of the circuit-breaker (see Figure 36).

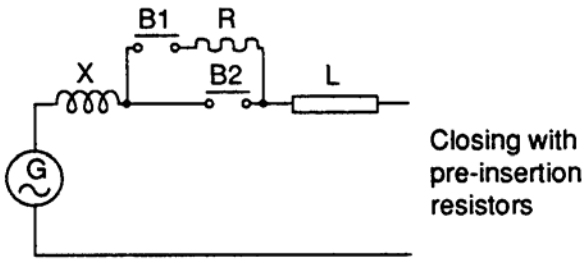


Figure 36 - Pre-insertion resistors and their function

In the first stage of closing, a resistor is switched in series with the line and a voltage division is obtained. This reduces the amplitude of the imposed wave on the line.

In the second stage, the main contacts close and at the same time the resistor is short-circuited. This gives rise to a new wave on the line, but the amplitude of this wave is also reduced. The resistor contacts are reset (opened) before the main contacts are opened.

The optimum value of the resistance of the pre-insertion resistor is usually of the same order of magnitude as that of the surge impedance of the line. The insertion time should be 6 - 8 ms in order to be effective.

Surge arresters have also been successfully used to control voltage transients when energising transmission lines. Refer to IEEE C62.22 [3].

Another way of reducing overvoltages is using controlled closing see also 8.3.8.

8.3 General application considerations

The capacitive current switching capability of the circuit-breaker is depending on its rated voltage, rated frequency, the particular application (i.e. overhead line, capacitor bank, etc.) and the earthing conditions of the network.

Caution should be exercised when applying older circuit-breakers that have not been tested to IEC 62271-100.

8.3.1 Maximum voltage for application

The operating voltage should not exceed the rated voltage since this is the upper limit for operation.

8.3.2 Rated frequency

The rated frequency for circuit-breakers is 50 or 60 Hz. As described in 8.2.1.1.2 a rated frequency of 60 Hz results in a more severe stress on the circuit-breaker, since the voltage peak occurs earlier (at 8,3 ms) than in the case of 50 Hz (10 ms).

Special consideration should be given when comparing tests performed at 60 Hz to cover 50 Hz requirements or vice versa. At lower frequencies, the capacitance current switching ability will be adequate. The switching capability demonstrated at 60 Hz covers the requirements for 50 Hz with the same voltage factor.

8.3.3 Rated capacitive current

The preferred values of the rated capacitive switching current are given in Table 5 of IEC 62271-100. Not all actual cases of capacitive current switching are covered by that table. The values for lines and cables cover most cases, the values of the current for capacitor banks (single and back-to-back) are typical and representative of actual values in service.

8.3.3.1 Overhead lines and cables

When very long lines and cables are considered, the no-load current may exceed that given in Table 5 of IEC 62271-100.

The following may serve as an example: The no-load current of an overhead line is approximately 1,1 A/km at 50 Hz and 1,3 A/km for 60 Hz. Without considering the Ferranti effect (see 8.2.1.3.3), the charging current of a 500 km line would be 605 A at 50 Hz and 715 A at 60 Hz. Ferranti rise on a 500 km line would increase the charging current by about 4 % at 50 Hz and 6 % at 60 Hz. This is not covered by Table 5 of IEC 62271-100.

The higher current does not pose a problem for circuit-breakers of present design, but the possible peak recovery voltage present on interruption could be a problem (see 8.2.1.3.3).

For altitudes exceeding 1000 m the capacitive current does not have to be corrected, provided that it does not exceed the corrected rated normal current.

8.3.3.2 Capacitor and filter banks

The same remark as given under 8.3.3.1 applies to capacitor and filter bank currents. The current is depending on the size of the capacitor bank and in certain cases the capacitor bank considered may have a current rating higher than that given in Table 5 of IEC 62271-100. This does not pose a problem for circuit-breakers of present design.

8.3.4 Voltage and earthing conditions of the network

Subclause 6.111.7 of IEC 62271-100 gives the multiplication factors for single-phase tests for the different conditions, refer to 8.2.1.4. They range from 1,0 for solidly earthed systems to 1,7 for non-effectively earthed systems in the presence of single- or two-phase to earth faults.

Both user and manufacturer must be aware of these earthing conditions in order to specify the correct circuit-breaker suitable for the application.

The recovery voltage of a harmonic filter bank may not follow a 1–cos waveshape, but may include harmonic components. The recovery voltage may have a shape as indicated in Figure 37. This needs to be considered when making the proper choice of circuit-breaker. The voltage waveshape as indicated in Figure 37 might cause occasional reignitions that may be acceptable to obtain an economical solution. If they are not acceptable a circuit-breaker of higher performance should be chosen.

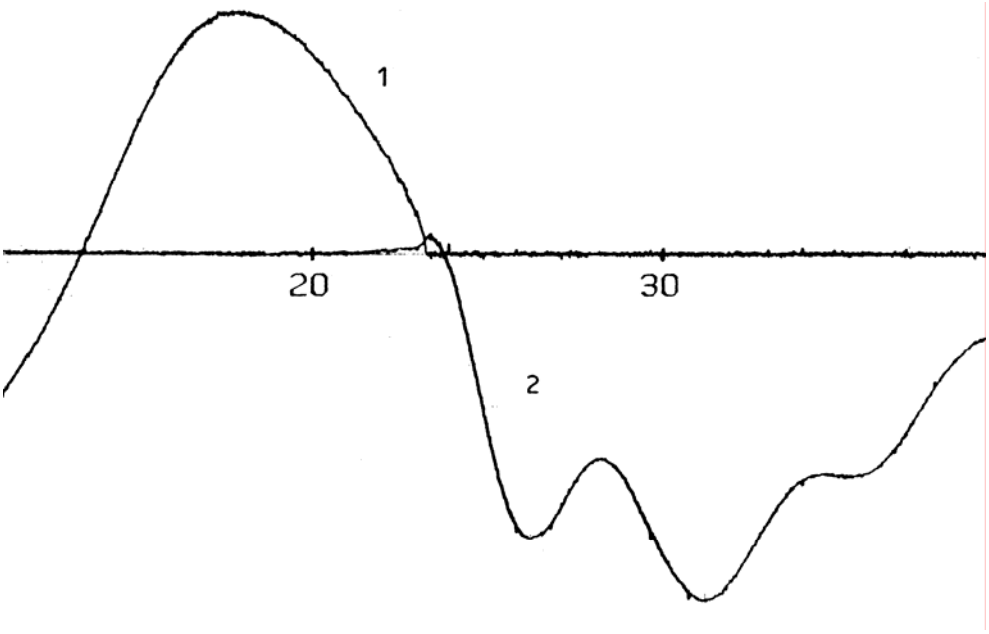


Figure 37 – Example of the recovery voltage across a filter bank circuit-breaker

1 Current through circuit-breaker

2 Voltage across circuit-breaker

8.3.5 Restrike performance

As all circuit-breakers have a certain restrike probability in service, it is not possible to define a restrike-free circuit-breaker. It is more logical to introduce the notion of a restrike performance and this has been done in IEC 62271-100.

The level of the restrike probability depends also on the service conditions (for example number of operations per year, network condition, maintenance policy of the user, etc.). So it is impossible to introduce a common probability level related to service condition.

To classify their restrike performance, two classes of circuit-breakers have been introduced: class C1 and class C2.

8.3.6 Class of circuit-breaker

The choice of the class of circuit-breaker is discussed in 2.2.3 of Part 1 of this application guide.

8.3.7 Interrupting Time

The interrupting time of a circuit-breaker on capacitive current switching is the interval between the energising of the trip circuit at rated control voltage and the interruption of the main circuit in all poles on an opening operation. For some circuit-breakers the time required for interruption may be greater than the rated interrupting time (e.g. oil circuit-breakers). For circuit-breakers equipped with opening resistors, the interrupting time of the resistor current may be longer. Note also that the interrupting time may be longer for close-open operations.

8.3.8 Transient overvoltages and overvoltage limitation

An important consideration for application of circuit-breakers for capacitive current switching is the transient overvoltage which may be generated by restrikes during the opening operation. The transient overvoltage factor is defined as the ratio of the transient voltage appearing between a circuit-breaker disconnected terminal and the neutral of the

disconnected capacitance during opening to the operating line-to-neutral crest voltage prior to opening.

The selection of the class (see 8.3.6) of circuit-breaker to be applied should be coordinated with the insulation capability of other components on the system.

8.3.8.1 Overvoltages

When switching capacitive currents, transients are generated. These transients are associated with the restrikes when de-energising a capacitive load and with the energisation of capacitive loads. These transients may cause:

- insulation degradation and possible failure of the substation equipment,
- operation of surge arresters;
- interference in the control wiring of the substation;
- increase in step potentials in substations;
- undesired tripping or damage to sensitive electronic equipment.

The magnetic fields associated with high inrush currents during back-to-back switching in either the no-load transmission line conductors or the earthing grid during back-to-back switching can induce voltages in control cables by both capacitive and electromagnetic coupling. These induced voltages can be minimised by shielding the cables and using a radial configuration for circuits (circuits completely contained within one cable so that inductive loops are not formed).

8.3.8.1.1 Switching of capacitor banks

The switching of capacitor banks is associated with voltage and current transients (see 8.2.1.1 and 8.2.2.1). As most modern circuit-breakers have a very low probability of restrike, the majority of the switching transients will be generated when energising capacitor bank(s). The effects of the transients will exhibit themselves locally and at remote locations on the power system.

The high-frequency transient inrush current associated with back-to-back switching can stress other equipment in the circuit as well as the circuit-breaker. Wound-type current transformers will have turn-to-turn insulation stressed because of the high rates of rise of current and the resulting voltage that is developed across inductance in the circuit.

8.3.8.1.1.1 Local effects

- voltage transients resulting in dielectric stresses on nearby equipment;
- electrical, mechanical and electromechanical forces caused by the inrush current.

8.3.8.1.1.2 Remote effects

- transfer of capacitively coupled fast transients through transformer windings;
- reflections of travelling wave transients on open ended lines or transformer terminated lines;
- excitation of near resonant portions of the power system by the oscillatory transient frequency.

8.3.8.1.2 Switching of lines and cables

When energising lines and cables, high overvoltages may be created depending on whether or not the line or cable was precharged as a result of a preceding breaking operation (i.e. in the case of an auto-reclosing). These overvoltages may result in damage of insulation.

8.3.8.2 Overvoltage limitation

There are several means available to reduce the overvoltages generated by the switching of capacitive currents:

- **current limiting reactors** are normally used to reduce the current transients associated with back-to-back switching. They do not limit the remote overvoltages.
- **pre-insertion resistors** limit the inrush current and remote overvoltages. It is a basic solution widely used on circuit-breakers. They are usually fitted on circuit-breakers and as such add to the complexity of the equipment. Depending on the design, the added complexity may or may not result in a reduced availability of the equipment (see also 8.3.16).
- **pre-insertion reactors** also limit the inrush current and remote overvoltages. They are usually fitted on circuit-switchers and their effect on complexity and availability of the equipment is sometimes equivalent to pre-insertion resistors, depending on the design of the devices.
- **controlled closing** reduces the magnitude of the inrush current depending on the point-on-wave of the voltage prior to the prestrike between the contacts. A simple way of reducing the transients is to let the circuit-breaker contacts close at a voltage zero. This method is called controlled closing. The controller also adds to the complexity of the equipment and can influence its availability.

8.3.9 No-load overhead lines

A circuit-breaker may be required to energise or de-energise an no-load transmission line during its normal operating duties. Prior to energisation, the line may or may not contain a trapped charge (see also 8.2.1.3). Consideration may need to be given to line energisation following load rejection (see [2]).

8.3.9.1 Line charging current

When considering the assigned line charging current rating, application is determined by the value of the line charging current. This current is a function of system voltage, line length, and line configuration.

Figure 38 gives an approximation of the line charging current per kilometre of different line configurations at 60 Hz. If the estimated current is greater than 90 % of the preferred line current rating, a more accurate calculation based on the actual line configuration and methods similar to that discussed in [1] should be used.

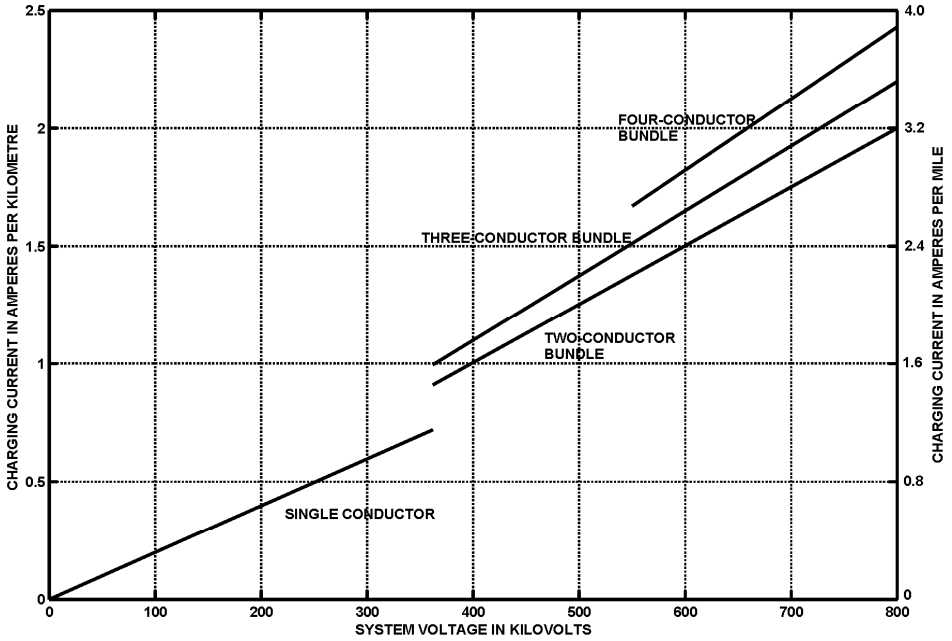


Figure 38 - RMS charging current versus system voltage for different line configurations at 60 Hz

From Figure 38 the capacitive reactance can be derived as follows:

Assume a system with a rated voltage of 245 kV, 60 Hz. The charging current is 0,5 A/km. The linear capacitive reactance X_C' is then:

$$X_C' = \frac{1}{\omega C'} = \frac{U}{I'} = \frac{245000\ \text{V}}{\sqrt{3} \times 0{,}5\ \text{A/km}} = 0{,}283\ \text{M}\Omega\,\text{km},$$

with X_C' linear capacitive reactance of the line in MΩ km

C' capacitance of the line in F/km

I' charging current of the line in A/km

For a 50 Hz system frequency the corresponding value of X_C' would be $0{,}283 \times \frac{60}{50} = 0{,}34\ \text{M}\Omega\,\text{km}$

To calculate the reactance X_C of a line with a given length l the linear reactance X_C' has to be divided by the length:

$$X_C = \frac{X_C'}{l}$$

Assume a length of 100 km for the example above. The reactance X_C is then:

$$X_C = \frac{X'_C}{l} = \frac{0{,}83\ \text{M}\Omega\text{km}}{100\ \text{km}} = 2{,}83\ \text{k}\Omega\ .$$

8.3.9.2 Compensated overhead lines

As described in 8.2.1.3.2, very long lines (> 200 km) are often compensated with shunt reactors to reduce the amount of charging current required of the system.

If the circuit-breaker rating is chosen based on I_{lc}, the line could not be switched without the compensating reactor(s) connected. The voltage rise caused by the Ferranti effect and also the location of the reactor(s) will change the line current slightly.

8.3.9.3 No-load line recovery voltage

The line-charging breaking current rating is assigned on the basis of a standard recovery voltage associated with this type of circuit. For solidly earthed systems, the no-load line charging current switching tests require a maximum voltage of 2,4 times (see also 8.2.1.3.1.2) the rated phase-to-earth voltage across the circuit-breaker one half-cycle after interruption (assumes C_1 = $2C_0$ where C_1 is the positive-sequence capacitance and C_0 is the zero-sequence capacitance). This is the difference voltage of the source and line sides, including the effects of coupled voltage on the first pole-to-clear. The test voltage requires a 1-cosine waveshape.

For double circuit lines with higher voltage factors refer to 8.2.1.4.

Deviations from the test voltage characteristics may increase or decrease the probability of the circuit-breaker restriking. As described in 8.2.1.3.2, a compensated line will have a lower peak of the recovery voltage, which will reduce the restrike probability.

8.3.10 Capacitor banks

A circuit-breaker may be required to switch a capacitor bank from a bus that does not have other capacitor banks energised (single or isolated) or against a bus that has other capacitor banks energised (back-to-back). In the application of circuit-breakers for capacitor switching duty, consideration must be given to the rated single (isolated) shunt capacitor bank switching current, rated back-to-back shunt capacitor bank switching current, rated transient inrush current, and rated transient inrush current frequency (see also 8.2.1.1 and 8.2.2.1).

8.3.10.1 Capacitor bank current

Circuit-breakers are to be applied according to the actual capacitive current they are required to interrupt. The rating should be selected to include the following effects.

a) *Voltage.* The reactive power rating of the capacitor bank, in kvar, is to be multiplied by the ratio of the maximum service voltage to the capacitor bank nameplate voltage when calculating the capacitive current at the applied voltage. This ratio can be as large as 1,1, since capacitors can be operated continuously up to 10 % above the capacitor rated voltage.

b) *Capacitor Tolerance.* The manufacturing tolerance in capacitance is -0 to +15 % with a more frequent average of -0 to +5 %. A multiplier in the range of 1,05 to 1,15 should be used to adjust the nominal current to the value allowed by tolerance in capacitance.

c) *Harmonic Component.* Capacitor banks provide a low-impedance path for the flow of harmonic currents. When capacitor banks are non-effectively earthed, no path is provided for zero-sequence harmonics (third, sixth, ninth, etc), and the multiplier for harmonic currents is less. A multiplier of 1,1 is generally used for a solidly earthed neutral bank and 1,05 for a non-effectively earthed neutral.

In the absence of specific information on multipliers for the above factors, it will usually be conservative to use a total multiplier of 1,25 times the nominal capacitor current at rated capacitor voltage for non-effectively earthed neutral operation and 1,35 times the nominal current for solidly earthed neutral operation.

8.3.10.2 Methods for calculating transient inrush currents

8.3.10.2.1 Single or isolated capacitor bank

A bank of shunt capacitors is considered single (isolated) when the conditions described in 8.2.2.1.1 are fulfilled. Table 6 gives the equations that apply for calculation of the inrush current for single (isolated) capacitor bank energisation.

8.3.10.2.2 Back-to-back capacitor bank

The inrush current of a single bank will be increased when other capacitor banks are connected to the same bus (see also 8.2.2.1.2).

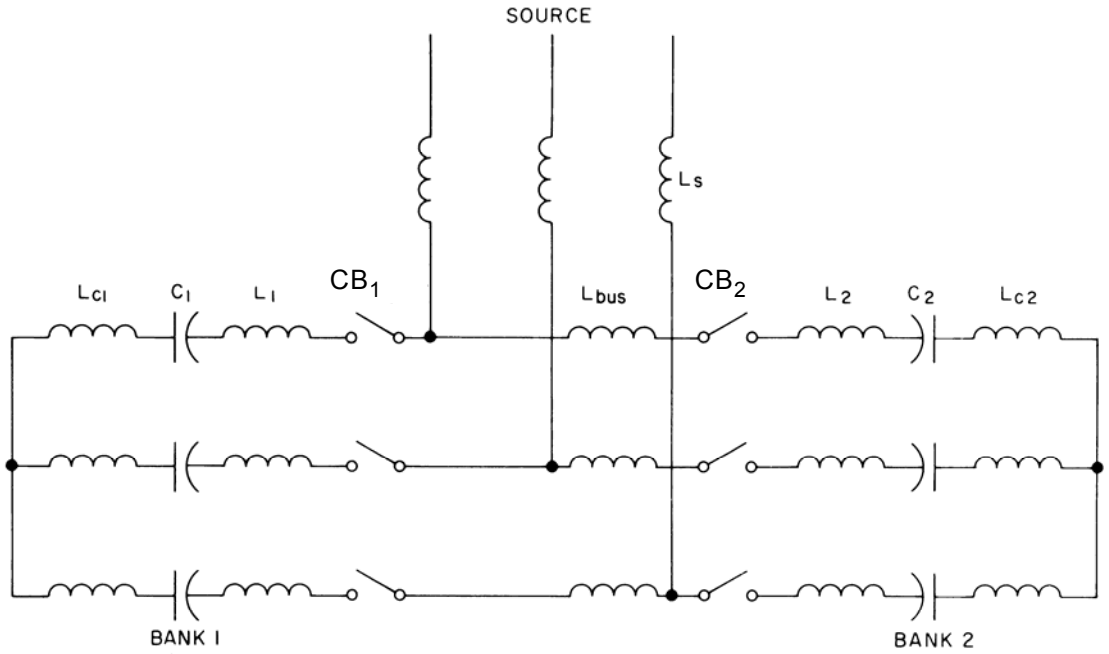
Table 6 gives the equations for calculating inrush current and frequency for both isolated and back-to-back capacitor bank switching, neglecting resistance. These equations are based on the theory described in 8.2.2.1.

A typical circuit for back-to-back switching is shown in Figure 39. The inductance in the circuit that limits the transient oscillatory current is composed of the inductance of the bus between switching devices, L_{bus}, the inductance between the switching device and the capacitor banks, L_1 and L_2, and the inductance of the capacitor banks, L_{c1} and L_{c2} and any additional reactance inserted. The total inductance between capacitor banks, $L_{c1} + L_1 + L_{bus} + L_2 + L_{c2}$, is very small with respect to the inductance of the source L_s. In most cases, the total inductance between capacitor banks will be less than 1 % of the inductance of the source, and the contribution of transient current from the source can be neglected.

The inductance of the bus can be calculated similar to a transmission line using values from tables available from suppliers of bus conductors for different bus configurations. (See 8.3.10.2.3)

The inductance within the capacitor bank itself is not easy to obtain, but in general it is of the order of 10 μH for banks above 52 kV, and 5 μH for banks below 52 kV. Typical values of inductance per phase between back-to-back capacitor banks and bank inductance for various voltage levels are given in Table 7.

Inherent resistance of the circuit causes rapid decay of the transient current so that the first peak actually may only reach 90 % to 95 % of the maximum value calculated. These values are applicable to both solidly earthed or non-effectively earthed banks and with Y or Δ connections. With a non-effectively earthed neutral, the current in the first two phases to close will be 87 % of calculated, but the current in the last phase will equal the value calculated. However, inherent resistance of the circuit will affect these currents by the factors indicated above.



Key

CB_1	circuit-breaker energising capacitor bank 1
CB_2	circuit-breaker energising capacitor bank 2
L_S	source inductance
L_{C1}, L_{C2}	capacitor bank inductance
L_1, L_2	bus inductance between switching device and capacitor bank
L_{bus}	inductance of bus between switching devices

Figure 39 - Typical circuit for back-to-back switching

The equations in Table 6 for back-to-back switching will give correct results when switching a bank against another bank. However, when switching against several other banks connected to the bus, the correct value of equivalent inductance to be used for the combination of banks connected to the bus is not easily obtained. For example, when switching a bank against three other banks energised on the bus, the calculated current will be too high if an inductance of $L/3$ is used. On the other hand, using a value of $3L$ will result in a current which is too low. If exact solutions cannot be made, conservative results should be used in calculating inrush currents by using the inductance divided by the number of capacitor banks, recognising that the results will be 20 to 30 % higher (see also 8.2.2.1.2).

Table 6 - Inrush current and frequency for switching capacitor banks

Condition	Quantity	When using currents
Energising an isolated bank	$i_{\text{i peak}}$ (A)	$1{,}41\sqrt{I_{\text{sc}} \times I_1}$
	f_{i} (Hz)	$f_{\text{s}}\sqrt{\frac{I_{\text{sc}}}{I_1}}$
Energising a bank with another on the same bus	$i_{\text{i peak}}$ (A)	$13\,500\sqrt{\frac{U_{\text{r}} I_1 I_2}{f_{\text{s}} L_{\text{eq}} (I_1 + I_2)}}$
	f_{i} (kHz)	$9{,}5\sqrt{\frac{f_{\text{s}} U_{\text{r}} (I_1 + I_2)}{L_{\text{eq}} (I_1 \times I_2)}}$
Energising a bank with an equal bank energised on the same bus	$i_{\text{i peak}}$ (A)	$9545\sqrt{\frac{U_{\text{r}} I_1}{f_{\text{s}} L_{\text{eq}}}}$
	f_{i} (kHz)	$13{,}5\sqrt{\frac{f_{\text{s}} U_{\text{r}}}{L_{\text{eq}} I_1}}$

f_{s} = system frequency (Hz)

L_{eq} = total equivalent inductance per phase between capacitor banks, in μH

I_1, I_2 = currents (in A) of banks being switched and of bank already energised, respectively. Capacitor bank being switched is assumed uncharged, with closing at a voltage crest of the source voltage. The current used should include the effect of operating the capacitor bank at a voltage above nominal rating of the capacitors and the effect of a positive tolerance of capacitance. In the absence of specific information, a multiplier of 1,15 times normal capacitor current would give conservative results

$I_{\text{i peak}}$ = peak value calculated without damping. In practical circuits it will be about 90 % of this value

U_{r} = rated voltage in kV

I_{sc} = symmetrical short-circuit current, in A r.m.s.

8.3.10.2.3 Considerations for transient inrush currents

The inrush currents of different types of compact multi-section banks with minimum spacing between the individual sections may differ by as much as 20 %. Consequently, these inrush currents can be reduced significantly by increasing the lengths (inductance) of the circuits between the sections.

Table 7 - Typical values of inductance between capacitor banks

Rated maximum voltage (kV)	Inductance per phase of busbar (μH/m)	Typical inductance between banks [a] (μH)
17,5 and below	0,702	10-20
36	0,781	15-30
52	0,840	20-40
72,5	0,840	25-50
123	0,856	35-70
145	0,856	40-80
170	0,879	60-120
245	0,935	85-170

[a] Typical values of inductance per phase between capacitor banks. This does not include inductance of the capacitor bank itself. Values of 5 μH for banks below 52 kV and 10 μH for banks above 52 kV are typical for the inductance of the capacitor banks.

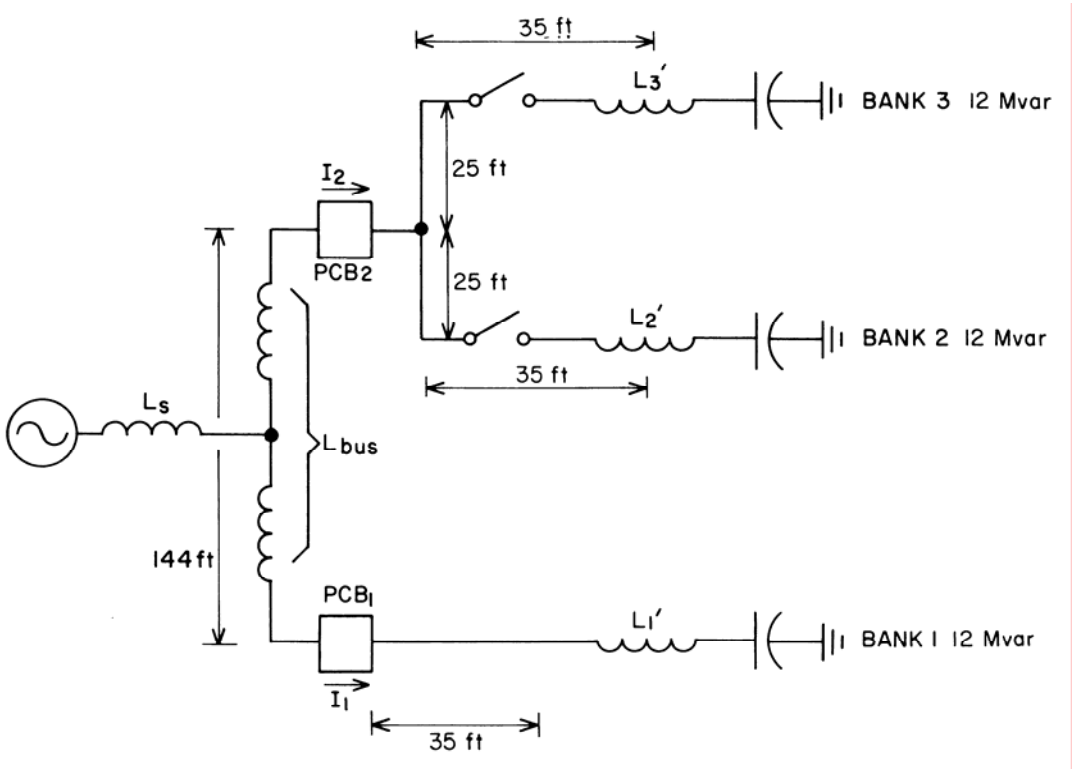
Another effective measure to reduce transient inrush currents is to add inductance in the circuit between the capacitor banks.

The capability of circuit-breakers to handle inrush current is often expressed in terms of the product of inrush current peak times the inrush current frequency, $i_{\text{i peak}} \times f_{\text{i}}$ (kAkHz).

Although circuit-breakers have usually been tested with inrush currents up to 25 kA_{peak} and 4 kHz, system designers should endeavour to keep the inrush currents far below this value for system quality reasons.

The following example will illustrate the use of the equations in Table 6.

A 115 kV system is assumed as shown in Figure 40.



Key

U_r	123 kV (115 kV nominal voltage)
L_S	source inductance, = 3,77 Ω, 10 mH (f_s = 60 Hz)
L_1', L_2', L_3'	inductance between circuit-breaker and capacitor bank; including inductance of capacitor bank
L_{bus}	inductance of bus between switching devices
PCB1, PCB2	Circuit-breakers
	short-circuit of source: 18 600 A at 123 kV

Figure 40 - Example of 115 kV system

The capacitor banks shown have a nominal rating of 12 Mvar (capacitors rated 100 kvar, 13,28 kV, five series sections with eight capacitors in parallel). Nominal current per bank is 60 A. In determining the rating of the circuit-breaker required, the increase in current due to applied voltage, capacitance tolerance, and harmonics should be considered. The increase in current at maximum rated voltage is: maximum voltage to capacitor rated voltage = 123/115 = 1,07. Assume a positive tolerance of capacitors of +10 %, multiplier of 1,1 and assume a multiplier for harmonic content for a solidly earthed neutral bank of 1,1.

The total multiplier used to determine the single (isolated) and back-to-back current rating is 1,07 x 1,1 x 1,1 = 1,29, giving a current of 1,29 x 60 = 78 A. With capacitor banks 2 and 3 energised, the current through PCB_2 is 156 A.

The circuit-breakers intended for this duty have the following ratings: rated voltage 123 kV, rated current 1600 A, rated short-circuit current 40 kA, rated single (isolated) and back-to-back capacitive switching current 400 A.

The transient inrush current and frequency are calculated using the equations in Table 6. In the example, L_1', L_2' and L_3' are the inductances between the respective capacitor banks and the circuit-breakers, including the inductance of the capacitor bank. L_{bus} is the inductance of the bus between the circuit-breakers.

The inductance values in Table 7 can be used or values can be calculated for the actual bus configuration used. In the example given below, the added reactance between the circuit-breaker and capacitor bank is:

L_1' = 20,0 μH

L_2' = L_3' = 27,1 μH

The reactance of the busbar L_{bus} = 37,6 μH.

In determining inrush current and frequency, the currents I_1 and I_2 as used in Table 6 should include the effect of operating the capacitor bank at a voltage above nominal rating of the capacitors and the effect of a positive tolerance of capacitance. In the example, the multiplier to be used is 1,07×1,1 = 1,18. The currents are I_1 = 60×1,18 = 71 A and I_2 = 71 A or 142 A, depending on whether bank 2 or 3 or both banks are energised.

Case I. Energisation of capacitor bank 1 with banks 2 and 3 not energised (single or isolated bank switching),

$$i_{\text{max peak}} = 1{,}4\sqrt{I_{\text{sc}} \times I_1} = 1{,}4\sqrt{18\,600 \times 71} = 1{,}4\sqrt{132 \times 10^4} = 1625 \text{ A}$$

$$f_{\text{i}} = f_{\text{s}}\sqrt{\frac{I_{\text{sc}}}{I_1}} = 60\sqrt{\frac{18\,600}{71}} = 971 \text{ Hz}$$

The calculated rate of change of current for the single (isolated) bank switching is

$$\left(\frac{\text{d}i_{\text{i}}}{\text{d}t}\right)_{\text{max}} = 2\pi f_{\text{i}} i_{\text{i peak}} = 2\pi \times 971 \times 1625 = 9{,}9 \text{ A/μs}$$

This is less than the maximum rate of change for a rated short-circuit current of 40 kA which is equal to $2\pi f_{\text{s}}\sqrt{2}\,I_{\text{sc}} = 21{,}3$ A/μs and therefore meets the requirements of isolated capacitor bank switching.

Case II. Energisation of bank 1 with bank 2 energised on the bus (back-to-back switching against an equal-size bank),

$$i_{\text{i peak}} = 9545\sqrt{\frac{U_{\text{r}} I_1}{f_{\text{s}} L_{\text{eq}}}}$$

The equivalent inductance L_{eq}, is the sum of L_1' + L_{bus} + L_2' = 20,0 + 37,6 + 27,1 = 84,7 μH.

$$i_{\text{max peak}} = 9545\sqrt{\frac{123\times 71}{60\times 84{,}7}} = 9545\sqrt{111} = 12\,512\ \text{A}_{\text{peak}}$$

$$f_{\text{i}} = 13{,}5\sqrt{\frac{f_{\text{s}}U_{\text{r}}}{L_{\text{eq}}I_1}} = 13{,}5\sqrt{\frac{60\times 123}{84{,}7\times 71}} = 15{,}0\ \text{kHz}$$

The calculated back-to-back inrush current and frequency must be compared with the back-to-back switching capability listed in Table 5 of IEC 62271-100. For a maximum voltage of 123 kV, the assumed rated values are 20 kA_{peak} and 4,25 kHz. The calculated value of the inrush current peak is within this rating, the inrush current frequency exceeds that assumed and inductance must be added between the capacitor banks to reduce the inrush current frequency. Adding an inductance of 1 mH will limit the inrush current to approximately 3,5 kA and the frequency to approximately 4,18 kHz, both of which are below the assumed capability.

Case III. Energisation of bank 1 with banks 2 and 3 energised on the bus. For this case, assume the equivalent inductance of banks 2 and 3 equal to one half of L_2' or (27,1)/2 = 13,6 μH. The total current of banks 2 and 3 is 142 A, which is under the assumed isolated bank switching capability of 400 A as listed in Table 5 of IEC 62271-100. For this case, I_1 = 71 A, I_2 = 142 A, and the equivalent inductance between the capacitor bank being energised and the banks already energised is the sum of L_2'/2 + L_{bus} + L_1' = 13,6 + 37,6 + 20 = 71,2 μH.

$$i_{\text{i peak}} = 13\,500\sqrt{\frac{U_{\text{r}}(I_1\times I_2)}{f_{\text{s}}L_{\text{eq}}(I_1+I_2)}} = 13\,500\sqrt{\frac{123\times 71\times 142}{60\times 71{,}2\times 213}} = 15\,760\ \text{kA}_{\text{peak}}$$

and

$$f_{\text{i}} = 9{,}5\sqrt{\frac{f_{\text{s}}U_{\text{r}}(I_1+I_2)}{L_{\text{eq}}(I_1\times I_2)}} = 9{,}5\sqrt{\frac{60\times 123\times 213}{71{,}2\times 71\times 142}} = 14{,}1\ \text{kHz}$$

Of the calculated values of inrush current peak and frequency, the frequency of 14,1 kHz exceeds the assumed back-to-back switching capability of 4,25 kHz listed in Table 5 of IEC 62271-100. As in the previous case of switching identical banks, adding an inductance of 0,71 mH will limit the inrush current and frequency to approximately 4,7 kA_{peak} and 4,24 kHz, respectively, both of which are below the assumed back-to-back switching capability of 123 kV circuit-breaker.

Based on the system and conditions studied, a circuit-breaker having the following ratings would be applied: rated short-circuit current of 40 kA and rated isolated capacitor bank switching current of 400 A. The assumed back-to-back rating of 20 kA and 4250 Hz that goes with this rating will be exceeded unless additional inductance is added between the capacitor banks. A value of 0,71 mH is sufficient to keep within the assumed ratings available.

8.3.11 Cables

In the application of circuit-breakers for cable switching duty, consideration must be given to the rated single (isolated) cable switching current, the rated back-to-back cable switching current, and the rated transient inrush current, both amplitude and frequency.

8.3.11.1 Cable inrush current

Table 8 gives a summary of the equations that are applicable for the different configurations.

Table 8 - Frequency and current amplitude relations

Condition	Quantity	When using surge impedance
Energising an isolated cable	$i_{\text{i peak}}$	$\frac{E_{\text{m}} - E_{\text{t}}}{Z}$
	F_{eq}	$f_{\text{s}}\left[\frac{\sqrt{2}I_{\text{sc}}}{I_{\text{MR}}}\right]$
Energising a cable with another on the same bus	$i_{\text{i peak}}$	$\frac{E_{\text{m}} - E_{\text{t}}}{Z_1 + Z_2}$
	F_{eq}	$f_{\text{s}}\left[\frac{E_{\text{m}} - E_{\text{t}}}{\omega(L_1 + L_2)I_{\text{MR}}}\right]$
Energising a cable with an equal cable energised on the same bus	$i_{\text{i peak}}$	$\frac{E_{\text{m}} - E_{\text{t}}}{2Z}$
	f_{eq}	$f_{\text{s}}\left[\frac{E_{\text{m}} - E_{\text{t}}}{\omega(L_1 + L_2)I_{\text{MR}}}\right]$

For proper circuit-breaker application, f_{eq} should be less than the rated inrush current frequency. Additional inductance may be added in series with the inductances making up L to meet the rated inrush frequency requirement. Such inrush reactors are common.

8.3.11.2 Alternate configurations

Other combinations of circuit elements can produce inrush currents associated with cable switching. For example, a cable can be switched from a bus which has a capacitor bank connected as shown in 8.2.2.5.3.

For application, the peak inrush current should be checked against the rated value for the circuit-breaker in question.

Many other combinations of banks, cables, and lines will occur in practice. For example, a cable may be used to exit from a substation and then connect to an overhead line after a short distance. One possible approach when considering circuits of this type is to compare the relative contributions of the cable and the line. For short cable runs this circuit could be considered the equivalent of a line with a capacitor to earth replacing the cable. Similar simplifications can be used for other configurations.

8.3.12 Switching through transformers

Circuit-breakers may be required in some applications to switch capacitors, lines, or cables through an interposed transformer. The current switched by the circuit-breaker will be N times the capacitor, line, or cable current on the other side of the transformer, where N is the transformer turns ratio.

Switching charging current through a transformer may be less difficult than switching the same current directly. The capacitive elements of the circuit will oscillate with the transformer inductance, which may also saturate, producing a less severe transient recovery voltage and a lower probability of restrike. If a restrike should occur, the additional inductance will help to limit the inrush current.

If the value of N is greater than 1, switching through a transformer will have the effect of increasing the current being switched. De-energising no-load overhead lines with lower voltage circuit-breakers can result in effective line charging currents in the 750-1000 A range. The capacitive switching rating of circuit-breakers which may be exposed to this type of duty must be carefully checked before application is made.

Voltage and current relations are shown in Figure 41 as an example of capacitor switching through an interposed transformer. It can be seen that due to the reduced recovery voltage, the increased current is not a problem for the circuit-breaker.

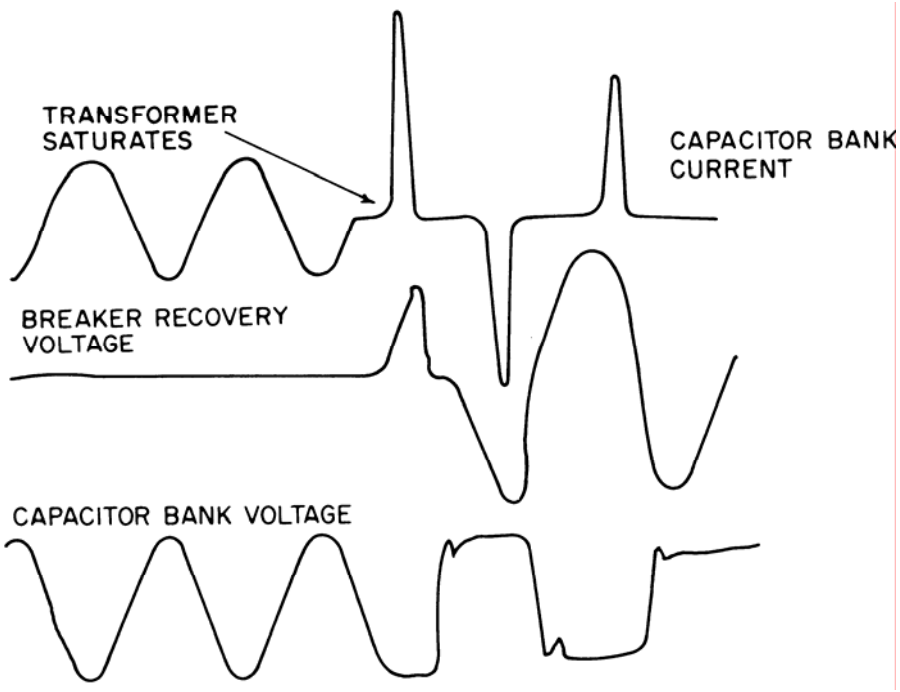


Figure 41 - Voltage and current relations for capacitor switching through interposed transformer

8.3.13 Unusual circuits

In the application of circuit-breakers in stations having banks of capacitors it may be necessary to investigate the effects of transient currents and other special situations upon circuit-breakers other than those specially equipped for and assigned to the routine capacitor switching.

The transient currents of capacitor banks may be considered in two aspects: the inrush currents upon energising of the banks and the discharge currents into faults. Where the quantity of parallel capacitor banks installed in a station is large, the transient currents may have significant effects upon the circuit-breaker.

The transient currents may have large peaks and high frequencies which may affect circuit-breakers in the following ways.

a) A circuit-breaker may be subjected to a transient inrush current which exceeds its rating. This may occur with the circuit-breaker in the closed position or when closing into solidly earthed faults.

b) The transient inrush current may have sufficient magnitude and rate of change to flash over the secondaries of linear couplers (a transducer having a linear relationship between input and output) or bushing current transformers as used in dead tank circuit-breakers, or the associated control wiring.

There are also special situations that may arise in fault switching sequences where circuit-breakers in a station others than those assigned to the capacitive switching duty may get involved in unplanned clearing of energised parallel banks. This section is intended to guide the engineer to take either the required corrective measures or to avoid the problems.

8.3.13.1 Exposure to transient inrush currents

Circuit-breakers located in a position such as a tie circuit-breaker between bus sections (bus section or bus coupler) may be exposed to the transient inrush currents from energising banks of capacitors when they are located on bus sections on both sides of the circuit-breaker (see Figure 42, CB_1).

Seldom will the inrush current exceed the capability of the circuit-breaker. However, a check may be required to determine if the rate of change of inrush current will cause overvoltages on the secondary of linear couplers or current transformers on the circuit-breaker or in the current path between the capacitor banks.

NOTE Appropriately sized metal oxide varistors can be used to clamp these secondary overvoltages.

With linear couplers, the secondary voltage induced across the terminals from the transient capacitive current is proportional to the frequency and to the amplitude of this current as shown in the following equation:

linear coupler secondary volts (crest) = (linear coupler ratio) × (transient frequency)/(system frequency) × (crest transient current)

The following example will illustrate the use of the above equation.

Linear coupler ratio	5 V per 1000 primary A
Frequency of transient inrush current	5400 Hz
Crest of transient inrush current	30 000 A
System frequency	60 Hz

$$\text{linear coupler secondary volts (crest)} = \frac{5}{1000} \times \frac{5400}{60} \times 30\,000 = 13\,500 \text{ V}$$

Manufacturer's voltage limits for linear couplers should not be exceeded.

With a bushing-type current transformer (BCT), the voltage developed in the secondary circuit is also proportional to the frequency and the amplitude of the transient inrush current, as shown in the following equation:

Voltage in BCT secondary (crest) = 1/(BCT ratio) × (crest transient current) × (relay reactance) × (transient frequency)/(system frequency)

The following example will illustrate the use of the above equation.

Bushing current transformer ratio	1000/5
Frequency of transient inrush current	5400 Hz
Crest of transient inrush current	30 000 A
Relay reactance burden at 60 Hz	0,3 Ω
System frequency	60 Hz
Voltage in BCT secondary (crest)	5/1000 × 30 000 × 0,3 × 5400/60 = 4050 V

The secondary voltage should not exceed those values specified in the relevant transducer standard.

8.3.13.2 Exposure to total capacitor bank discharge current

In a substation where parallel capacitor banks are located near or on a busbar, any circuit-breaker connected to the bus may be exposed during faults to the total discharge current of all the banks located behind the circuit-breaker. In Figure 42, CB_2 will be subjected to this total discharge current with a fault occurring at location A. The worst case, or highest capacitor discharge current, occurs with a bolted three-phase fault where capacitor banks are non-effectively earthed and for a case of a three-phase-to-earth or a line-to-earth fault where capacitor banks are solidly earthed.

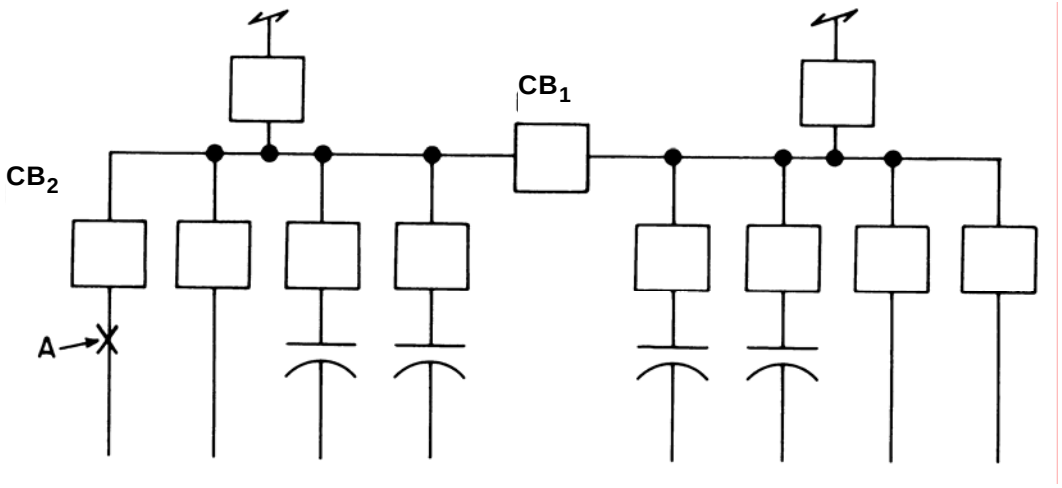


Figure 42 - Station illustrating large transient inrush currents through circuit-breakers from parallel capacitor banks

The total discharge current (peak) of all banks behind the circuit-breaker is equal to the algebraic sum of the individual banks of capacitors. Neglecting resistance, the discharge current of an individual capacitor bank is equal to:

$$I_{\text{d peak}} = \frac{\sqrt{2}}{\sqrt{3}} U_{\text{r}} \sqrt{\frac{C}{L}} \qquad (59)$$

where

$I_{\text{d peak}}$ crest value of discharge current

U_{r} rated voltage

C capacitance per phase of individual bank

L inductance per phase between capacitor bank and fault location.

The inductance L is primarily made up of bus conductors and any additional inductance added to the bank for limiting the inrush currents.

If there are n capacitor banks of approximately equal capacitance and separated by an approximately equal inductance to the fault, then the total discharge current is approximately equal to the sum of the crest current of each bank or n times that of one bank. This is demonstrated as follows:

$$I_{\text{d peak}} = \frac{\sqrt{2}}{\sqrt{3}} U_{\text{r}} \sqrt{\frac{Cn}{L/n}} = \frac{\sqrt{2}}{\sqrt{3}} U_r n \sqrt{C/L} \qquad (60)$$

In addition to the checking of the crest current, it may be necessary also to check the rate of change of the discharge current with the manufacturer.

The transient discharge current passing through a circuit-breaker must also be examined for its effects upon the linear couplers and bushing current transformers. The discharge currents may substantially exceed the magnitudes and the frequency of the inrush currents described in 8.3.13.1. This occurs because the contribution may come from a number of capacitor banks and is not limited by the inrush impedance seen when energising a bank of capacitors. The equations given in 8.3.13.1 for determining the induced voltages in the linear couplers or in bushing current transformers also may be used for determining the effects of the discharge currents.

8.3.13.3 Exposure to capacitive switching duties during fault switching

Where parallel banks of capacitors are located on bus sections in a station, caution must be exercised in the fault switching sequence so that the last circuit-breaker to clear is not subjected to a capacitive switching duty beyond its capability. This is especially a concern for a circuit-breaker used as a bus section tie circuit-breaker with capacitors located on both sides of the circuit-breaker as shown in Figure 42, CB_1.

The worst case occurs in a station where the bus section tie circuit-breaker is last to clear the bus for a fault that leaves one or more phases of the capacitor banks fully energised. In this situation, the bus tie circuit-breaker must be properly equipped and rated for the parallel switching of the capacitor banks remaining on the bus section to be de-energised. In the example of Figure 42, this means that the tie circuit-breaker must be capable of switching two banks of capacitors in parallel with two banks of capacitors on the source side. Another solution is to coordinate if possible the clearing times so that the tie circuit-breaker is always first to clear to avoid the capacitor switching duty.

8.3.14 Effect of load

The situation can occur where a circuit-breaker is called upon to switch a combination of a capacitive current and a load current. The circuit-breaker will have the required switching capability if the total current does not exceed the rated continuous current of the circuit-breaker and either

a) the power factor is at least 0,8 leading, or
b) the capacitive current does not exceed the rated capacitive switching current of the circuit-breaker.

Where the above conditions are exceeded, the capability and performance of the circuit-breaker is not defined by the standards and the manufacturer should be consulted. When the power factor is below 0,8 leading, the voltage may be sufficiently out-of-phase with the current to cause unacceptable restriking. The situation will be more severe if there is also a bank of capacitors located on the source side of the circuit-breaker.

8.3.15 Effect of reclosing

Up to twice normal inrush currents are possible when reclosing is applied to a circuit-breaker switching capacitive loads. When capacitor bank current is interrupted at or near a normal current zero, the voltage remaining on the bank may be near peak value. Reclosing a circuit-breaker against such a charged capacitor bank may produce high inrush current.

When a capacitor bank is connected to the load side of a feeder circuit-breaker equipped with automatic reclosing, high inrush currents can be avoided by isolating the capacitor bank from other loads after the circuit-breaker is tripped and before reclosing. The switching device used for regular capacitor bank switching can be employed for isolation. This technique is particularly recommended where other capacitor banks are connected to the same station bus.

A second technique to avoid high inrush currents during reclosing is to increase reclosing time delay. Normally, the discharge resistors inside each capacitor unit will reduce residual voltage or other deliberately introduced discharging devices (e.g. magnetic voltage transformers).

Discharge curves are available from the capacitor supplier and should be consulted where reclosing time is delayed.

8.3.16 Resistor thermal limitations

For capacitor bank circuit-breakers equipped with preinsertion resistors, the thermal capability of the resistors must be considered in determining the time interval between capacitive current switching operations. The resistance value is related to the size of the capacitor bank and the preinsertion resistors should normally have a thermal capability as defined by the rated duty cycle.

If capacitive current switching field tests are planned which exceed the number of operations as defined by the thermal capacity of the preinsertion resistors, or which utilise a specially designed circuit-breaker, the manufacturer should be consulted regarding the frequency of operations.

8.3.17 Application considerations for different circuit-breaker types

The switching of capacitive current poses different stresses on the different types of circuit-breakers. Restrikes on opening and prestrikes on closing may or may not be a problem. The considerations given below are general and are based on experiences gained by laboratory tests, field tests and field experience.

8.3.17.1 Oil circuit-breakers

8.3.17.1.1 Restrikes

Depending on the design (contact speed, electrode shape, etc.) an oil circuit-breaker generally has long arcing times when interrupting. The restrike probability increases with increased current, because gas bubbles reduce the effective amount of oil between the contacts causing a reduction of the dielectric strength of the contact gap. These circuit-breakers deserve special consideration when used or relocated to a system where the line charging current exceeds the rating.

Some oil circuit-breakers are pressurised to reduce the size of the bubbles and therewith increasing the dielectric strength of the contact gap. Some oil circuit-breakers may be fitted with breaking resistors, to reduce the effects of a restrike.

An oil circuit-breaker will normally not interrupt the high frequency current associated with the restrike and the high arc impedance introduces an additional damping of the restrike current. This will reduce the risk for multiple restrikes.

Older contraction type oil circuit-breakers are known to produce multiple restrikes with voltage escalation and evolving fault as a result.

8.3.17.1.2 Prestrikes

Oil circuit-breakers are especially sensitive to high-frequency prestrikes when energising capacitor banks. The prestrikes cause a shock wave in the oil. As oil is not compressible, the shock wave causes mechanical stresses on the internal components of the breaking chamber. As a result of the exposure to these high mechanical stresses, the breaking chamber insulator may shatter and even stationary contacts may crack. Application of an oil circuit-breaker for capacitor bank switching requires a severe reduction of the inrush current frequency or special design of the oil circuit-breaker (e.g. using preinsertion resistors).

Bulk oil circuit-breakers have been applied using a limitation of 20 kAkHz for over 30 years with no documented problems.

For minimum oil circuit-breakers a value of 1 kAkHz is suggested.

8.3.17.2 Vacuum circuit-breakers

8.3.17.2.1 Restrikes

The voltage withstand of the contact gap of a vacuum circuit-breaker rises very fast and the restrike probability is low. When a restrike occurs, the contact gap is small and the vacuum circuit-breaker is usually capable of interrupting the high-frequency restrike current, resulting in negligible voltage escalation.

8.3.17.2.2 NSDDs

NSDDs (see 8.2.1.1.2) are associated with vacuum circuit-breakers and are generally not a concern.

8.3.17.2.3 Prestrikes

The duration of the prestrike in a vacuum circuit-breaker is short. Shock waves are not a problem for this type of circuit-breaker.

The high-frequency discharge together with contact bouncing may lead to micro contact melting, especially when the arc is burning in the anode-spot mode (this occurs with currents higher than 10 kA). The breaking of welded points during a subsequent breaking operation with a very low current can damage the contact surface and this may reduce the dielectric withstand of the contact gap. However, a subsequent breaking operation with higher current may increase the dielectric withstand to its original condition. A subsequent no-load test may flatten the micro spot resulting in an increased dielectric strength.

8.3.17.3 SF_6 circuit-breakers

8.3.17.3.1 Restrikes

The interrupting capacity of SF_6 circuit-breakers is limited by the recovery voltage, which means that the frequency and earthing conditions (i.e. whether the circuit is effectively or non-effectively earthed) are important factors in the determination of the capability of the circuit-breaker.

Interruption of capacitive current is an easy switching case for a modern SF_6 circuit-breaker and higher currents than suggested in Table 5 of IEC 62271-100 do not pose a problem.

The capacity of clearing the high-frequency restrike current is low for puffer circuit-breakers and even lower for self-blast (or arc assisted) circuit-breakers. This also means that the risk for voltage escalation is low. However, a restrike may cause tracking and/or puncture of the insulating material between the contacts (e.g. nozzle, sleeve, etc.).

8.3.17.3.2 Prestrikes

The duration of the prestrike is depending on the voltage per breaking unit and the closing speed. In general this duration is short. SF_6 gas is a compressible medium and the shock wave does not cause any damage to the contacts and insulating material. In terms of capability to handle inrush currents, SF_6 circuit-breakers can handle 100 times more than oil circuit-breakers, i.e. $f_{\mathrm{i}} \times I_{\mathrm{i\ peak}}$ = 100 kAkHz.

8.3.17.4 Air-blast circuit-breakers

8.3.17.4.1 Restrikes

In general, the restrike probability of an air-blast circuit-breaker is higher than that of an SF_6 circuit-breaker. The flashover characteristic of air has a wider scatter than that of SF_6. Air-blast circuit-breakers can interrupt the high-frequency discharge current, which means that they have a higher probability of multiple restrikes, which may lead to voltage escalation. Restrikes may affect the air-blast circuit-breaker in the same way as the SF_6 circuit-breaker.

8.3.17.4.2 Prestrikes

The considerations given in 8.3.17.3.2 also applies to air-blast circuit-breakers.

8.4 Considerations of capacitive currents and recovery voltages under fault conditions

8.4.1 Voltage and current factors

Some requirements, general ratings and tests for capacitive current switching are based on switching operations in the absence of faults. The presence of a fault can increase the value of both the capacitive switching current and recovery voltage. This is recognised by IEC 62271-100 by the specification of two voltage factors when breaking in the presence of faults. These voltage factors are given in 8.2.1.4 and are 1,4 for effectively earthed systems and 1,7 for non-effectively earthed systems. Tests for these conditions are not mandatory. An example of such a fault is a circuit-breaker switching an overhead line that interrupts fault current in one phase and capacitive current in the other two phases.

The fact that the capacitive switching current increases in the presence of earth faults is recognised in subclause 6.111.9.3 of IEC 62271-100, where the line and cable charging currents are multiplied by 1,25 for effectively earthed neutral systems and 1,7 for non-effectively earthed systems. The number of tests is reduced to reflect the fact that such operations do not occur frequently.

For capacitor banks the situation is different. No tests are required for switching of solidly earthed neutral single (isolated) capacitor banks in solidly earthed neutral systems. Switching of non-effectively earthed neutral capacitor banks in solidly earthed neutral systems is not considered a normal system condition and no requirements or tests have been specified. Switching back-to-back is not considered a normal system condition and no requirements and tests have been specified.

8.4.2 Reasons for these specific tests being non-mandatory in the standard

In service, circuit-breakers have been successful in interrupting capacitive circuits under faulted conditions for a number of reasons. Principal reasons for successful operation include:

a) The probability of a fault occurring at minimum operating conditions of the circuit-breaker and its operating mechanism is extremely small.

b) The capacitance of the faulty phase is likely to be discharged before contact separation takes place.

c) The voltage factor used for single-phase tests is in excess of the service condition giving the tested circuit-breaker added margin.

d) Laboratory tests are performed using a minimal voltage jump, resulting in short arcing times. This condition is more severe than the actual network condition.

e) When switching a capacitor bank, with its neutral, or the system neutral, or both, non-effectively earthed, interruption of the first phase results in a single-phase circuit in the uninterrupted phases. Thus, since the two poles of the circuit-breaker are in series at final interruption, the voltage across each pole is less than rated.

8.4.3 Contribution of a capacitor bank to a fault

Consider the network situation given in Figure 42. A single line simplification is given in Figure 43. A fault has occurred on the line that is interrupted by the circuit-breaker. The capacitance of the capacitor bank will modify the TRV across the circuit-breaker to a 1-cos waveshape having a moderate rate-of-rise with an enlarged amplitude factor compared to the case without the presence of the capacitor bank.

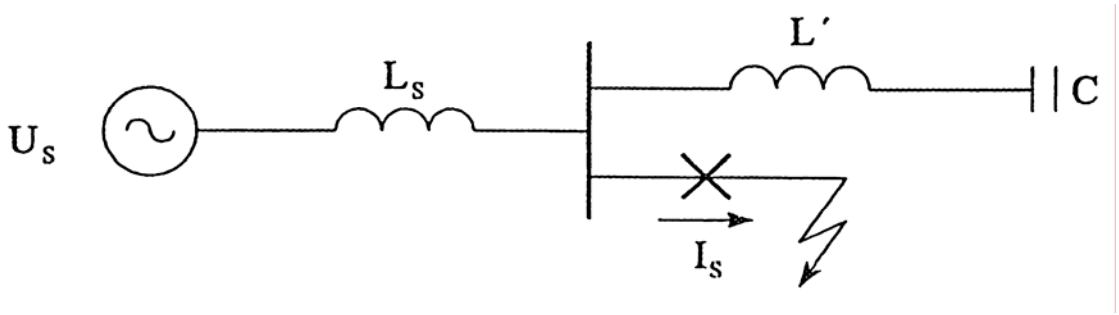


Figure 43 – Fault in the vicinity of a capacitor bank

When the ITRV is negligible, the circuit-breaker will attempt to interrupt at the first available current zero following contact separation, resulting in a relatively small contact gap. As the recovery voltage increases across the gap, a reignition might occur and the capacitor bank will discharge into the fault through the circuit-breaker. The amplitude of the discharge current depends on the voltage across the circuit-breaker contacts at the time of reignition and the frequency of the discharge current is determined by the inductance between the capacitor bank and the fault location.

If the ITRV is not negligible, which is usually the case, the circuit-breaker will interrupt with a longer arcing time (larger contact gap) and the case described above will not occur.

The high frequency discharge current is superimposed on the fault current, which creates additional current zeros. Depending on the type of circuit-breaker (oil, air-blast, vacuum or SF_6), the high frequency current may be interrupted causing high overvoltages. For further information there is referred to [4] and [5].

A similar situation may occur, when circuit breaker CB closes into a fault. The capacitor bank discharges into the fault and depending on the magnitude of the inductance between the capacitor bank and the fault location, the discharge current can reach peak values and frequencies that exceed those given in Table 5 of IEC 62271-100 (see also 8.3.13.2).

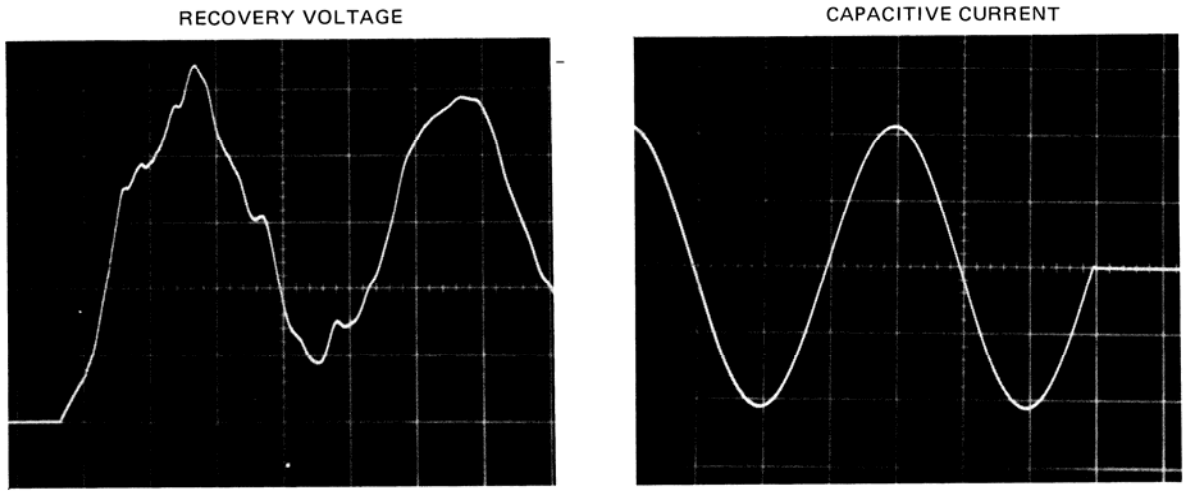
For these specific outrush cases the manufacturer should be consulted. For further treatment of this subject see IEEE 1036 – 1992 [6].

8.4.4 Switching overhead lines under faulted conditions

The voltages and currents which occur when switching a faulted transmission line are affected by the circuit parameters and the sequence in which the three phases interrupt. IEC 62271-100 lists the maximum value of recovery voltage for switching an unfaulted transmission line as $2 \times 1{,}2 \frac{U_r \sqrt{2}}{\sqrt{3}} = 2{,}4$ p.u. When switching a faulted line this value may be exceeded, as may be the rated capacitive switching current value as listed in Table 5 of IEC 62271-100 (see also [7]).

When switching a no-load overhead line with a phase-to earth fault, the highest voltage occurs on the unfaulted phase which interrupts prior to the faulted phase (see Figure 44a). The highest current occurs on the last phase to interrupt when the faulted phase is the first to

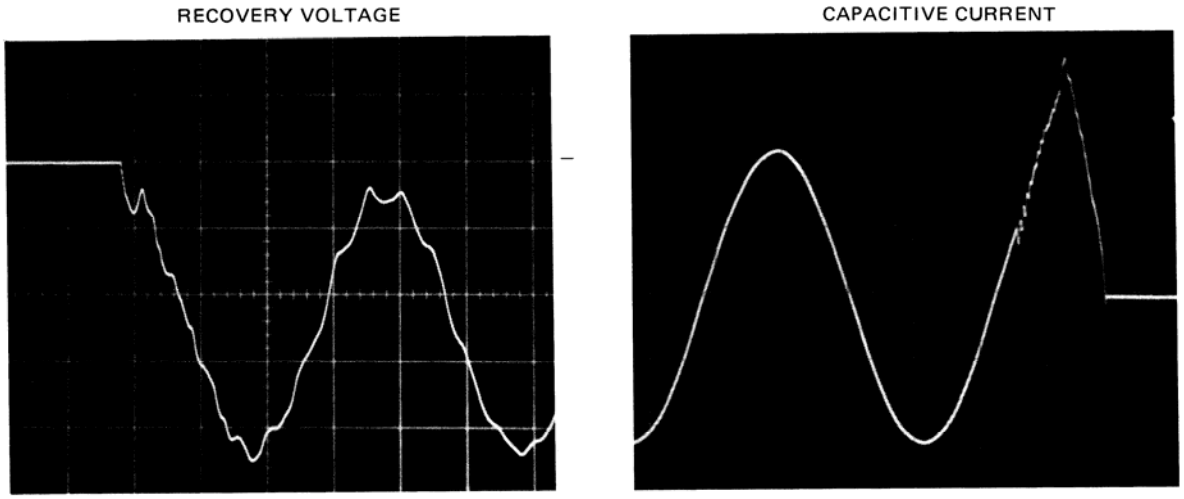
interrupt. The current for this case is not a sine wave but is distorted, as shown in Figure 44b. Under these conditions, the voltages and currents may exceed those on which the design tests are based.



Maximum recovery voltage 2,74 × U_{max} (phase-to-earth)

Maximum current 1,09 × rated current

Figure 44a – Recovery voltage and current for first-phase-to-clear when the faulted phase is the second phase-to-clear



Maximum recovery voltage 2,18 × U_{max} (phase-to-earth)

Maximum current 1,77 × rated current

Figure 44b – Recovery voltage and current for last-phase-to-clear when the faulted phase is the first-phase-to-clear

Figure 44 - Recovery voltages and currents for different interrupting sequences

For the phase-to-phase fault condition, the recovery voltage and capacitive current are less severe than for the two phase to earth fault condition, see also [6].

8.4.5 Switching capacitor banks under faulted conditions

The voltages and currents which can occur when switching a faulted capacitor bank depend upon the earthing conditions, whether the fault is to the bank neutral or to earth, and on the sequence in which the three phases interrupt. IEC 62271-100 lists the maximum value of recovery voltage in switching an unfaulted shunt capacitor bank as 2,8 p.u. When switching a faulted bank, this value may be exceeded, as may the rated capacitive switching current value. In the sections below a comparison is given between the recovery voltages and currents of a reference condition and two faulted conditions: a fault to neutral in the capacitor bank and a fault to earth in one phase.

NOTE The factor 2,8 for the maximum recovery voltage specified in IEC 62271-100 is valid when switching a non-effectively earthed capacitor bank where the second and third phases clear 90 degrees after the first. This is true for modern circuit-breakers. For older circuit-breakers, where the second and third phases do not clear 90 degrees after the first, this factor is 3,0.

8.4.5.1 Reference condition

The reference condition is illustrated in Figure 45. The neutral of the source and the capacitor bank may be solidly earthed and/or non-effectively earthed. The size of the capacitor bank is such that the current is equal to the rated single (isolated) capacitor bank current.

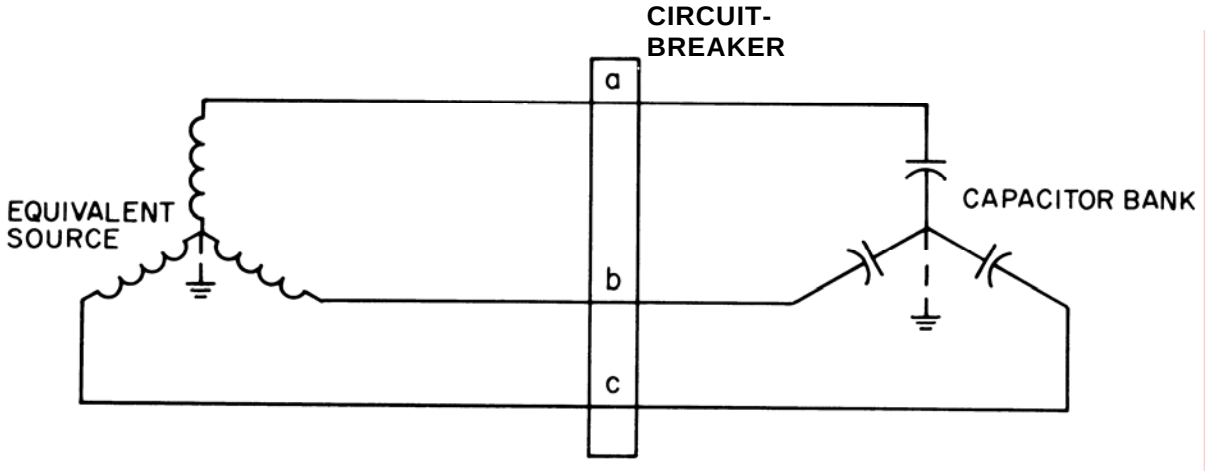


Figure 45 – Reference condition

8.4.5.1.1 Recovery voltage

The highest recovery voltage (2,8 p.u.) is obtained in the first pole-to-clear when either the neutral of the capacitor bank, the neutral of the source or both are non-effectively earthed and poles 2 and 3 clear 90 degrees after the first.

The voltages and currents obtained with this reference condition (unfaulted balanced system) agree with the 2,8 p.u. voltage listed in IEC 62271-100. Although the voltage across the last poles to interrupt when at least one of the neutrals (source or bank) is non-effectively earthed can reach $2 \times U_r \sqrt{2}$ (3,46 p.u.), the two phases are in series so that neither is stressed to more than 1,4 p.u.

8.4.5.1.2 Capacitor bank current

In all cases the capacitor bank current does not exceed the rated single (isolated) capacitor bank current.

8.4.5.2 Fault to neutral in one phase (one capacitor bank phase short-circuited)

8.4.5.2.1 Recovery voltage

The highest recovery voltage ($2 \times U_r \sqrt{2} = 3{,}46\,\text{p.u.}$) is obtained when at least one neutral is non-effectively earthed and the first pole-to-clear clears a healthy phase. This is in agreement with the voltage factor of 1,7 specified in IEC 62271-100. If the first pole-to-clear interrupts an unfaulted phase, it is subjected to a recovery voltage of 3,46 p.u. until the second and third phases interrupt.

The highest recovery voltage in the remaining phases is 3,46 p.u., but it is shared by two interrupters in series.

8.4.5.2.2 Current

The highest capacitive current is obtained in the cases described under 8.4.5.2.1 when the faulted phase is the first pole-to-clear and is equal to 3 times that of the reference case.

8.4.5.3 Fault to earth in one phase

Most systems are effectively earthed and the highest recovery voltage is obtained when the first-pole-to-clear interrupts a non-faulted phase. In this case the maximum recovery voltage peak will be 2,8 p.u.

The most severe case is when the source is non-effectively earthed and the bank neutral is solidly earthed. If an unfaulted pole is the first to interrupt, the current may reach √3 times that of the reference condition and the recovery voltage 3,46 p.u. The remaining poles are subjected to the same current, but upon interrupting, share the 3,46 p.u. recovery voltage. When the faulted pole is the first pole-to-clear, the current may be 3 times the rated current value and the recovery voltage $2 \times 1{,}25 \times \frac{U_r \sqrt{2}}{\sqrt{3}}$. The second pole to interrupt will have a lower current but a higher recovery voltage of $2 \times U_r \sqrt{2} = 3{,}46\,\text{p.u.}$ which will be shared with the third pole. If the faulted pole reignites, one of the unfaulted poles will then interrupt and the conditions will be as previously described when an unfaulted pole was the first to interrupt.

8.4.5.4 Other fault cases

For phase-to-phase earth faults, or phase-to-phase non-effectively earthed faults, with the source solidly earthed and the bank neutral non-effectively earthed, recovery voltages and currents are no more severe than for the standard no-fault condition.

8.4.6 Switching cables under faulted conditions

The normal frequency capacitive currents and recovery voltages on a faulted cable circuit will be the same as for a solidly earthed capacitor bank under faulted conditions.

8.4.7 Examples of application alternatives

Other application options available are:

a) Use a circuit-breaker of a higher rating in those cases of earth faults on non-effectively earthed systems where the recovery voltage and current, or both, exceed the requirements of IEC 62271-100.

b) Reduce the capacitance of the existing capacitor bank size so that the current under faulted conditions does not exceed the rated capacitive switching current of the circuit-breaker.

c) Use a high- speed switch to earth the source or capacitor bank neutral before switching the capacitor bank under faulted conditions.

d) Use a Δ configuration for the capacitor bank instead of a non-effectively earthed Y.

8.5 Explanatory notes regarding capacitive current switching tests

Subclause 6.111 of IEC 62271-100 deals with capacitive current switching tests. In the 1st edition of this standard a new test procedure has been introduced for the two classes of capacitive current switching that deserve some explanation.

8.5.1 Restrike performance

See 8.3.5.

8.5.2 Test programme

In defining the test programme for these two classes, the following elements have been taken into account:

- the average number of operations per year carried out by circuit-breakers switching capacitive loads;
- the ability to reduce the number of tests by performing an increased number of switching operations at the minimum arcing time, usually the most difficult capacitive switching operation for circuit-breakers, thus keeping a high level of reliability;
- the recommendations of CIGRE working group A3.04. The expected restrike probability is exclusively related to the type tests

The proposed number of tests may be questioned because of different assumptions for probability calculations. Nevertheless, these values represent a good compromise (which is the role of the standard where conflicting views exist), reflecting the needs of users (in response to market demand) and above all they avoid unrealistic demands. These tests are not reliability tests but type tests to demonstrate a satisfactory capacitive current switching capability of the equipment in service.

8.5.3 Subclause 6.111.3 – Characteristics of supply circuit

The paragraph concerning factor k_c / k_{pp} (from earlier versions of the standard) where k_c is the voltage factor as described in 8.2.1.4 and k_{pp} is the first-pole-to-clear factor has been deleted because there is neither use nor need for testing.

The variation of the power frequency voltage has been chosen as 5 % for test-duty 2 (LC2, CC2 and BC2) and 2 % for test-duty 1 (LC1, CC1 and BC1). These values are a compromise, taking limitations of testing laboratories into account. Considering the type test as a whole, because of the different stresses in the individual test-duties, any undue reduction of the electric stress during the tests is avoided. The actual values for the power frequency voltage variation (depending on the short-circuit power of the system and the capacitive load) is in the range of 1 % to 2 %.

8.5.4 Subclause 6.111.5 – Characteristics of the capacitive circuit to be switched

The interval after final arc extinction, in which the voltage decay shall not exceed 10 %, has been changed from 100 ms to 300 ms based on service conditions.

8.5.5 Subclause 6.111.9.1.1 – Class C2 test duties

Performing these capacitive current switching tests for class C2 equipment on a preconditioned circuit-breaker is, on the one hand, a recommendation of CIGRE working group A3.04; on the other hand, it draws closer to the real conditions of service, without prejudice as to whether this preconditioning improves the capacitive current switching performance of the circuit-breaker or not.

Close-open operations may be performed with no-load closing operations. In any case, the complete sequence shall be tested in order to test the circuit-breaker during opening in a dynamic condition, i.e. during the motion of the fluid caused by the previous closing operation.

8.5.6 Subclauses 6.111.9.1.1 and 6.111.9.2.1 – Class C1 and C2 test duties

The tolerance of the testing current values for test-duty 1 (LC1, CC1 and BC1) were increased from the old range 20 % to 40 % to the new range 10 % to 40 % in order to give more freedom during testing for combined test-duties for different applications.

The proposed test sequences have been tested in a laboratory (particularly the adjustment of the minimum arcing time by steps of 6°) and are well adapted to the philosophy of the tests.

Performing some tests at rated pressure is a more pragmatic approach to the notion of type testing, knowing that the circuit-breaker does not always stand under the worst functioning conditions.

8.5.7 Subclauses 6.111.9.1.2 and 6.111.9.1.3 – Single-phase and three-phase line- and cable-charging current tests

In test-duty 2 of single-phase line-charging and cable-charging tests (LC2 and CC2), the tests are split into open operations and close-open operations (6.111.9.1.3) to follow more or less the actual service conditions. However, for practical reasons, due to the small number of tests, in three-phase tests (6.111.9.1.2) in test-duty 2 (LC2 and CC2), close-open operations are performed exclusively.

8.5.8 Subclauses 6.111.9.1.2. to 6.111.9.1.5 – Three-phase and single-phase line, cable and capacitor bank switching tests

Close-open operations are important for capacitor bank switching because of the effect of inrush current. Close-open operations are not significant for line- or cable-switching applications, therefore for line- and cable-switching tests, only a small number of close-open operations are requested (closing may be performed as a no-load operation).

A rough parity of the number of three-phase and single-phase tests has been maintained.

The mandatory nature for capacitor bank switching tests is due to the necessity to introduce the effect of inrush current at the beginning of the tests.

8.5.9 Subclauses 6.111.9.1.4 and 6.111.9.1.5 – Three-phase and single-phase capacitor bank switching tests

Because of the large number of operations in actual service compared with the limited number of operations during type testing, a high number (80 or 120 respectively) of close-open operations shall be carried out in capacitor bank tests to simulate the wear in service even if the close-open operation is not the normal switching sequence.

For capacitor bank switching tests test-duty 1 (BC1) also needs to be performed, even if the actual service switching duty is always at 100 % nominal current, for the following reasons:

- the tests at 10 - 40 % nominal current cover an increased number of actual currents;
- knowledge of the capacitive current switching performance is improved.

8.6 References

[1] GABRIELLE, A. F., MARCHENKO, P. P., and VASSELL, G. S. Electrical Constants and Relative Capabilities of Bundled Conductor Transmission Lines. *IEEE Transactions on Power Apparatus and Systems,* vol 83, Jan 1964, pp 78-92

[2] CIGRE Technical Brochure 47: Line-Charging Current Switching of HV Lines – Stresses and Testing Part 1 and 2, Oct 1996

[3] IEEE C62.22-1997: IEEE Guide for the Application of Metal-Oxide Surge Arresters for AC Systems

[4] van der SLUIS, L., and JANSSEN, A.L.J., Clearing faults near shunt capacitor banks, IEEE transactions on power delivery, Vol. 5, No. 3, July 1990, pp. 1346-1354

[5] CIGRE Technical Brochure 134: Transient recovery voltages in medium voltage networks

[6] IEEE 1036-1992: IEEE Guide for Application of Shunt Capacitors

[7] R. Eriksson and V.S. Rashkes: Three-phase interruption of single and two-phase faults: Breaking stresses in the healthy phase. Electra No. 67 (1980), pp. 77-92

8.7 Bibliography

McCauley (T.M.), Pelfrey (D.L.), Roettger (W.C.), Wood (C.E.). The impact of Shunt Capacitor Installations on Power Circuit Breaker Applications. IEEE Transactions on Power Apparatus and Systems, Vol. PAS-99, N°6 (1980-11)

O'Leary (R.P.), Harner (R.H.). Evaluation of Methods for Controlling the Overvoltages Produced by Energization of a Shunt Capacitor Bank. CIGRE Session 1988, Report 13-05 (1988).

Heldman (D.E.), Johnson (I.B.), Titus (C.H.), Wilson (D.D.). Switching of Extra-High-Voltage Circuits, Surge reduction with circuit-breaker resistors. IEEE Transactions on Power Apparatus and Systems, Vol.83 (1964-12)

Konkel (H.E.), Legate (A.C.), Ramberg (H.C.), Limiting switching surge overvoltages with conventional power circuit breakers. IEEE Transactions on Power Apparatus and Systems, Vol.96 (1977-03)

CIGRE WG 13-02, Switching overvoltages in EHV and UHV systems with special reference to closing and reclosing transmission lines. Electra N°30 (1973-10)

Electrical Transmission and Distribution Book. East Pittsburgh, Pa.: Westinghouse Electric Corporation, 1950

IEEE Committee Report Bibliography on Switching of Capacitive Circuits Exclusive of Series Capacitors, *IEEE Transactions on Power Apparatus and Systems,* vol PAS 89, Jun/Jul 1970, pp 1203-1207

JOHNSON, I.B.; SCHULTZ, A.J.; SCHULTZ, N.R.; and SHORES, R.B., *AIEE Transaction*, pt III, 1955 pp 727-736

H.M. Pflanz and G.N. Lester: Control of Overvoltages on Energizing Capacitor Banks. IEEE Transactions on Power Apparatus and Systems, vol. PAS-92, pp. 907 - 915, No. 3, May/June 1973

9 Inductive load switching

The IEC 62271-100 subclause relevant to this chapter is:

4.108 Inductive current switching

9.1 Introduction

Inductive current switching covers the following cases:

- shunt reactor switching;
- motor switching;
- unloaded transformer switching.

Circuit-breakers in general have no difficulty interrupting small inductive currents, the current in fact is usually forced to a premature zero by a phenomenon known as current chopping. However, the resultant chopping overvoltages and those due to subsequent reignition (in the circuit-breaker), the magnitude of which are dependent on both the characteristics of the circuit-breaker and the circuit, can be of such significance as to require some form of limitation. The duty is thus very interactive and due diligence should be exercised in selecting a circuit-breaker for this purpose.

The general theory of inductive current switching is essentially common to all of the above-noted switching cases. On this basis, shunt reactor switching is considered in detail and unloaded transformer and motor switching as extensions to that case.

9.2 Shunt reactor switching

9.2.1 General

The three shunt reactor switching cases to be considered are:

- solidly earthed shunt reactors usually applied at HV (72,5 kV $\leq U_r \leq$ 245 kV, where U_r is the rated voltage) and EHV (300 kV $\leq U_r \leq$ 800 kV);
- neutral reactor earthed shunt reactors usually applied at EHV;
- unearthed shunt reactors usually applied at $U_r \leq$ 52 kV.

All three cases can be readily analyzed by first considering the general case of the neutral reactor earthed shunt reactor and extending it to the other two cases.

Typical shunt reactor characteristics are provided in Appendix A and related system and station characteristics in Appendix B.

9.2.2 Chopping Overvoltages

The general case is shown in Figure 46 where the shunt reactor is represented by its inductance L and capacitance C_L and the neutral reactor correspondingly by L_N and C_N. C_L includes the inherent capacitance of the shunt reactor and the capacitance of all components between the circuit-breaker and the shunt reactor. C_N is the inherent capacitance of the neutral reactor but does not influence first-pole-to-clear considerations and can be ignored.

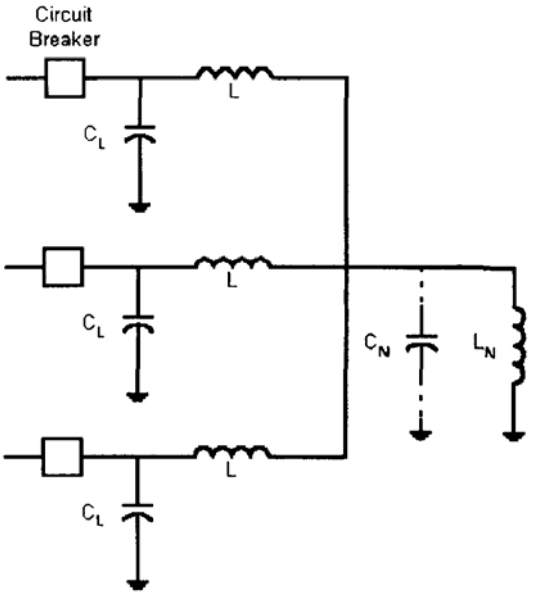
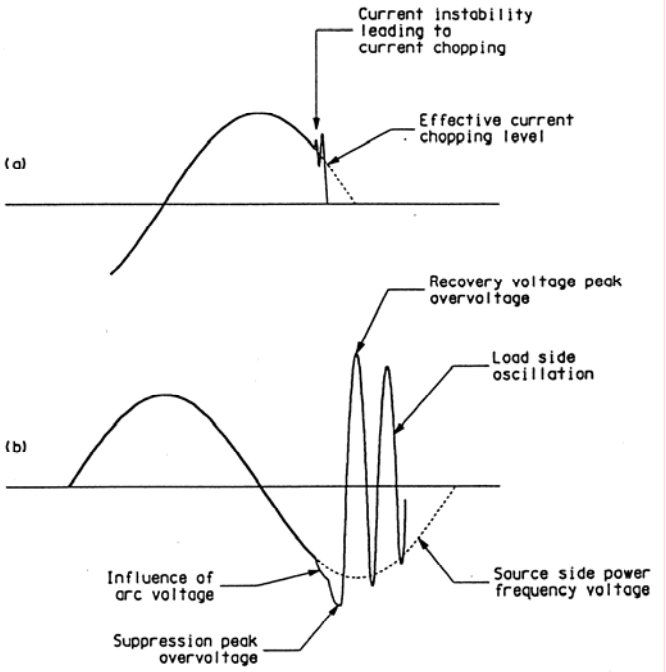


Figure 46 – General case for shunt reactor switching

After contact parting as the current goes towards zero, an unstable interaction occurs between the arc and the capacitance in parallel with the circuit-breaker (refer to Appendix C). This interaction results in a negatively damped oscillation in the current which eventually crosses the zero line thus chopping the current prior to the power frequency zero crossing as shown in Figure 47. The chopping of the current leaves stored energy in the shunt reactor resulting in an overvoltage referred to as the suppression peak overvoltage. The task now is to calculate the magnitude of this overvoltage and apply it to the first-pole-to-clear case for the circuit-breaker. The highest suppression peak overvoltage may actually occur on the second or third pole to clear due to higher current chopping at the associated longer arcing times.



(a) Current through circuit-breaker

(b) Voltage across shunt reactor

Figure 47 – Current chopping phenomena

The first-pole-to-clear representation for the general case (Figure 46) is shown in Figure 48. i_c is the chopped current in the first-pole-to-clear and the second and third poles are considered to be earthed through an infinite bus.

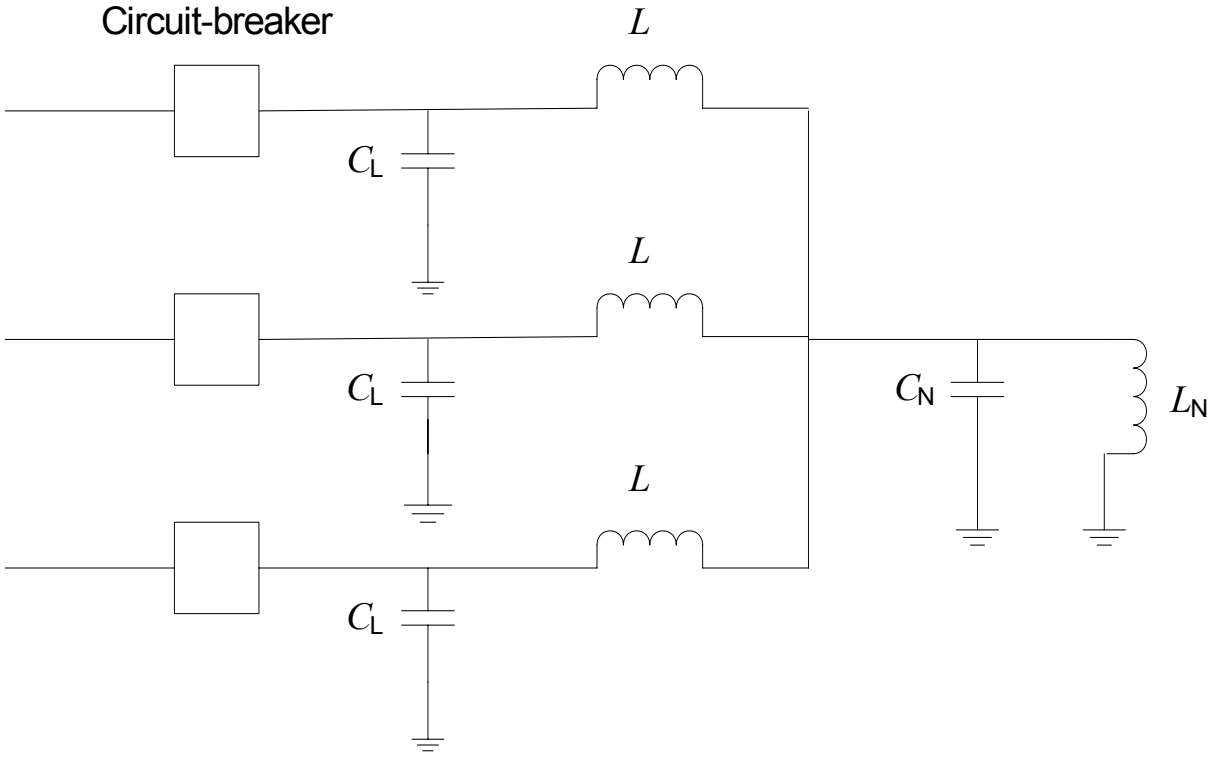


Figure 48 – General case first-pole-to-clear representation

The single-phase equivalent circuit for the first-pole-to-clear is derived from Figure 48 and shown in Figure 49.

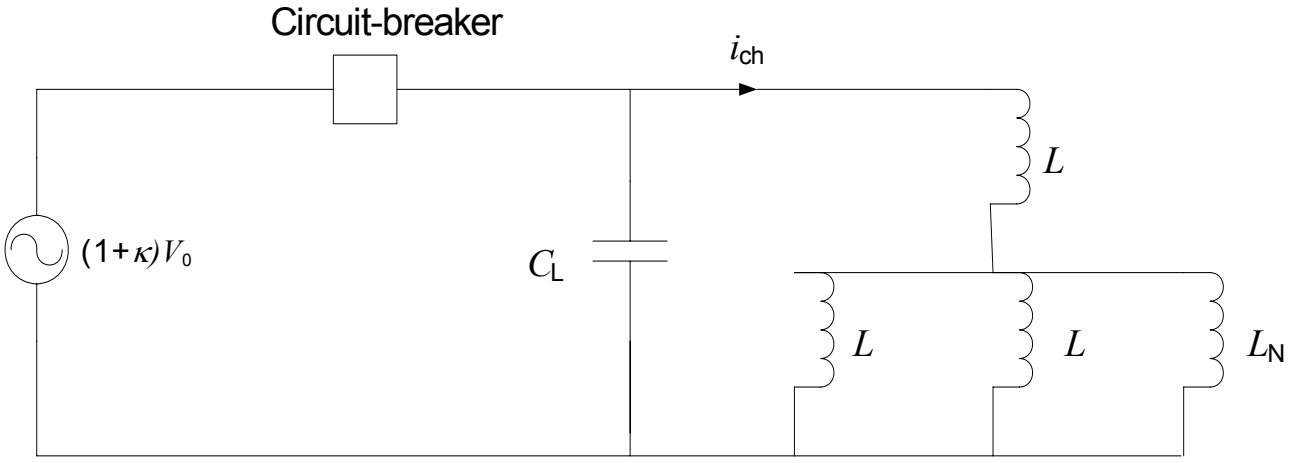


Figure 49 – Single phase equivalent circuit for the first-pole-to-clear

In Figure 49, V_0 is the peak power frequency voltage across the shunt reactor at the instant of current chopping and $(1+\kappa)$ is the first pole factor given by:

$$L' = L\left[1 + \frac{1}{2 + L/L_N}\right] = L[1 + \kappa] \qquad (61)$$

For solidly earthed shunt reactors, L_N = 0, κ = 0 and L' = L; for non-effectively earthed shunt reactors L_N = ∞; κ = 0,5 and L' = 1,5 L.

The energy trapped in L' and C_L at the instant of current chopping will oscillate between the two circuit elements. The suppression peak overvoltage can be calculated by considering the energy balance since the maximum overvoltage will occur when the available energy is stored capacitively in C_L:

Energy at suppression peak overvoltage = Energy at current interruption

or

$$\frac{1}{2} C_L V_m^2 = \frac{1}{2} C_L [(1 + \kappa) V_0)]^2 + \frac{1}{2} i_{ch}^2 L' \qquad (62)$$

where V_m is the peak voltage on the capacitor C_L when all the available energy is capacitively stored.

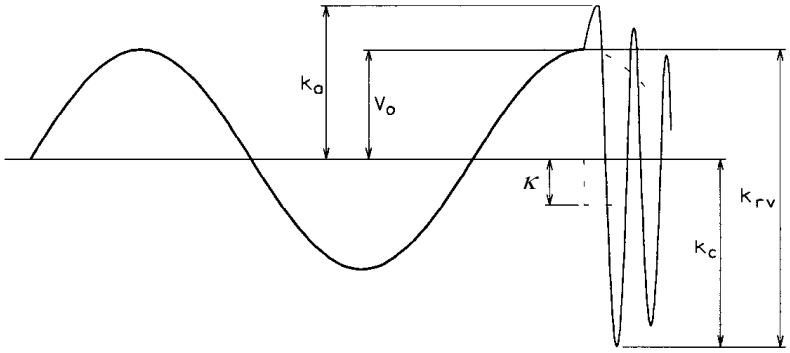


Figure 50 – Shunt reactor voltage at current interruption

The instant of current chopping is usually taken as occurring at the peak of the voltage across the shunt reactor (V_o) and neglecting arc voltage Equation (62) can be rewritten as:

$$\frac{V_m}{V_0} = (1 + \kappa)\sqrt{1 + \frac{1}{(1 + \kappa)}\left(\frac{i_{ch}}{V_0}\right)^2 \left(\frac{L}{C_L}\right)} = k_a + \kappa \qquad (63)$$

with (k_a + κ) in p.u. The factor (k_a + κ) is usually designated k_b. From Equation (63) the suppression peak overvoltage k_a (refer to Figure 50) can be calculated as follows:

$$k_a = (1 + \kappa)\sqrt{1 + \frac{1}{(1 + \kappa)}\left(\frac{i_{ch}}{V_o}\right)^2 \left(\frac{L}{C_L}\right)} - \kappa \qquad (64)$$

The value of the chopped current is dependent on the capacitance C_t seen from the circuit-breaker terminals including the grading capacitor capacitance C_p, the number N of interrupters in series per pole and the so-called chopping number λ for a single interrupter, which is a characteristic value of the circuit-breaker. The chopping current level is given by:

$$i_{ch} = \lambda\sqrt{NC_t} \tag{65}$$

where $$C_t = C_p + \frac{C_s C_L}{C_s + C_L}$$

The chopping number approach can be applied for all current circuit-breaker types except vacuum circuit-breakers, where the basic Equation (64) must be used. The approach is valid provided that the circuit as seen by the circuit-breaker can be considered as an equivalent parallel capacitance in the relevant range of frequencies. Where this is not the case a computational approach using EMTP or other method is required [3].

Typical chopping numbers are given in Table 9. For gas circuit-breakers in particular, current chopping increases with arcing time and likewise the chopping number.

Table 9 – Circuit-breaker chopping numbers

Circuit-breaker type	Chopping number λ $AF^{-0,5}$
Minimum oil	$5{,}8 \times 10^4$ to 10×10^4
Air blast	15×10^4 to 20×10^4
SF_6 puffer	4×10^4 to 19×10^4
SF_6 self-blast	3×10^4 to 10×10^4
SF_6 rotating arc	$0{,}39 \times 10^4$ to $0{,}77 \times 10^4$

The maximum value of C_t leading to the highest chopping level and subsequent highest suppression peak overvoltage occurs when $C_s >> C_L$ and C_t is given by:

$$C_t = C_P + C_L \tag{66}$$

Substituting for i_{ch} (from Equations (65) and (66)) in Equation (64) gives k_a on a chopping number basis:

$$k_a = (1+\kappa)\sqrt{1 + \frac{NL}{(1+\kappa)}\left(\frac{\lambda}{V_o}\right)^2\left(\frac{C_P}{C_L}+1\right)} - \kappa \tag{67}$$

A more useful variation of Equation (67) based on the shunt reactor rating Q in VA and taking V_o as the peak value of the system voltage to earth is:

$$k_a = (1+\kappa)\sqrt{1 + \left(\frac{1{,}5}{1+\kappa}\right)\left(\frac{N\lambda^2}{\omega Q}\right)\left(\frac{C_P}{C_L}+1\right)} - \kappa \tag{68}$$

For solidly earthed shunt reactors, $\kappa = 0$ and k_a is given by:

$$k_a = \sqrt{1 + \frac{1{,}5N\lambda^2}{\omega Q}\left(\frac{C_P}{C_L}+1\right)} \tag{69}$$

For non-effectively earthed shunt reactors, $\kappa = 0{,}5$, $N = 1$, C_P is negligible compared to C_L and k_a is given by:

$$k_a = 1{,}5\sqrt{1+\frac{\lambda^2}{\omega Q}} - 0{,}5 \qquad (70)$$

k_a and the subsequent recovery voltage peak overvoltage k_c stress the shunt reactor, the latter being given by (refer to Figure 50):

$$k_c = 2\kappa + k_a \qquad (71)$$

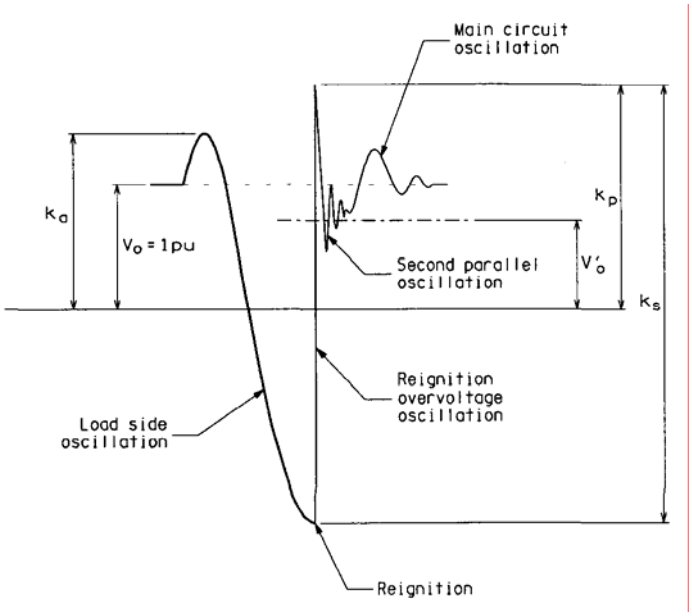
The transient recovery voltage peak imposed on the circuit-breaker is k_{rv} (refer to Figure 50) given by:

$$k_{rv} = 1 + 2\kappa + k_a \qquad (72)$$

The influence of the earthing arrangement is reflected in the 2κ factor, the multiplier of 2 being due to the fact that the oscillation is about the shifted neutral point.

9.2.3 Reignition Overvoltages

When a reignition occurs in the circuit-breaker the load side voltage rapidly tends to the source side voltage but overshoots producing a reignition overvoltage as shown in Figure 51.



V_0 Power frequency crest voltage to earth at instant of current interruption

k_a Suppression peak overvoltage in p.u. of V_0

k_p Reignition overvoltage peak to earth in p.u. of V_0

k_s Reignition overvoltage excursion in p.u. of V_0

$$\frac{V'_0}{V_0} = \frac{C_s}{C_s + C_L}\left(1 - k_a \frac{C_L}{C_s}\right)$$

Figure 51 – Reignition at recovery voltage peak for a circuit with low supply side capacitance

Figure 51 shows the case for a circuit with a low source side capacitance and the only difference for a high source side capacitance is that $V'_o = V_o$ and the initial second parallel oscillation is around the source voltage (circuit oscillations are discussed in 9.2.4).

The reignition overvoltage in the worst case (C_s very large) oscillates around the source voltage and its magnitude k_i in p.u. to earth assuming damping (β) is given by:

$$k_p = 1 + \beta(1 + 2\kappa + k_a) \quad (73)$$

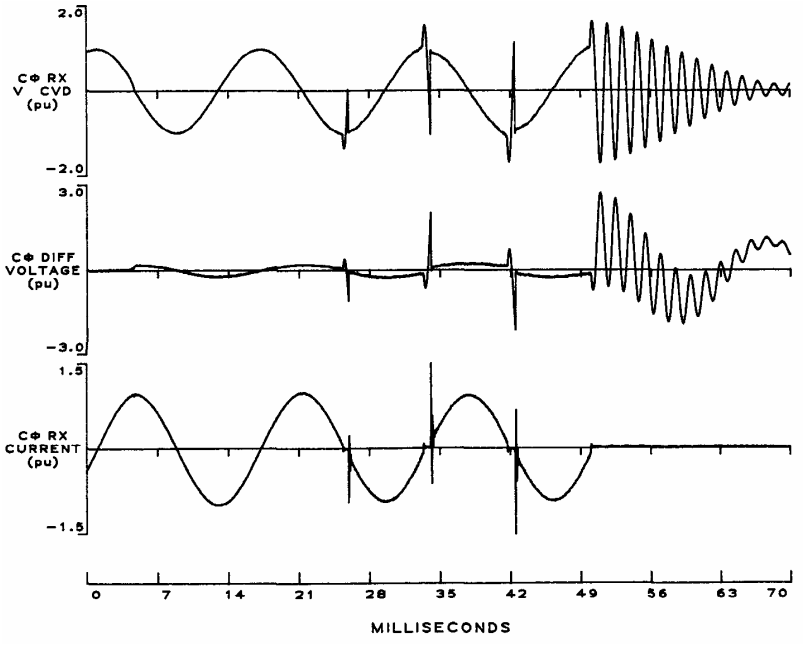
The damping factor β is usually taken as 0,5 based on actual field experience.

The excursion of the reignition transient k_s in p.u. is given by:

$$k_s = (1 + \beta)(1 + 2\kappa + k_a) \quad (74)$$

Reignitions are normal occurrences but may be harmful to the interrupters [4] and also to the shunt reactor windings.

Figure 52 shows an actual 500 kV shunt reactor switching event illustrating chopping and reignition overvoltages. The circuit-breaker in this case exhibits an extraordinary number of reignitions as compared to the typical case of reignition at one zero crossing only.



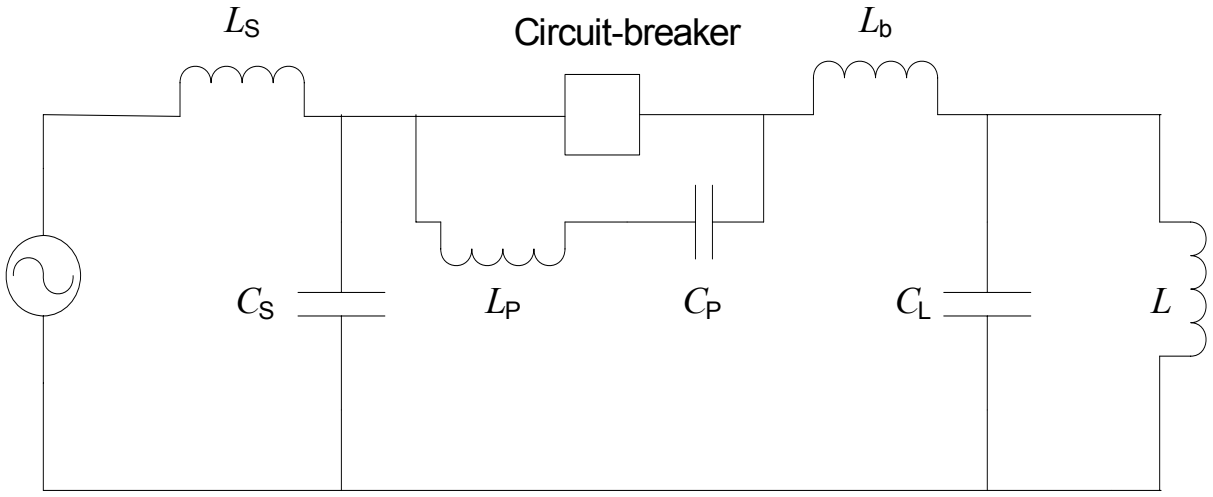
Upper trace	Voltage to earth at shunt reactor
Middle trace	Voltage across circuit-breaker
Lower trace	Shunt reactor current

Figure 52 – Field oscillogram of switching out a 500 kV 135 MVAR solidly earthed shunt reactor

A summary of the principal overvoltage equations derived in 9.2.2 and 9.2.3 above is provided in Appendix D. At $U_r \leq 52$ kV the arc voltage for SF_6 circuit-breakers may be significant relative to the supply voltage and the overvoltage equations without and with arc voltage are provided in Appendix E.

9.2.4 Oscillation Circuits

Four oscillation circuits play a role in shunt reactor switching and can be generally described by considering the solidly earthed shunt reactor case (refer to Figure 52). The first oscillation circuit relates to current interruption and the other three circuits to the reignition process.



Key

L_s	source inductance	L_b	connection series inductance
C_s	source side capacitance	C_L	load side capacitance
L_p, C_p	first parallel circuit inductance and capacitance	L	reactor inductance

Figure 53 – Single-phase equivalent circuit

9.2.4.1 Load Side Oscillation

A successful shunt reactor current interruption results in a decaying load side oscillation with the trapped energy oscillating between the inductance L and the capacitance C_L (Figure 53). The frequency of this oscillation is:

$$f_L = \frac{1}{2\pi\sqrt{LC_L}} \qquad (75)$$

and is typically in the range 1 to 5 kHz for EHV and HV shunt reactors and up to 30 kHz for MV shunt reactors. f_L is the frequency of the circuit-breaker transient recovery voltage whose peak value is given by Equation (72).

9.2.4.2 First Parallel Oscillation

When a reignition occurs in the circuit-breaker, a first parallel oscillation occurs due to the discharge of capacitance C_P through the circuit-breaker (Figure 51 and Figure 53). The frequency of this oscillation is given by:

$$f_{p1} = \frac{1}{2\pi\sqrt{L_P C_P}} \qquad (76)$$

and is typically in the range 1 to 10 MHz. The circuit-breaker will not interrupt the current associated with this oscillation and therefore it has no significance with respect to overvoltages.

9.2.4.3 Second Parallel Oscillation

The second parallel oscillation follows the first parallel oscillation involving C_s, C_L and L_b and results in equalization of the voltages on C_s and C_L (Figure 51 and Figure 53). The frequency of this oscillation is given by:

$$f_{p2} = \frac{1}{2\pi\sqrt{L_b\left(\frac{C_s C_L}{C_s + C_L}\right)}} \tag{77}$$

and is typically in the range of 50 kHz to 1 MHz. This transient voltage is steep and may be unevenly distributed across the shunt reactor winding, stressing in particular the entrance turns of the winding. The reignition itself is particularly hazardous to the entrance turns.

9.2.4.4 Main Circuit Oscillation

Under certain circumstances (C_s and C_L of the same order of magnitude), a main circuit oscillation follows the second parallel oscillation (Figure 51 and Figure 53). This oscillation is complex and its frequency in its simplest form is given by:

$$f_m = \frac{1}{2\pi}\sqrt{\frac{L_s + L}{L_s L(C_s + C_L)}} \tag{78}$$

and is in the range 5 to 20 kHz.

9.2.5 Overvoltage limitation

Some method of overvoltage limitation is usually applied in all shunt reactor switching cases. The various methods and their relative effectiveness are reviewed in Table 10.

Table 10 – Chopping and reignition overvoltage limitation method evaluation for shunt reactor switching

Overvoltage limitation method	How does the method work?	Advantage	Disadvantage
Opening resistor	Resistor causes phase shift of current with respect to voltage resulting in current interruption by resistor switch at lower point on voltage halfwave thus reducing k_a and consequently k_{rv} significantly.	Very effective on circuit-breakers with very high chopping numbers, i.e. air-blast and dual pressure SF_6 circuit-breakers.	Adds significantly to mechanical complexity and maintenance requirements of the circuit-breaker; not viable – technically or economically – on single pressure SF_6 circuit-breakers; reignitions can still occur.
Surge arresters to earth at shunt reactor	Limits overvoltage to earth (k_a) at shunt reactor.	Passive.	Effective only for circuit-breakers producing suppression peak overvoltages in excess of the surge arrester protective level; reignition overvoltages still occur at up to twice the protective level of the surge arrester with no reduction in the reignition overvoltage excursion frequency.
Metal oxide varistor (MOV) across circuit-breaker [5]	Limits the recovery voltage (k_{rv}) across the circuit-breaker to the protective level of the varistor and subsequent reignition overvoltages to maximum $1+\beta k_{arv}$ where k_{arv} is the protective level of the arrester in p.u. of V_o.	Passive; effective for all circuit-breaker types; particularly suitable for use on circuit-breakers at ≤ 52 kV; magnitude and probability of reignitions significantly reduced; energy absorbed by surge arrester is minimal.	Adds to complexity of circuit-breaker; surge arresters must be able to withstand forces associated with circuit-breaker operation; some reignitions will still occur albeit at low voltage levels.
Surge capacitor	Decreases frequency and thereby rate of rise of the load side oscillation; decreases frequency of reignition overvoltage excursion.	May reduce probability of reignitions; reduces frequency of the voltage excursion imposed on the shunt reactor winding; may reduce value of k_a for vacuum breakers where chopping current is dependent mainly on contact material.	Does not influence k_a for circuit-breakers other than vacuum type; leads to increased chopping current but not necessarily increased suppression peak overvoltages; does not eliminate reignitions; may have the effect of reducing the minimum arcing time such that probability of reignitions is unchanged; require space.
Controlled switching	Ensures contact parting with respect to current wave such that interruption occurs at the first subsequent current zero.	Eliminates reignitions.	Suitable only for mechanically consistent circuit-breakers with appropriate minimum arcing times; requires independent pole operation thereby increasing capital cost of the circuit-breaker (but this is mitigated by the low life cycle cost due to significantly reduced maintenance requirements).

9.2.6 Circuit-breaker specification and selection

9.2.6.1 General

Shunt reactor switching is a very unique switching duty and requires diligent specification and selection of the circuit-breaker. The intent should be to specify the circuit-breakers in terms

under the control of the manufacturer and to select the circuit-breaker to perform the duty while minimizing the overvoltage impact on the application which is under the control of the user.

9.2.6.2 Circuit-breaker Specification

On the basis that the dedicated purpose of the circuit-breaker is to switch a shunt reactor only, the following characteristics should be specified. If short circuit current interruption capability is required than this duty must also be specified.

- Dielectric withstand requirements.
- Rated short-time and peak withstand currents (assumes no fault clearing).
- Shunt reactor rating.
- Shunt reactor current.
- Load side characteristics: Inductance L of the shunt reactor and C_{L} the total effective capacitance of the load side circuit including the shunt reactor and all connected equipment.
- Overvoltage limitation: The suppression peak overvoltage (k_{a}) limitation should be stated; a k_{a} value of 2 p.u. is recommended for EHV and HV applications at or above 72,5 kV and 2,5 p.u. for applications at $\leq$ 52 kV. Note that no limitation for reignition overvoltages should be stated since these overvoltages are very circuit dependent.
- Earthing arrangement whether solidly earthed, non-effectively earthed or neutral reactor earthed. In the latter case, the inductance of the neutral reactor should be stated.
- Mechanical endurance: Shunt reactor circuit-breakers are usually subject to frequent operation and class M2 should be specified.

9.2.6.3 Circuit-breaker selection

Overvoltages can be limited by proper selection of the circuit-breaker. For HV circuit-breakers, by reference to Equation (69), a degree of control of overvoltage levels can be exercised by considering the quantities N, λ and C_{P} as follows [6]:

N: k_{rv} can be reduced by minimizing the number of interrupters in series on the circuit-breaker.

λ: Choose a circuit-breaker with a low chopping number. For gas circuit-breakers, the chopping number tends to increase with arcing time and therefore the minimum arcing time should be as short as possible.

C_{P}: The grading capacitance value should be as low as possible.

For vacuum circuit-breakers, where the chopping number approach is not applicable, reference is made to Equation (64) and Appendix B. The only circuit-breaker characteristic in the equation is the chopped current level i_{c}. To provide some overvoltage level control, the choice is to select a vacuum circuit-breaker with contact material that minimizes current chopping [21].

The selection of circuit-breakers for non-effectively earthed shunt reactor switching at voltages $\leq$ 52 kV differs from that of the HV and EHV cases. At these voltages the current magnitudes are in the range of hundreds to thousands of Amperes (refer to Appendix A) and arc voltage rather than current chopping is the consideration. Each application should be related to the TRV requirements for T10/T30 in Table 13 of IEC 62271-100. The procedure to be followed is as follows:

a) Calculate the frequency of the load side oscillation:

$$f_{\mathrm{L}} = \frac{1}{2\pi\sqrt{1{,}5LC_{\mathrm{L}}}}$$

b) Calculate k_{a} from the equation given in Appendix E. Note that the second term under the square root will usually be negligible and k_{a} can thus be taken as equal to k_{in}.

c) Calculate k_{rv} from the equation given in Appendix E for α = 1:

k_{rv} = 2 + k_{in}

d) Calculate the time to peak t_{p} of the recovery voltage oscillation:

$$t_{\mathrm{p}} = \frac{1}{2f_{\mathrm{L}}}$$

e) Calculate the t_3 value:

t_3 = 0,087 × t_{p}

f) Calculate the rate of rise of the recovery voltage RRRV:

$$\mathrm{RRRV} = \frac{U_{\mathrm{r}}\sqrt{2}}{\sqrt{3}} \times k_{\mathrm{rv}} / t_3$$

g) Select the circuit-breaker rating from the above-noted table where both the recovery voltage peak and the rate of rise of recovery voltage equal or exceed the T10/T30 TRV values in the table.

9.2.7 Testing

EHV and HV circuit-breaker shunt reactor switching tests are normally unit tests in single phase circuits. The representation of the shunt reactor side circuit is of the essence. The test should be carried out using a directly connected HV shunt reactor and not a transformer coupled shunt reactor. This ensures that the load side oscillation is single frequency (as it should be), that the load side effective capacitance (C_{L}) can be exactly defined and that the proper interaction between the circuit-breaker and the circuit occurs. The exact definition of the load side effective capacitance, which includes the stray capacitances in the circuit and the circuit-breaker grading capacitance, is mandatory in order to determine the true chopping member of the circuit-breaker.

By reference to Equation (64), the worst case for suppression peak overvoltage generation is at minimum current giving the highest inductance value (L). The purpose of the testing is not so much to demonstrate interrupting capability – the current is after all forced to a premature zero – but rather to establish that the circuit-breaker meets certain performance criteria and to derive its chopping current and chopping number characteristics. These characteristics are dependent on arcing time for most circuit-breaker types and a large number of test shots are required in order to provide confidence in the results. In a typical test, the required number of test shots are applied over the expected range of arcing time and the suppression peak overvoltages are measured. Equation. (64) is used to calculate i_{c} (κ = 0) and then Equation (65) to calculate λ. A regression analysis is required to derive the chopping number characteristic and, once derived, the characteristic can be used to predict actual performance in the field [1, 2].

To be judged as suitable for shunt reactor switching, a circuit-breaker must meet the following two performance criteria:

a) Reignition should only occur at the first current zero after contact parting, i.e. the reignition window is less than one half-cycle.

b) All reignitions should occur between the arcing contacts.

The application of laboratory test results to actual shunt reactor applications is described in Appendix F. Statistical equations associated with Appendix F are given in Appendix G.

No testing is required for circuit-breakers used in unearthed shunt reactor switching applications. These applications lack the commonality of the chopping number approach and it would be impossible for any laboratory to carry the range of reactor sizes required for the purpose. However, because the applications can be related to the T10/T30 values as described above, these tests constitute proof of the breaker capability for the application.

9.3 Motor Switching

9.3.1 General

High voltage AC motors are typically in the range 2 to 14 kV and 100 kW to 40 MW and can be classified as follows [7]:

- asynchronous squirrel-cage motors, direct starting, starting current 6 to 7 times rated motor current, power factor 0,1 to 0,2;
- asynchronous slip-ring motors, starting current generally less than 6 times rated motor current;
- synchronous motors, often started by means of a squirrel-cage rotor, starting current 3 to 5 times motor rated current, power factor 0,25 to 0,3.

From a circuit-breaker (or contactor) perspective, the direct started asynchronous motor is the most important category. The characteristics of this application are [7]:

a) Starting current
   - high current (I = 6…7 $\times$ motor rated current);
   - low power factor (cos $\varphi \approx$ 0,1…0,2);
   - infrequent operation;
   - due to the higher interrupted current the chopping current can attain higher values;
   - the arcing time for some switching devices may be longer than when the motor is running;
   - according to practical experience the overvoltages when breaking the starting current are usually higher than when breaking no-load or load-current. In addition to possible higher chopping currents, overvoltages are also caused by reignitions, which usually are much more numerous when starting current is interrupted.

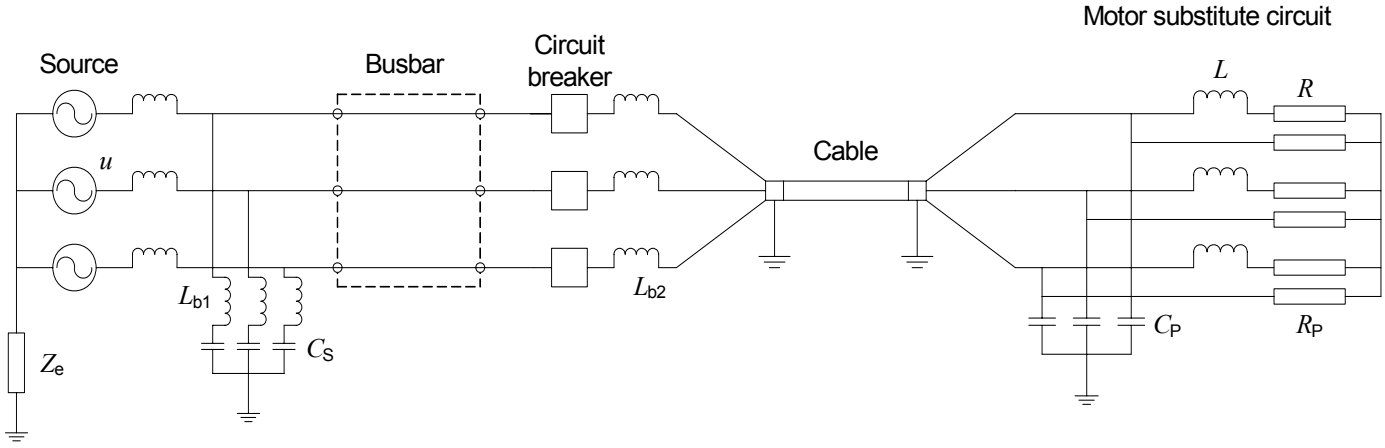
b) No-load current
   - the no-load current of a small HV motor may be lower than the chopping current level of the circuit-breaker;
   - the power-frequency recovery-voltage is very small compared to the case of breaking the starting current. As the rotor is running a voltage is induced in the stator with a frequency equal to the power frequency during the first periods;
   - reignitions are not likely as the recovery voltage is low;
   - low power factor (cos $\varphi \approx$ 0,1).

c) Load current
   - high power factor (cos φ = 0,7 – 0,9);
   - power-frequency recovery voltage is low;
   - low overvoltages, no reignitions.

With regard to breaking capability and overvoltage generation, it is clear that the breaking of starting current is the most severe case. This case is discussed in the following based on the CIGRE motor switching equivalent circuit approach.

9.3.2 Chopping and Reignition Overvoltages

The motor switching equivalent circuit is shown in Figure 54..



u	rated voltage	R_P	motor substitute parallel resistance
Z_e	earthing impedance	L_{b2}	inductance of connections
L_s	source side inductance	L	motor substitute inductance
C_s	supply side capacitance	R	motor substitute resistance
L_{b1}	inductance of capacitors and connections	C_P	motor substitute parallel capacitance

Figure 54 – Motor switching equivalent circuit

Motor switching is analogous to the non-effectively earthed shunt reactor switching case and the equations for this case as shown in Appendix B can be applied with the following qualifications:

a) C_L is the total motor and cable capacitance per phase. The cable is treated as a lumped capacitance.

   The equations for k_p and k_s are applicable for the single reignition case shown in Figure 51, i.e. no voltage escalation. Voltage escalation is discussed in 9.3.3 below.

   The chopping number approach is not applicable to vacuum circuit-breakers or contactors.

9.3.3 Voltage Escalation

A characteristic of vacuum circuit-breakers or contactors is their ability to interrupt high frequency currents. This can lead to repeated prestriking and interruption during a closing operation and repeated restriking and interruption during an opening operation. In both cases this can result in a phenomenon referred to as voltage escalation [8, 9]. Voltage escalation occurs when successive restriking and interruption results in increasing trapped current, and thus energy, in the motor winding and consequent increasing overvoltage levels. By reference to Equation (64), voltage escalation will cause an increase of the second component under the square root sign and is the equivalent of increasing the chopped current level. In fact, the phenomenon is frequently referred to as virtual current chopping being the suppression of one current (power frequency load current) by the superposition of another (the high frequency reignition current). It is usually reignition in one phase that causes virtual current chopping in the other two phases and it is related to mutual coupling between the phases [24]. However, occurrence is limited to small motors (20 – 100 kW) operating at the higher operating voltages of 6,6 kV or 11 kV [16, 17].

Voltage escalation is hazardous to the motor due to the high stress imposed on the turn-to-turn winding insulation by the steep fronted reignition overvoltage excursions. However,

voltage escalation can be suppressed by RC dampers or by gapped metal oxide surge suppressors on the load side of the motor [12, 13, 14, 15].

9.3.4 Overvoltage limitation

Some method of overvoltage limitation is applied in all motor circuits with the intent of protecting the motor insulation against steep front reignition overvoltage transients. The various methods and their effectiveness are reviewed in Table 11. The reignition circuit is that equivalent to the second parallel oscillation circuit described in 2.4.3.

Table 11 – Reignition overvoltage limitation method evaluation for motor switching

Overvoltage limitation method	How does the method work?	Advantage	Disadvantage
Surge arresters to earth at motor terminals [16, 17]	Limits overvoltage to earth at the motor.	Passive.	Effective only for circuit-breakers producing suppression peak overvoltages in excess of the surge arrester protective level; reignitions can still occur at up to twice the above protective level with no reduction in the reignition overvoltage excursion frequency; has little or no influence on multiple reignitions associated with vacuum circuit-breakers.
Surge suppressors at circuit-breaker terminals [14, 15]	Limits overvoltage to earth at the motor.	Passive; more effective than surge arrester given that it consists of a metal oxide varistor (MOV) in series with gap thereby resulting in a lower protective level.	Similar to that for surge arresters but more effective in limiting multiple reignitions.
Surge capacitors at motor terminals [16, 17]	Decreases frequency of the motor circuit recovery voltage and also frequency of the reignition overvoltage excursion.	Effective for circuit-breaker types other than vacuum circuit-breakers; may reduce k_a for vacuum circuit-breakers where the chopping current is dependent mainly on contact material	Multiple reignitions will still occur with vacuum circuit-breakers; single reignitions will still occur with other circuit-breaker types.
RC damper at motor terminals [12, 13, 17]	Introduces losses into the reignition circuit; high frequency reignition current damped and becomes exponentially decaying current with no zero crossing.	Properly selected can eliminate multiple reignitions, voltage escalation and virtual current chopping in adjacent phases.	Cost of losses in resistor; each installation may have to be treated as unique thereby restricting use of standard components; no waveshaping effect of capacitor; fast surges up to 3 p.u. still possible.
Zinc oxide (ZnO) RC-damper at motor terminals [17]	ZnO surge arrester is applied across the resistor and operates when the reignition overvoltage exceeds ≤ 1,5 p.u. inserting the capacitor.	Offers the advantages of both surge capacitors and RC-dampers; overvoltages can be limited to 2 p.u.	Cost of losses in resistor; each installation may be unique.
Series reactors [18]	Applied in series with the circuit-breaker provides damping of the high frequency reignition currents.	Damps the high frequency reignition currents and limits the voltage escalation process; reduces the steepness of the surges imposed on the motor windings.	Does not eliminate multiple reignitions and voltage escalation; not in common use having been applied only in Japan at voltages up to 6,6 kV; cost of losses; noise.
MOV across circuit-breaker [19]	Limits the voltage across the circuit-breaker at which reignitions can occur to the protective level of the varistor.	Magnitude and probability of reignitions are reduced; multiple reignitions and voltage escalation are suppressed.	Does not eliminate multiple reignitions and voltage escalation; steep surges can still be imposed on motor even though the magnitude of the overvoltages may be limited.
Controlled switching [20]	Ensures contact parting with respect to current wave such that interruption occurs at the first subsequent current zero.	Eliminate reignitions.	To date never used and thus unproven in motor starting current interruption application.

9.3.5 Circuit-breaker specification and selection

9.3.5.1 General

The specification and selection of circuit-breakers (or contactors) for motor switching is simpler than for the case of shunt reactors. While shunt reactor switching devices are often customized, off-the-shelf devices are generally used for motor switching. This is enabled by the application of overvoltage limitation measures as appropriate to the type of switching device.

9.3.5.2 Circuit-breaker specification

The following characteristics should be specified:

- dielectric withstand requirements;
- motor rating;
- motor starting, load and no-load currents;
- load side characteristics: motor starting equivalent inductance and the total effective capacitance including the connecting cable;
- mechanical endurance: class M1 or M2 in accordance with expected frequency of operation.

9.3.5.3 Circuit-breaker selection

The two predominant circuit-breaker technologies in use for motor switching today at medium voltage are SF_6 based on self-extinguishing and vacuum. While both technologies offer equal or relative performance with regard to application characteristics, both are well-suited for motor switching [19]. The choice of technology will in most cases be based on the installed cost of the circuit-breaker and associated overvoltage limitation measures.

9.3.6 Testing

The circuit-breaker should be tested in accordance with the requirements of [1].

9.4 Unloaded transformer switching

9.4.1 Oil-filled transformers

The switching of no-load oil-filled transformers from the high-voltage side using high-voltage circuit-breakers is not considered onerous or to be deserving particular attention. The reason for this is that the stresses imposed on the circuit-breakers are very much less severe than for any other switching duty. The current level is negligible – generally less than 10 A even at 100% excitation – and the transformer side TRV is in most cases over damped at a natural frequency of no more than a few hundred Hz. Apart from circuit-breakers this explains why air-break disconnectors equipped with fast-break attachments, as are common in North America, are capable of reignition-free or restrike-free transformer magnetizing current interruption. A field trace of an air-break disconnector, without a fast-break attachment, de-energizing a 230 kV no-load transformer is shown in Figure 55.

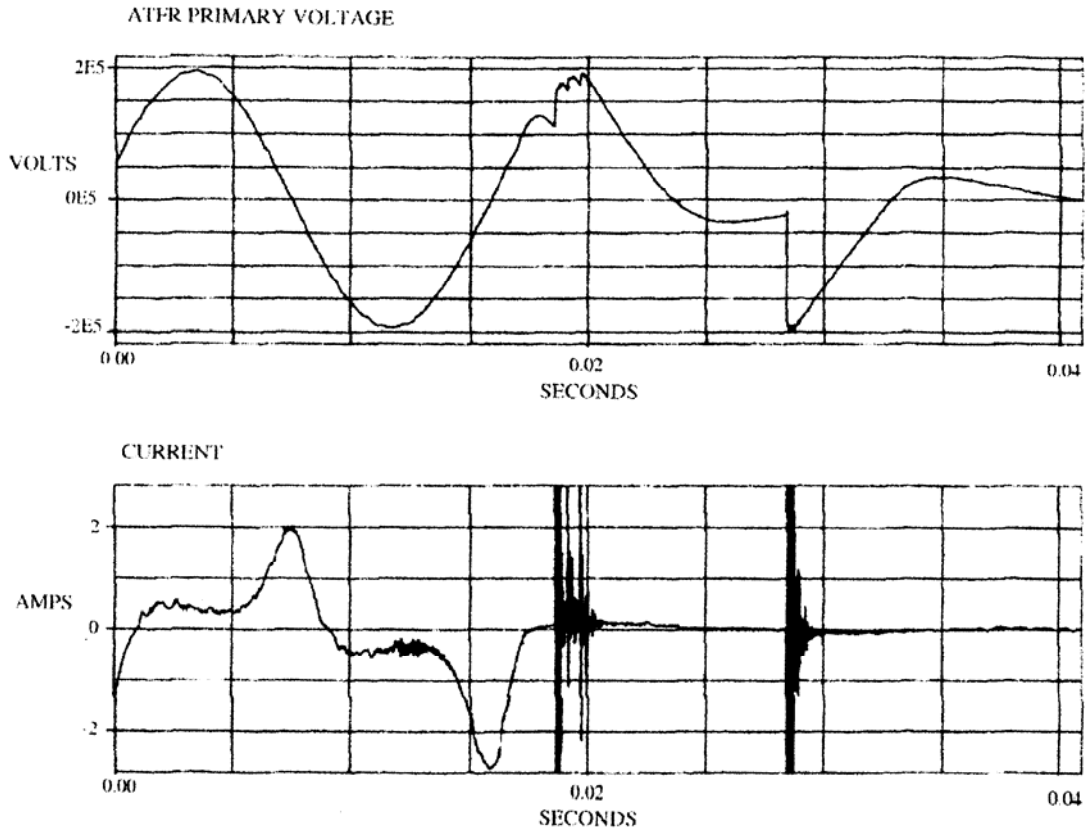


Figure 55 – De-energizing of a 230 kV no-load transformer with an air-break disconnector

In practice, where disconnectors are used to switch no-load transformers, due regard should be given to pre-striking and re-striking overvoltages and their impact on the transformer.

9.4.2 Dry type transformers

In systems at ≤ 52 kV the use of dry type transformers is common. Such transformers are often switched with vacuum circuit-breakers. This case has certain similarities to motor switching including the fact that there is usually a length of cable between the circuit-breaker and the transformer [8]. The transformers can be treated, as for both shunt reactors and motors, as a capacitance in parallel with an inductance. The effective capacitance is much lower than for oil-filled transformers and is in the order of 200 to 500 pF. The inductance is the magnetizing inductance of the transformer and the magnetizing currents are typically in the range 1 % to 3 % of rated full load current. For example, a 13,8 kV, 5 MVA transformer with 3 % magnetizing current would have a natural frequency of 3,8 kHz (C = 500 pF, L = 3,52 H) assuming that the core losses are insignificant.

9.4.2.1 Chopping and reignition overvoltages

Unloaded transformer switching is analogous to the solidly earthed shunt reactor switching case and the general equations for this case as shown in Appendix B can be applied to vacuum circuit-breakers with the following qualifications:

a) C_L is the total transformer and cable capacitance per phase, the cable being treated as a lumped. The influence of cable length is discussed below.

b) The equation for k_a is written as [8, 22]:

$$k_a = \sqrt{1+\eta\left(\frac{i_c}{V_0}\right)^2\left(\frac{L}{C_L}\right)} \qquad (79)$$

where η is the magnetic energy factor representing the portion of the magnetic energy dissipated in the reignition process. The value of η is estimated to be in the range 0,3 to 0,8 [8, 22]. The conservative approach however is to treat η as unity.

c) The equations for k_p and k_s are applicable for the single reignition case shown in Figure 51, i.e. no voltage escalation. Voltage escalation is discussed in 9.3.3 above.

d) The chopping number approach is not applicable to vacuum circuit-breakers or contactors.

In contrast to shunt reactor and motor switching, where the current to be interrupted is in the range of hundreds to thousands of amperes, magnetizing currents are in the order of amperes. This means that even the crest valve may be within the chopping capability of the switching device. Equation (76) applies for current chopping at the voltage crest and for current chopping away from the voltage crest Equation (80) below applies.

$$V_{\theta max} = \sqrt{(V_0 \sin\theta)^2 + \eta i_{c\theta}^2\left(\frac{L}{C_L}\right)} \qquad (80)$$

where $V_{\theta max}$ is the suppression overvoltage peak for a chopped current level of $i_{c\theta}$ at a point on-wave phase angle of θ on the voltage, θ being between 0 and 180 degrees.

On reignition in the circuit-breaker, inrush current may occur. Inrush current can be up to 15 times rated current and any instantaneous chopping of the current will not be possible. Chopping will be delayed for some milliseconds until the current approaches the chopping range of the circuit-breaker. The net effect of this is that the next reignition, should one occur, will be at a stepped up voltage due to the larger gap spacing.

Studies have shown that the overvoltage level on switching unloaded dry-type transformers is dependent on the length of cable between the circuit-breaker and the transformer [8]. The results indicate that the longer the cable the lower the overvoltage level, but the overvoltage level tends to increase with increasing MVA for constant cable length. The highest overvoltages occur on multiple reignitions and voltage escalation to as high as 3,5 p.u.; interruption of inrush current can result in overvoltages in excess of 5 p.u. [23].

9.4.2.2 Overvoltage limitation

Overvoltage limitation is considered by reference to that for motor switching as discussed in Table 11.

Surge arresters: studies indicate that surge arresters applied at the transformer terminals are effective in limiting overvoltages to earth for transformer sizes above a certain MVA value [8]. Below this MVA size, the overvoltages are below the surge arrester protective level. However, if interruption of inrush current is a possibility, then surge arresters are recommended [23].

Surge suppressors: by their nature, surge suppressors should provide somewhat better protection than surge arresters. Whether such devices have been applied in this context is unknown.

Surge capacitors: surge capacitors have the effect of reducing the surge impedance of the load and thereby the overvoltage levels [8].

RC dampers: effectiveness similar to that described for motor switching applications, i.e. will prevent multiple reignitions in vacuum circuit-breakers [24].

ZnO-RC dampers: effectiveness similar to that described for motor switching. Whether such devices have been applied in this context is unknown.

Series reactors and controlled switching are not viewed as being applicable to this switching duty.

9.4.2.3 Circuit-breaker specification and selection

In most cases, circuit-breakers rated at 52 kV and below are specified and selected according to requirements other than unloaded transformer switching. The reason for this is that the circuit-breakers are taken to inherently have this capability with due regard to possible overvoltage limitation.

9.4.3 Testing

Due to the enormous variations in transformer ratings and the non-linear behaviour of the core, it is not possible to model the switching of no-load transformers using linear components in a test laboratory. A test on an available transformer would only be valid for that transformer at the particular level of excitation used and would not be representative for other excitation levels on the same transformer and certainly not for other transformers. In summary, type testing for no-load transformers is not required for two reasons. Firstly, the duty is less severe than any other switching duty and secondly, the duty cannot in any case be correctly modelled in a test laboratory.

In exceptional cases at voltages of 52 kV and below where there is an agreement with the manufacturer and the user to test a specific combination of circuit-breaker and transformer, reference can be made to the French National Standard[2] for unloaded transformer switching tests for circuit-breakers rated at 1 kV to 36 kV.

9.5 References

NOTE Reference 2 below includes an extensive list of references which are not repeated here.

[1] IEC 62271-110, Ed. 1: High-voltage switchgear and controlgear – Part 110: Inductive load switching. To be published in 2005

[2] IEEE Standard C37.015 IEEE Application Guide for Shunt Reactor Switching, 1993

[3] D. Dufournet, “Arc Modelling Applied to Small Inductive Currents Interruption.” CIGRE Paper No. 13-01, 1988

[4] J.A. Bachiller, E. Cavero, F. Salamanca and J. Rodriguez, “The Operation of Shunt Reactors in the Spanish 400 kV Network – Study of the Suitability of Different Circuit-breakers and Possible Solutions to Observed Problems.” CIGRE Paper No. 23-106, 1994

[5] A.K. McCabe, G. Seyrling, J.D. Mandeville and J.M. Willieme, “Design and Testing of a Three-Break 800 kV SF_6 Circuit-breaker with ZnO Varistors for Shunt Reactor Switching.” Proceedings IEEE PES T&D Conference 1991

[6] D.F. Peelo and J.H. Sawada, “Experience with Controlled Transmission Line Autoreclosing and Controlled Shunt Reactor Switching on B.C. Hydro System.” CIGRE Paper No. 13-101, 1998

[7] Interruption of small inductive currents: Chapter 3, Part A. Electra No. 75, March 1981

[8] J.F. Perkins, “Evaluation of Switching Surge Overvoltages on Medium Voltage Power Systems.” IEEE Transactions of Power Apparatus and Systems, Vol. PAS-101(6), June 1982

[9] A. Greenwood and M. Glinkowski, “Voltage Escalation in Vacuum Switching Operations.” IEEE Transactions on Power Delivery, Vol. 3, No. 4, October 1988

---

[2] UTE C64-115, February 1990.

[10] M. Murano, T. Fujii, H. Nishikawa, S. Nishiwaki and M. Okawa, “Three-phase Simultaneous Interruption in Interrupting Inductive Current Using Vacuum Switches.” IEEE Transactions on Power Apparatus and Systems, Vol. PAS-93, 1974

[11] J. Panek and K.G. Fehrle, “Overvoltage Phenomena Associated with Virtual Current Chopping in Three-phase Circuits.” IEEE Transactions on Power Apparatus and Systems, Vol. PAS-94, 1975

[12] M. Murano, T. Fujii, H. Nishikawa, S. Nishiwaki and M. Okawa, “Voltage Escalation in Interrupting Inductive Current by Vacuum Switches.” IEEE Transactions on Power Apparatus and Systems, Vol. PAS-93, 1974

[13] J.P. Eichenberg, H. Hennenfent and L. Liljestrand, “Multiple Restrikes Phenomenon when Using Vacuum Circuit-breakers to Start Refiner Motors.” Pulp & Paper Canada 98:7 (1977)

[14] A. Luxa and A. Priess, “Switching of Motors During Start-up.” Siemens Power Engineering and Automation VII (1985)

[15] S.H. Telander, M.R. Wilhelm and K.B. Stump, “Surge Limiters for Vacuum Circuit-breakers,” IEEE Transactions on Industry Applications, Vol. 24, No. 4, 1988

[16] R.E. Pretorius, “Guide for the Application of Switching Surge Suppressors to Medium Voltage Motors.” Report for Electric Power Coordinating Committee, South Africa

[17] R.E. Pretorius, “The Suppression of Internal Overvoltage Surges in Industrial High Voltage Systems.” The Certified Engineer, July 1981, South Africa

[18] Y. Murai, T. Nitta, T. Takami and T. Itoh, “Protection of Motor from Switching Surge by Vacuum Switch.” IEEE Transactions on Power Apparatus and Systems, Vol. PAS-93, 1974

[19] A.M. Chaly, A.T. Chalaya, V.N. Poluyanov and I.N. Poluyanova, “The Peculiarities of Interruption of the Medium Voltage Motors by VCB with CuCr Contacts.” IEEE 18th International Symposium on Discharges and Electrical Insulation in Vacuum, Eindhoven 1998

[20] C. Cereda, C. Gemme and C. Reuber, “Synchronous MV Circuit-breaker with Magnetic Drive and Electronic Control.” ABB Review 6/99

[21] D. Braun, W. Hellmann and A. Plessl, “Application Criteria for SF_6 and Vacuum Circuit-breakers.” ABB Review 4/99

[22] J. Kopainsky and E. Ruoss, “Interruption of Low Inductive and Capacitive Currents in High Voltage Systems.” Brown Boveri Review 4-79

[23] W.M.C. van den Heuvel, J.E. Daalder, M.J.M. Boone and L.A.H. Wilmes, “Interrution of Dry-Type Transformer in No-Load by a Vacuum Breaker.” Eindhoven University of Technology Report 83-E-141, August 1983

[24] G.C. Damstra, “Virtual chopping phenomena switching three-phase inductive currents” CIGRE SC 13 colloquium, Helsinki, Finland, 1981

Appendix A

Shunt reactor characteristics

At 72,5 kV and above, shunt reactors are directly connected to station busbars or to transmission line terminations and are solidly earthed or through a neutral reactor (sometimes referred to as a four-reactor scheme). At voltages below 72,5 kV, reactors are commonly connected to system transformer tertiary windings and are usually unearthed

A.1 Shunt reactors rated 72,5 kV and above

The majority of the installed shunt reactors at 72,5 kV and above are in the 30 Mvar to 300 Mvar (three-phase) range. The largest single-phase units have a rating of 400 Mvar as a three-phase group.

The characteristics of shunt reactors depend to a great extent on the design, which can be:

- three-legged gapped iron-core;
- five-legged gapped iron-core;
- shell-type gapped iron-core;
- coreless (air-cored).

Table A.1 gives some typical shunt reactor characteristics.

Table A.1 – Typical shunt reactor electrical characteristics

Applied voltage	Rating	Power frequency	Rated current	Inductance	Capacitance	Natural frequency
kV	Mvar	Hz	A	H	nF	kHz
765	150 – 300	60	113 – 226	5,17 – 10,35	1,7 – 4,0	1,1 – 1,7
735	330	60	259	4,34	4,1	1,2
525	135	60	148	5,43	1,8 – 4,0	1,1 – 1,6
400	120 – 200	50	173 – 289	2,55 – 4,25	1,9 – 3,2	1,4 – 2,3
236	125	60	306	1,18	2,1	3,2
132	55	50	240	1,0	1,3	4,4
115	25	60	126	1,4	2,9	2,5
60	20	60	190	0,48	2,0	5,1
36	35 – 100	50/60	560 – 1600	98 – 34	0,8 – 2 [a)]	9 – 16 [b)]
24	35 – 100	50/60	840 – 2400	44 – 15	0,8 – 2 [a)]	14 – 24 [b)]
17,5	40 – 80	50/60	1400 – 2600	20 – 10	0,8 – 2 [a)]	21 – 29 [b)]
12	40 – 75	50/60	1900 – 3600	10 – 5	0,8 – 2 [a)]	29 – 41 [b)]

[a)] Oil-filled reactor capacitance phase-to-earth ignoring internal capacitive coupling between phases.

[b)] Applicable to first-pole-to-clear.

In the range 72,5 kV to 245 kV, reactors are most commonly oil-filled and have three-legged gapped cores with layer, continuous disc or interleaved disc windings. Future reactors in the range 69 kV to 145 kV will tend to be air-cored dry coil units.

At 300 kV to 550 kV, reactors are single-phase or three-phase units with three-legged, five-legged or shell-type cores (with the wound core legs gapped). The windings are of the layer, continuous disc or interleaved disc type.

At 735 kV and 765 kV, reactors are almost exclusively banks of single-phase units with similar constructions as for 550 kV single-phase units.

The effective capacitance values of the reactors are dependent on the design and construction. For oil-filled units, the capacitance is composed of bushing capacitance, winding series capacitance and winding capacitances to earth or to shields. Bushing capacitances range from 500 pF to 800 pF.

Effective winding capacitances vary from a minimum of about 1 200 pF to a maximum of about 3 500 pF, layer windings having the lowest values and interleaved disc windings the highest values. For dry coil units, no bushings are involved and capacitance is that due to windings to earth and winding series capacitance. Both of these values are low, the latter so because of the large number of turns inherent in such coils, and the effective capacitance is in the range 300 pF to 500 pF.

For general reactor switching application and laboratory testing purposes, oil-filled reactors can reasonably be assumed to have an effective capacitance of at least 2 000 pF. This will give natural frequencies of 1 kHz to 5 kHz for reactors rated 72,5 kV to 800 kV, the lower frequencies being applicable at the higher voltages and vice versa.

A.2 Shunt reactors rated below 72,5 kV

Shunt reactors rated below 72,5 kV are either oil-filled, three-legged iron-core units or dry coil units. Table A.1 gives some typical shunt reactor characteristics in this range.

Table A.1 illustrates the wide range of current and natural frequency applicable in this voltage range. For dry-coil reactor units, the capacitance to earth is in the range 300 pF to 500 pF and the corresponding natural frequencies will be two to three times those given in the above table.

Appendix B

System and station characteristics

System (source) and station characteristics interact with the circuit-breaker during the switching of shunt reactors and must be considered in the application of circuit-breakers for this purpose.

B.1 System characteristics

The system characteristics which impact on reactor switching are the source inductance and the source side capacitance. The source inductance can be derived from the prevailing short-circuit level at the station. The source side capacitance is in general very much greater than the load side capacitance. For circuit-breaker type testing purposes, the former capacitance is assumed to be at least ten (10) times greater than the latter.

B.2 Station characteristics

Directly connected shunt reactors are connected either to station busbars or to overhead lines. A worldwide survey has shown that connection to busbars is three times more common than that to transmission lines. The characteristics which are of relevance are the inductance of the connecting busbar or line and any capacitances in addition to that of the reactor. Typical values are given in Table B.1.

Table B.1 – Connection characteristics for shunt reactor installations

Connection	Inductance µH/km	Capacitance pF/m
Busbar/line	1	10
Cable	0,2 – 0,5	200 – 400
GIS	0,2	60

The inductance of even the longest connection lengths (150 m to 200 m) is not significant compared to the inductance of high-voltage reactors, but does influence the reignition process. The capacitance of long connecting busbar/line lengths (up to 170 m reported), and relatively short cable or busbars in gas insulated substations (GIS) lengths is significant compared to that of the reactor and must be considered. Additionally, other connected equipment between the circuit-breaker and the reactor will also contribute to the overall load side capacitance and may also require consideration. Capacitance values for such equipment are given in Table B.2.

Table B.2 – Capacitance values of various station equipment

Equipment	Capacitance* nF
Capacitive voltage transformers	2 – 16
Current transformers	0,15 – 1,2
Voltage transformers	0,15 – 0,45
Surge arresters	0,08 – 0,12
Switch disconnectors	0,06 – 0,20
Busbar support insulators	0,05
GIS air entrance bushings - SF_6 - Capacitor - Epoxy	 0,03 – 0,15 0,10 – 1 0,10 – 1
* Variation is with voltage rating	

Appendix C

Current chopping level calculation

When interrupting small inductive currents, circuit-breakers will force the current to zero prior to the natural current zero. This phenomenon is referred to as current chopping, the degree of which and associated resultant overvoltages, depends on the type of circuit-breaker and the circuit involved.

Current chopping is caused by an unstable interaction between the arc and the circuit. Arc instability is defined as any abrupt change in the conductivity of the arc occurring away from the natural zero in the current loop and having its origin in the arc characteristic and/or the arc cooling mechanism. In the early 1960s Rizk showed for arcs in gases and oil that, following a rapid change of arc current, the arc voltage will approach a new stationary value through an exponential curve, which is characterized by a time constant [1, 2]. Assuming initial static arc conditions of a current I_a giving an arc voltage of U_a, the response to a step current change of δI is:

$$U(t) = U_a + R_i \delta I + (R_a - R_i)\delta I e^{-t/\theta},$$

where $R_i = \left(\frac{dU}{dI}\right)_{I=I_a}$ i.e. the incremental or dynamic arc resistance, which is negative for low current arcs (see Figure C.1),

$R_a = \frac{U_a}{I_a}$, the static arc resistance

and θ is the thermal time constant of the arc. θ is proportional to the current and is dependent on the circuit-breaker cooling mechanism [1].

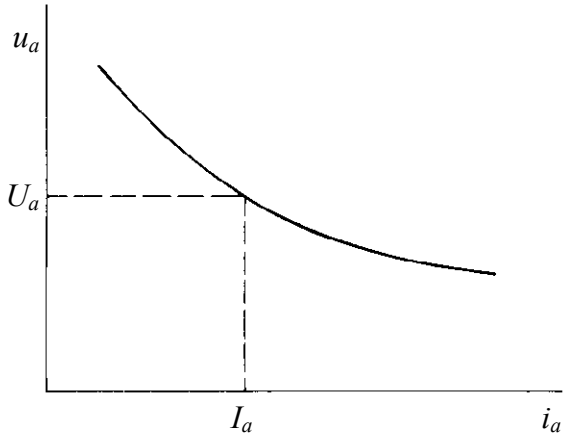


Figure C.1 – Arc characteristic

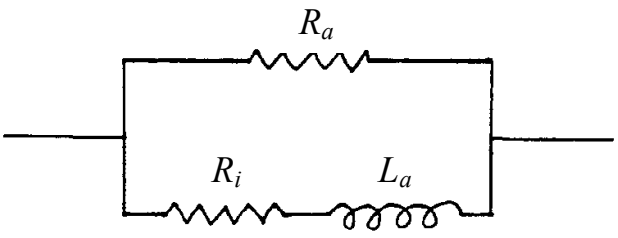


Figure C.2 – Rizk's equivalent circuit for small current deviations from steady state

Rizk recognized that the above behaviour could be represented by means of an equivalent circuit assuming that the static characteristic of the arc is given by the equation:

$$u_a i_a^{\alpha} = n \qquad \text{(C.1)}$$

where u_a is the arc voltage, i_a the arc current, α a constant and n a statistically random variable.

The equivalent circuit for the arc is shown in Figure A.2.

In the equivalent circuit, R_a is as defined above and

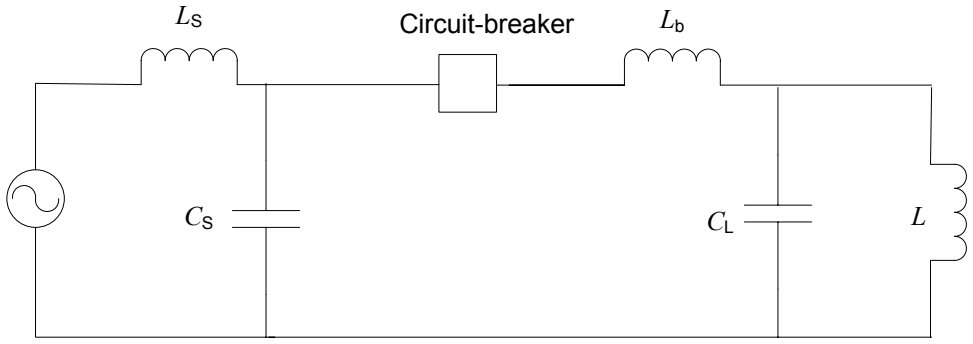
$$R_i = -\frac{\alpha R_a}{1+\alpha} \qquad \text{(C.2)}$$

and

$$L_a = \frac{\theta R_a}{1+\alpha} \qquad \text{(C.3)}$$

The single-phase equivalent circuit for inductive current switching is shown in Figure C.3.

In Figure C.3:



L_s	source side inductance
L	load inductance
C_s	source side capacitance
C	load side capacitance
L_b	stray inductance between C_s and the load

Figure C.3 – Single phase equivalent circuit

L_s and L are large enough to prevent rapid current changes and L_b is assumed small enough to be neglected. Therefore, the external circuit which interacts with the arc can be first reduced to C_s and C in series; however, since $C_s \approx C$, the circuit reduces further to C alone.

The combined arc/external-circuit circuit that can be used to calculate the instability limit is as shown in Figure C.4.

The impedance Z of the circuit is:

$$Z = \frac{R_{\mathrm{a}}\left(R_{\mathrm{i}} + \mathrm{j}\omega L_{\mathrm{a}}\right)}{R_{\mathrm{a}} + R_{\mathrm{i}} + \mathrm{j}\omega L_{\mathrm{a}}} + \frac{1}{\mathrm{j}\omega C} \tag{C.4}$$

or

$$Z = R^{*} + \mathrm{j}\left(\omega L^{*} - \frac{1}{\omega C}\right) \tag{C.5}$$

where

$$R^{*} = \frac{R_{\mathrm{a}}R_{\mathrm{i}}\left(R_{\mathrm{a}} + R_{\mathrm{i}}\right) + \omega^{2}R_{\mathrm{a}}L_{\mathrm{a}}^{2}}{\left(R_{\mathrm{a}} + R_{\mathrm{i}}\right)^{2} + \omega^{2}L_{\mathrm{a}}^{2}} \tag{C.6}$$

and

$$L^{*} = \frac{L_{\mathrm{a}}R_{\mathrm{a}}}{\left(R_{\mathrm{a}} + R_{\mathrm{i}}\right)^{2} + \omega^{2}L_{\mathrm{a}}^{2}} \tag{C.7}$$

The circuit becomes unstable when the real part of Z, i.e. R^{*}, becomes negative resulting in negative damping. This occurs, then, at an angular frequency of ω_{i} (the instability limit) when

$$R_{\mathrm{a}}R_{\mathrm{i}}\left(R_{\mathrm{a}} + R_{\mathrm{i}}\right) + \omega_{\mathrm{i}}^{2}R_{\mathrm{a}}L_{\mathrm{a}}^{2} < 0 \tag{C.8}$$

Substituting for R_{i} and L_{a} (Equations C.2 and C.3) in C.8 gives

$$\omega_{\mathrm{i}} < \frac{\sqrt{\alpha}}{\theta} \tag{C.9}$$

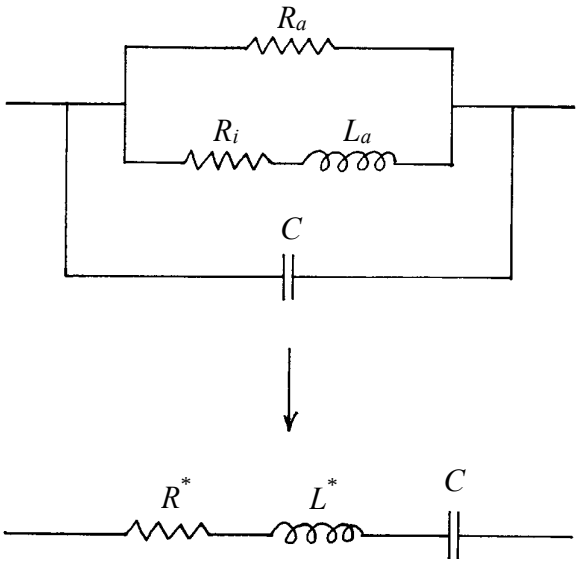


Figure C.4 – Circuit for calculation of arc instability

At ω_{i}, the arc behaves like a pure inductance

$$L^{*}\omega_{\mathrm{i}} = \frac{L_{\mathrm{a}}R_{\mathrm{a}}}{\left(R_{\mathrm{a}} + R_{\mathrm{i}}\right) + \omega_{\mathrm{i}}^{2}L_{\mathrm{a}}^{2}}$$

Again substituting for R_i and L_a, this gives

$$L^*_{\omega i} = \theta R_a \qquad \text{(C.10)}$$

Now,

$$\omega_i^2 = \frac{1}{L^*_{\omega i} C} = \frac{1}{\theta R_a C} = \frac{\alpha}{\theta^2}$$

or

$$\alpha R_a C = \theta \qquad \text{(C.11)}$$

The circuit will become instable and chop the current when Equation C.11 is fulfilled. If I_c is the chopped current, then at chopping

$$R_a = \frac{U_{ac}}{I_c}$$

but $U_{ac} = n I_c^{-\alpha}$ giving

$$R_a = n I_c^{-\alpha-1} \qquad \text{(C.12)}$$

Substituting for R_a in Equation C.11

$$\alpha n I_c^{-\alpha-1} C = \theta$$

or

$$I_c = \left(\frac{\alpha n}{\theta} \cdot C \right)^{\frac{1}{\alpha+1}} \qquad \text{(C.13)}$$

Laboratory tests have shown that α is approximately 1 and thus

$$I_c = \sqrt{\frac{n}{\theta} C} \qquad \text{(C.14)}$$

or

$$I_c = \lambda \sqrt{C} \qquad \text{(C.15)}$$

Equation C.15 has been shown to be valid for air-blast [4, 5], minimum oil [3, 5] and SF_6 circuit-breakers [5, 6, 7]. The frequency of the instability oscillation is high and chopping can be considered to be instantaneous.

References

[1] F. Rizk, “Arc Instability and Time Constant in Air-Blast Circuit-breakers.” CIGRE Paper No. 107, 1964

[2] F. Rizk, “Arc Response to a Small Unit-Step Current Pulse.” Elteknik, Volume 7, Part 2, February 1964

[3] S. Berneryd, C.E. Solver, L. Ahlgren and R. Eriksson, “Switching of Shunt Reactors Comparison Between Field and Laboratory Tests.” CIGRE Paper No. 13-04, 1976

[4] A.U. Dowell, G.E. Gardner, R.J. Urwin, F.P. Matraver and W. Watson, “A Review of Switchgear Testing Requirements Including the Interruption of Low Inductive Currents.” CIGRE Paper No. 13-02, 1976

[5] M. Murano, S. Yanabu, H. Ohashi, H. Ishizuka and T. Okazaki, “Current Chopping Phenomenon of Medium Voltage Circuit-breakers.” IEEE Transactions Vol. PAS-96, No. 1, January/February 1977

[6] J.C. Henry, G. Perrissin and C. Rollier, “The Behaviour of SF_6 Puffer Circuit-breakers Under Exceptionally Severe Conditions.” CIGRE Paper No. 13-08, 1978

[7] R. Eriksson, S. Berneryd and A. Eriksson, “Laboratory and Field Tests with a 420 kV SF_6 Puffer Breaker for a Gas Insulated Substation.” IEE Conference on High Voltage Switchgear Publication 182, 1979

Appendix D

Summary of overvoltage factors for solidly earthed, non-effectively earthed and reactor earthed reactors

Overvoltage factor in p.u.	Solidly earthed reactor	Non-effectively earthed reactor	Reactor earthed reactor (general formula)
k_a	$\sqrt{1+\left(\frac{i_c}{V_o}\right)^2\left(\frac{L}{C_L}\right)}$ $\approx\sqrt{1+\left(\frac{1{,}5N\lambda^2}{\omega Q}\right)\left(\frac{C_P}{C_L}+1\right)}$	$1{,}5\sqrt{1+\frac{1}{1{,}5}\left(\frac{i_c}{V_o}\right)^2\left(\frac{L}{C_L}\right)}-0{,}5$ $\approx 1{,}5\sqrt{1+\left(\frac{\lambda^2}{\omega Q}\right)}-0{,}5$	$(1+\kappa)\sqrt{1+\frac{1}{(1+\kappa)}\left(\frac{i_c}{V_o}\right)^2\left(\frac{L}{C_C}\right)}-\kappa$ $\approx(1+\kappa)\sqrt{1+\frac{1{,}5}{(1+\kappa)}\left(\frac{N\lambda^2}{\omega Q}\right)\left(\frac{C_P}{C_L}+1\right)}-\kappa$
κ	0	0,5	$\frac{1}{2+\frac{L}{L_N}}$
k_b	k_a	$k_a+0{,}5$	$k_a+\kappa$
k_c	αk_a	$0{,}5+\alpha(k_a+0{,}5)$	$\kappa+\alpha(k_a+\kappa)$
k_{rv}	$1+\alpha k_a$	$1{,}5+\alpha(k_a+0{,}5)$	$(1+\kappa)+\alpha(k_a+\kappa)$
k_p	$1+\beta(1+\alpha k_a)$	$1+\beta[1{,}5+\alpha(k_a+0{,}5)]$	$1+\beta[(1+\kappa)+\alpha(k_a+\kappa)]$
k_s	$(1+\beta)(1+\alpha k_a)$	$(1+\beta)[1{,}5+\alpha(k_a+0{,}5)]$	$(1+\beta)[(1+\kappa)+\alpha(k_a+\kappa)]$
α is the damping factor associated with the chopping overvoltage oscillation and is in the order of 0,9 A conservative approach is to assume α=1. β is the damping factor associated with the reignition overvoltage oscillation and can be assumed to be 0,5			

Appendix E

Summary of overvoltage factors for non-effectively earthed reactors with and without arc voltage

Overvoltage factor in p.u.	No arc voltage	With arc voltages
k_a	$1{,}5\sqrt{1+\frac{1}{1.5}\left(\frac{i_c}{V_o}\right)^2\left(\frac{L}{C_L}\right)}-0{,}5$ $\approx 1{,}5\sqrt{1+\left(\frac{\lambda^2}{\omega Q}\right)\left(\frac{C_s}{C_s+C_L}\right)}-0{,}5$	$\sqrt{(k_{in}+0{,}5)^2+1{,}5\left(\frac{i_c}{V_o}\right)^2\left(\frac{L}{C_L}\right)}-0{,}5$ $\approx \sqrt{(k_{in}+0{,}5)^2+\left(\frac{1{,}5\lambda^2}{\omega Q}\right)\left(\frac{C_s}{C_s+C_L}\right)}-0{,}5$
K	0,5	
k_b	$k_a+0{,}5$	
k_c	$0{,}5+\alpha(k_a+0{,}5)$	
k_{rv}	$1{,}5+\alpha(k_a+0{,}5)$	
k_p	$1+\beta[1{,}5+\alpha(k_a+0{,}5)]$	
k_s	$(1+\beta)[1{,}5+\alpha(k_a+0{,}5)]$	

α is the damping factor associated with the chopping overvoltage oscillation and is in the order of 0,9. A conservative approach is to assume α=1.

β is the damping factor associated with the reignition overvoltage oscillation and can be assumed to be 0,5.

k_{in} = source voltage crest value plus the arc voltage in p.u..

Appendix F

Application of laboratory test results to actual shunt reactor installations

F.1 General

The purpose of this appendix is to describe the procedure, based on laboratory test results, to be followed to estimate the overvoltage levels that will occur in actual shunt reactor installations and to determine the suitability of a particular circuit-breaker for the purpose.

The procedure described applies principally to shunt reactor installations with solidly earthed neutrals. The procedure may however be applied with suitable adaptation to the unearthed and neutral reactor earthed cases. Due to the statistical nature of overvoltage generation, it is necessary to apply statistical methods to estimate the risk for overvoltages at or above certain levels. Applicable statistical equations are given in Appendix G for convenience.

F.2 Overvoltage estimation procedures

F.2.1 Chopping number of one interrupter

The main characteristic evaluated in the laboratory test is the chopping number (λ). The chopping number is an inherent characteristic of the circuit-breaker and is usually independent of the circuit. The chopping number can therefore be used to estimate the behaviour of the circuit-breaker in other circuits than the test circuit.

The chopping number varies statistically and must be expressed in terms of:

- a mean value;
- a standard deviation;
- dependence on arcing time (if applicable).

The chopping number for a single interrupter circuit-breaker is defined by:

$$\lambda = i_{\mathrm{ch}} / \sqrt{C_{\mathrm{t}}} \qquad \text{(F.1)}$$

where

i_{ch} is the chopped current value; and

C_{t} is the total capacitance in parallel with the circuit-breaker.

The value of chopped current should, if possible, be directly measured for each test and current zero at which interruption is attempted or achieved.

If actual measurement is not possible, then i_{ch} can be calculated for *solidly earthed reactors* using the following equation:

$$i_{\mathrm{ch}} = u_0 \sqrt{\frac{C_{\mathrm{L}}}{L}\left(k_{\mathrm{a}}^2 - k_{\mathrm{in}}^2\right)} \qquad \text{(F.2)}$$

with $k_{\mathrm{in}} = u_{\mathrm{in}}/u_{\mathrm{o}}$ = initial load voltage in p.u. to earth at the moment of chopping.

λ is then calculated using Equation (F.1).

For circuit-breakers above 72,5 kV the arc voltage can be neglected in comparison with u_o and k_{in} = 1 can be used in Equation (F.2).

Equation (F.2) is restricted to single-phase reactors or solidly earthed reactors. The determination of the chopping number is usually made in single-phase tests.

If only three-phase tests with *unearthed reactors* are available for estimation of the chopping number, Equation (F.3) can be used. For medium-voltage circuit-breakers the arc voltage may be substantial and the recorded value of u_{in} has then to be used in the calculation.

$$i_{ch} = u_o \sqrt{\frac{2C_L}{3L}} \left[(k_a + 0{,}5)^2 - (k_{in} + 0{,}5)^2 \right] \qquad \text{(F.3)}$$

If C_L is not explicitly known, it can be calculated from the load oscillation frequency since the effective inductance can be assumed equal to the power frequency value, L, which is always known. Refer to 9.2.4.

The values of i_{ch} and λ will vary statistically from test to test. If the values show no clear dependence on the arcing time, the statistical variation is usually a normal distribution. On this basis, the mean value, λ_{mean}, and the standard deviation s are calculated according to Appendix G.

In the event that i_{ch} and λ exhibit a clear dependence on arcing time, a linear relationship can be assumed as a first approximation:

$$\lambda_{mean} = A + Bt_a \qquad \text{(F.4)}$$

where t_a is the arcing time. The constants A and B can be derived by performing a linear regression. The dispersion around the regression line will probably be wide and therefore it is also necessary to derive the standard deviation of the regression line (generally referred to as the standard error of estimate). Refer to F.3 below and Appendix G.

F.2.2 Estimation of chopping overvoltages in shunt reactor installations

For the first case, where the chopping number is independent of the arcing time, the maximum chopping number for one interrupter is given by:

$$\lambda_{max} = \lambda_{mean} + 2\sigma \qquad \text{(F.5)}$$

Statistically, this is the 2% value, i.e. the value that will be exceeded in less than 2% of the switching operations.

To estimate the maximum chopping overvoltage to earth for a circuit-breaker with N interrupters in series, the applicable value of λ_{max} is inserted in Equation (F.6), if the arc voltage can be neglected, i.e. k_{in} = 1.

$$k_{b\,max} = [1 + \kappa] \sqrt{1 + \frac{N\lambda_{max}^2 \times L}{u_0^2 (1 + \kappa)} \times \frac{C_t}{C_L}} \qquad \text{(F.6)}$$

$k_{a\,max} = k_{b\,max} - \kappa$

$k_{c\,max} = k_{b\,max} + \kappa$

where

$k_{a\,max}$ is the maximum suppression peak overvoltage to earth (2% value), in p.u. of u_o;

$k_{b\,max}$ is the initial amplitude of load oscillation, in p.u. of u_o;

$k_{c\,max}$ is the maximum voltage to earth at the recovery peak (2% value), in p.u. of u_o;

u_o is the crest phase-to-earth voltage of the network;

κ is the offset voltage of the neutral point, in p.u.;

L is the effective phase-to-neutral load inductance;

N is the number of interrupters in series per pole;

C_t is the total capacitance parallel to the circuit-breaker;

C_L is the total effective load capacitance neglecting C_p.

$C_L = C_G + 2C_\varphi$ for the first phase-to-clear taking phase-to-phase capacitances, C_φ, into account, where C_G is the total capacitance to earth (including capacitance to earth of connections).

For solidly earthed reactors ($\kappa = 0$) the highest chopping overvoltage is the suppression peak ($k_a = k_b \approx k_c$), while for unearthed and neutral reactor earthed reactors, the maximum chopping overvoltage to earth occurs at the recovery peak.

Often one can assume that the supply side capacitance to earth is much larger than the load capacitance, $C_S >> C_L$, which simplifies the equation above by setting $C_t/C_L \approx 1$. This is generally the case with several lines/cables connected to the busbar. However, if this assumption is not valid, the chopping level is reduced resulting in lower chopping overvoltages. Therefore Equation (F.6) with $C_t/C_L = 1$ gives a conservative result.

By inserting:

$$u_0^2 = \frac{2\omega LQ}{3} \text{ and } \frac{C_t}{C_L} = 1$$

into Equation (F.6) the following equation for *solidly earthed reactors* ($\kappa = 0$) is given:

$$k_{a\,max} = \sqrt{1 + \frac{3N\lambda^2}{2\omega Q}} \qquad \text{(F.7)}$$

where

Q is the three-phase reactive power of reactor, in var; and

ω is the angular power frequency (314 or 377 for 50 Hz and 60 Hz, respectively).

For the second case, where the chopping number is dependent on arcing time, the maximum chopping number will occur at the maximum arcing time, $t_{a\,max}$ The maximum chopping number (2% value) for a single interrupter is given by:

$$\lambda_{max} = (A + Bt_{a\,max} + 2S_e) \qquad \text{(F.8)}$$

where S_e is the standard error of estimate defined in Appendix G.

The maximum chopping overvoltage is calculated using equations (F.6) or (F.7), depending on whether the reactor is solidly earthed or not.

F.2.3 Estimation of reignition overvoltages in shunt reactor installations

It is important to note that overvoltages occurring in laboratory tests due to reignitions have no relevance for the estimation of reignition overvoltages in actual shunt reactor installations. Estimated reignition overvoltage levels are derived on the basis described in 9.2.3.

For the case where the chopping number is independent of arcing time, reignition overvoltages k_p and k_s are given by:

$$k_{p\ max} = 1 + \beta\,(1 + k_{b\ max\ r} + \kappa) = 1 + \beta\,(1 + k_{a\ max\ r} + 2\ \kappa) \qquad \text{(F.9)}$$

$$k_{s\ max} = (1 + \beta)\,(1 + k_{b\ max\ r} + \kappa) = (1 + \beta)\,(1 + k_{a\ max\ r} + 2\ \kappa) \qquad \text{(F.10)}$$

where

$k_{p\ max}$ is the maximum reignition overvoltage to earth (2 % value) in p.u.;

$k_{s\ max}$ is the maximum reignition overvoltage peak-to-peak transient (2 % value) in p.u.;

$k_{a\ max\ r}$ is the maximum suppression peak overvoltage value in p.u. at interruptions with reignitions (derived using equations (F.6) or (F.7));

$k_{b\ max\ r}$ is the maximum initial amplitude of load oscillation at interruptions with reignitions (derived using Equation (F.6));

β is a damping factor assumed to be $\beta \approx 0{,}5$.

For circuit-breakers, whose chopping numbers vary with arcing time, the applicable k_a value is that obtained at the longest arcing time (t_{ar}) resulting in a reignition. The value t_{ar} can generally be considered as the longest arcing time, $t_{a\ max}$, less one half-cycle. The applicable maximum chopping number is thus:

$$\lambda_{max\ r} = A + Bt_{ar} + 2\ S_e \qquad \text{(F.11)}$$

This value is then used in equations (F.6) or (F.7) to derive the actual value of $k_{b\ max\ r}$ or $k_{a\ max\ r}$. Finally, $k_{p\ max}$ and $k_{s\ max}$ are derived using equations (F.9) and (F.10), respectively.

F.2.4 Evaluation of recovery voltage stress across circuit-breaker

The maximum recovery voltage across the circuit-breaker ($k_{r\ max}$) in per unit value is given by the following:

- for solidly earthed reactors:

$$k_{r\ max} = 1 + k_{a\ max} \qquad \text{(F.12)}$$

- for unearthed reactors:

$$k_{r\ max} = 2 + k_{a\ max} = 1{,}5 + k_{b\ max} \qquad \text{(F.13)}$$

- for neutral reactor earthed reactors:

$$k_{r\,max} = 1 + 2\,\kappa + k_{a\,max} \qquad \text{(F.14)}$$

F.3 Case studies

The case studies are based on laboratory tests carried out on a single interrupter of an SF_6 circuit-breaker in a single-phase test with 101 A at 175 kV and 60 Hz (refer to Figure 8). The tests were performed as follows: 38 tests with point-on-wave settings increased by 18 electrical degrees per test supplemented by a test series of 18 tests with settings in the range giving maximum and minimum arcing times. The tests are analyzed as described in F.2 and are then applied to predict performance in a field installation with and without overvoltage limitation measures applied. The values of C_s and C_L were 30 nF and 2,1 nF, respectively.

The test interrupter had no grading capacitor. The chopped current values were not measured, but are derived using Equation (F.2) where k_a is the measured suppression peak-voltage value. The chopping numbers are then calculated using Equation (F.1). The results of the calculation are given in Table F.1.

Table F.1 – Single interrupter laboratory test values

t_a ms	k_a p.u.	i_{ch} A	λ $AF^{-0,5}$
8,2	1,36	4,98	112 488
7,3	1,18	3,38	76 347
6,6	1,15	3,07	69 345
5,8	1,11	2,6	58 729
5	1,07	2,06	46 531
4,2	1,03	1,33	30 042
11,7	1,6	6,74	152 243
10,9	1,44	5,6	126 493
10	1,31	4,57	103 227
9,3	1,4	5029	119 491
8,7	1,3	4,49	101 420
7,8	1,23	3,87	87 416
7	1,22	3,77	85 157
6,1	1,09	2,34	52 856
5,6	1,13	2,84	64 150
4,4	1,07	2,06	46 531
10,6	1,25	4,05	91 481
10,3	1,47	5,82	131 462
9,6	1,29	4,4	99 387
8,3	1,32	4,65	105 034
5,3	1,07	2,06	46 531
5,2	1,15	3,07	69 345
5,2	1,07	2,06	46 531
5,2	1,05	1,73	39 077
6,1	1,09	2,34	52 856
5	1,09	2,34	52 856
5,5	1,09	2,34	52 856
5,5	1,06	1,9	42 918
5,8	1,14	2,96	66 860
5,5	1,11	2,6	58 729
5,6	1,1	2,47	55 792
5,8	1,12	2,72	61 439
4,8	1,03	1,33	30 042
4,8	1,12	2,72	61 439
4,8	1,06	1,9	42 917
4,8	1,13	2,84	64 150
4,8	1,01	0,77	17 393
4,9	1,06	1,9	42 917

The derived chopping numbers are plotted against arcing time in Figure F.1. A linear regression analysis, using the equations given in Appendix G or a computer spreadsheet program, gives the following expression:

λ_{mean} = 13 744 t_a – 21 028

S_e = 12 167

This result is applied to predict the performance of a circuit-breaker with two interrupters applied at 550 kV to switch out a 525 kV, 135 Mvar shunt reactor. Performance is considered first for the solidly earthed case without overvoltage limitation measures applied, secondly with a surge arrester applied across the circuit-breaker and finally, with controlled opening applied.

Performance is then considered in a similar manner for the case where the neutral is earthed through a 1 600 Ω neutral reactor.

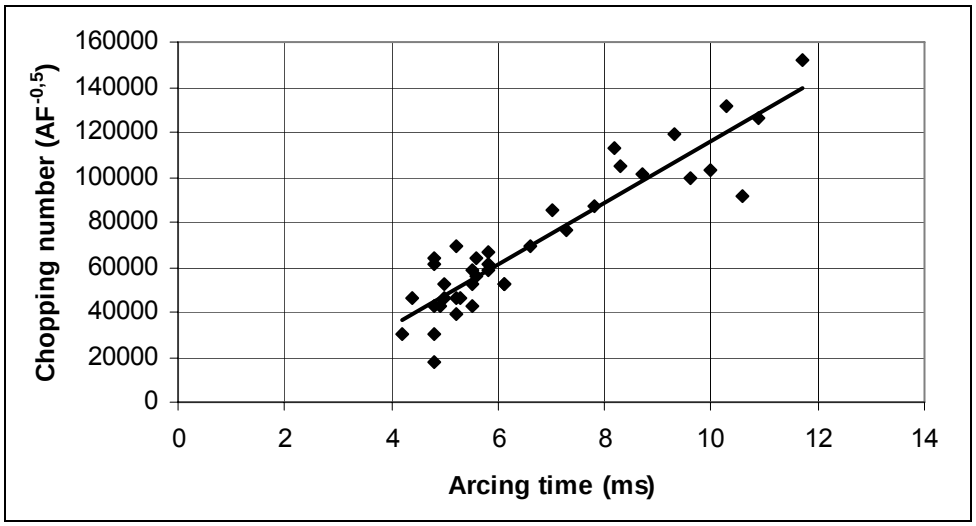


Figure F.1 – Chopping number as function of arcing time in laboratory test

Case 1: Solidly earthed shunt reactor

Option 1.1: Without overvoltage limitation measures applied

The maximum chopping overvoltage will occur at the maximum arcing time. The maximum arcing time in the laboratory test was 11,7 ms at 60 Hz. From Equation (F.5):

λ_{max} = 13 744 t_a – 21 028 + 2 × 12 167

= 16,4 × 10^4

Using Equation (F.7) (with N = 2):

$$k_{a\,max} = \sqrt{1+\frac{3\times 2(16{,}4\times 10^4)^2}{2\times 377\times 135\times 10^6}} = 1{,}6 \text{ p.u.}$$

giving: $k_{r\,max}$ = 1 + 1,6 = 2,6 p.u.

To calculate the magnitude of the reignition overvoltages, the maximum chopping number with reignitions is calculated from Equation (F.11):

$\lambda_{max\ r}$ = 13 744 (11,7 – 8,33) + 21 028 + 2 × 12 167

$\lambda_{max\ r}$ = 4,96 × 10^4

and from Equation (F.7):

$k_{a\ max\ r}$ = 1,07 p.u.

Using equations (F.9) and (F.10):

$k_{p\ max}$ = 1 + 0,5 (1 + 1,07) = 2,04 p.u.

$k_{s\ max}$ = (1 + 0,5) (1 + 1,071) = 3,11 p.u.

Option 1.2: Metal oxide surge arrester applied across the circuit-breaker

The surge arrester is taken to have a protective level k_{arv} equal to 1,6 p.u. (refer to 9.2.5). The effect of the surge arrester on the circuit-breaker is to limit the reignition voltage and tends to reduce the arcing time. The maximum arcing time will thus be 11,7 ms or less.

Therefore:

$k_{a\ max}$ ≤ 1,6 p.u.

$k_{r\ max}$ = 1,6 p.u.

$k_{p\ max}$ ≤ 1 + 0,5 x 1,6 ≤ 1,8 p.u.

$k_{s\ max}$ ≤ 1,6 (1 + 0,5) ≤ 2,4 p.u.

Option 1.3: Controlled opening applied to the circuit-breaker

With controlled opening applied to the circuit-breaker, the maximum chopping overvoltage is determined by the arcing time setting of the synchronizer to give no reignitions. A setting at 7 ms arcing time should allow some variation in opening time since the maximum arcing time with reignitions at the first current zero was 3,4 ms in the laboratory tests. Again, from Equation (F.7):

λ_{max} = 13 744 × 7 – 21 028 + 2 × 12 167 = 9,95 x 10^4

$k_{a\ max}$ = 1,26 p.u.

giving: $k_{r\ max}$ = 2,26 p.u.

$k_{p\ max}$ = 0 p.u.

$k_{s\ max}$ = 0 p.u.

Case 2: Neutral reactor earthed shunt reactor

The λ_{max} values from the laboratory tests can be used, i.e. the same as in case 1.

To take into account that the energy oscillates around a voltage of κ p.u. of opposite polarity, the amplitude, k_b, of this oscillation is calculated using Equation (F.6) with C_t/C_L = 1, i.e. C_S >> C_L.

The inductance of the neutral reactor L_N is 4,24 H, L being 5,43 H giving κ = 0.3 (refer to 1.2.2).

Option 2.1: Without overvoltage limitation measures applied

From Equation (F.6):

$$k_{\mathrm{b\,max}} = 1{,}3\sqrt{1+\frac{2\times\left(16{,}4\times10^{4}\right)^{2}\times5{,}43}{\left(428\times10^{3}\right)^{2}\times1{,}3}} = 1{,}94 \text{ p.u.}$$

giving: $k_{\mathrm{a\,max}}$ = 1,64 p.u.

$k_{\mathrm{c\,max}}$ = 2,24 p.u.

$k_{\mathrm{r\,max}}$ = 3,24 p.u.

From Equation (F.6):

$k_{\mathrm{b\,max\,r}}$ = 1,37 p.u.

From Equations (F.9) and (F.10):

$k_{\mathrm{p\,max}}$ = 1 + 0,5 (1 + 0,3 + 1,37) = 2,33 p.u.

$k_{\mathrm{s\,max}}$ = (1 + 0,5) (1 + 0,3 + 1,37) = 4,0 p.u.

Option 2.2: Metal oxide surge arrester applied across the circuit-breaker

The surge arrester is identical to that applied in option 1.2 above.

$k_{\mathrm{a\,max}} \leq$ 1,64 p.u.

$k_{\mathrm{r\,max}}$ = 1,6 p.u.

$k_{\mathrm{c\,max}} \leq$ 0,6 p.u.

$k_{\mathrm{p\,max}} \leq$ 1,8 p.u.

$k_{\mathrm{s\,max}} \leq$ 2,4 p.u.

Option 2.3: Controlled opening applied to the circuit-breaker

$$k_{\mathrm{b\,max}} = 1{,}3\sqrt{1+\frac{2\times\left(9{,}95\times10^{4}\right)^{2}\times5.43}{\left(428\times10^{3}\right)^{2}\times1{,}3}} = 1{,}57$$

giving: $k_{\mathrm{a\,max}}$ = 1,27 p.u.

$k_{\mathrm{c\,max}}$ = 1,87 p.u.

$k_{\mathrm{r\,max}}$ = 2,87 p.u.

$k_{\mathrm{p\,max}}$ = 0 p.u.

$k_{\mathrm{s\,max}}$ = 0 p.u.

Case 1 overvoltage predictions are summarized in Table F.2.

Table F.2 – Case 1 predicted overvoltage values

Option	Overvoltage p.u.			
	$k_{a\ max}$	$k_{r\ max}$	$k_{p\ max}$	$k_{s\ max}$
1.1	1,6	2,6	2,04	3,11
1.2	≤ 1,6	1,6	≤ 1,8	≤ 2,4
1.3	1,26	2,26	0	0

Reference 1 states that Table 2a of IEC 60094 (same as Table 2a of IEC 62271-1) is applicable to EHV circuit-breakers used for shunt reactor switching. The switching surge capability across the circuit-breaker is thus 3,15 p.u. (900 kV + 450 kV). Taking the position that the maximum allowable chopping overvoltage across the circuit-breaker shall not exceed 80% of the switching surge withstand capability i.e. 2,52 p.u., the following can be concluded:

a) Overvoltage limitation measures are essential for the application of the proposed circuit-breaker;

   The relative merit of applying options 1.2 and 1.3 is evident, both in terms of impact on the circuit-breaker and the shunt reactor, respectively.

Case 2 overvoltage predictions are summarized in Table F.3.

Table F.3 – Case 2 predicted overvoltage values

Option	Overvoltage p.u.				
	$k_{a\ max}$	$k_{c\ max}$	$k_{r\ max}$	$k_{p\ max}$	$k_{s\ max}$
2.1	1,64	2,24	3,24	2,33	4,0
2.2	≤ 1,64	≤ 0,6	1,6	≤ 1,8	≤ 2,4
2.3	1,27	1,87	2,87	0	0

Applying the same 2,52 p.u. maximum allowable voltage across the circuit-breaker, the following can be concluded:

   The circuit-breaker cannot be applied without some form of overvoltage limitation;

a) Option 2.2 can be applied without any further measures;

b) Option 2.3 can only be applied if the neutral reactor is by-passed prior to opening the circuit-breaker, i.e. switching duty becomes identical to case 1, option 1.3.

Appendix G
Statistical equations for derivation of chopping and reignition overvoltages

G.1 General

The purpose of this annex is to provide, for convenience, the statistical equations used in the derivation of chopping and reignition overvoltages.

G.2 Chopping number independent of arcing time

With reference to Equation (F.4):

$$\lambda_{\text{mean}} = \frac{1}{n}\sum_{i=1}^{n}\lambda_{\text{i}} \qquad \text{(G.1)}$$

and

$$\sigma^2 = \frac{n\sum_{i=1}^{n}\lambda_{\text{i}}^2 - \left(\sum_{i=1}^{n}\lambda_{\text{i}}\right)^2}{n(n-1)} \qquad \text{(G.2)}$$

where

n is the number of test shots;

λ_{i} chopping number corresponding to the i^{th} test shot.

G.3 Chopping number dependent on arcing time

Calculate values for S_{xx}, S_{yy} and S_{xy} as follows:

$$S_{\text{xx}} = n\sum_{i=1}^{n}t_{\text{ai}}^2 - \left(\sum_{i=1}^{n}t_{\text{ai}}\right)^2$$

$$S_{\text{yy}} = n\sum_{i=1}^{n}\lambda_{\text{i}}^2 - \left(\sum_{i=1}^{n}\lambda_{\text{i}}\right)^2$$

$$S_{\text{xy}} = n\sum_{i=1}^{n}t_{\text{ai}}\lambda_{\text{i}} - \left(\sum_{i=1}^{n}t_{\text{ai}}\right)\left(\sum_{i=1}^{n}\lambda_{\text{i}}\right)$$

where n and λ_{i} are as noted above and t_{ai} is the arcing time corresponding to the i^{th} test shot.

With reference to Equation (F.8):

$$B = \frac{S_{xy}}{S_{xx}} \tag{G.3}$$

$$A = \frac{1}{n}\sum_{i=1}^{n} \lambda_i - \frac{B}{n}\sum_{i=1}^{n} t_{ai} \tag{G.4}$$

$$S_e^2 = \frac{1}{n(n-2)}\left(S_{yy} - B^2 S_{xx}\right) \tag{G.5}$$

10 Synthetic testing, synthetic making tests

10.1 Synthetic testing

10.1.1 Introduction

With the increasing voltage and current ratings of recently developed circuit-breakers, the total available short-circuit power of a high power laboratory has to be increased accordingly. The investments required to increase the short-circuit power are very high. In order to still be able to perform the correct type tests on circuit-breakers with the available short-circuit power, one possibility is open: performing synthetic tests.

Requirements for synthetic testing and examples of synthetic circuits are given in IEC 62271-101 [1].

A synthetic test circuit consists of separate high-current and high-voltage circuits (see Figure 56). During the short-circuit period, the short-circuit current will be fed from a short-circuit generator at a limited voltage. The voltage should have an amplitude of sufficient magnitude to prevent the arc voltage from influencing the short-circuit current.

When the current is interrupted, the high voltage circuit will give the correct voltage stresses across the contact gap.

The principle used for the making operation is similar. The high-voltage circuit first provides the correct voltage stress during the closing operation and as soon as the prearcing occurs, the high current circuit will then provide the correct short-circuit current.

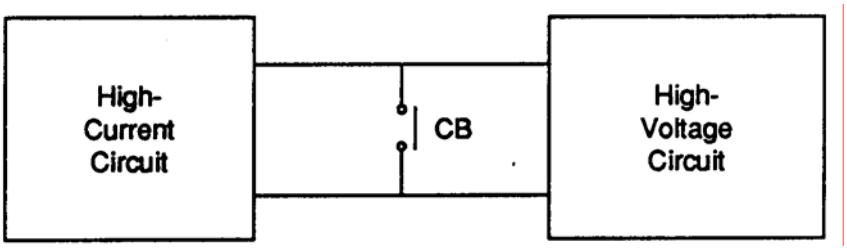


Figure 56 - Principle of synthetic testing

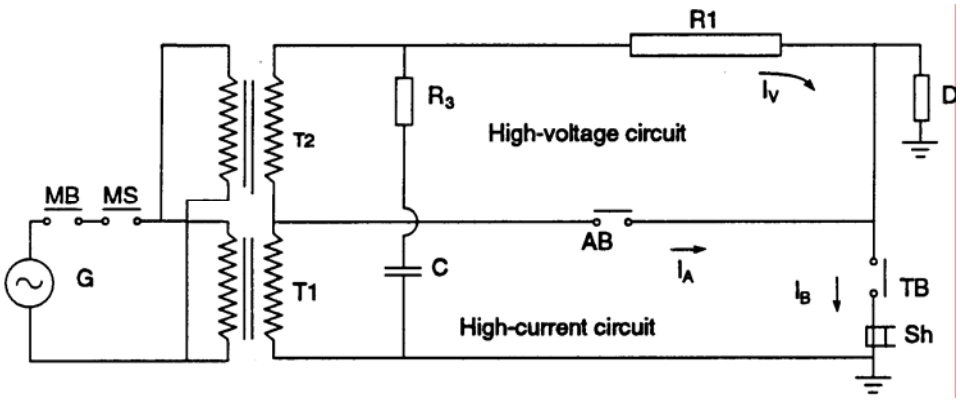
In order for the synthetic test to be valid, the following requirements shall be met:

- the arc energy in the contact gap shall be equal to that of a direct test;
- the di/dt at current zero shall be in accordance with the current and frequency specified;
- the recovery voltage shall appear immediately after current zero i.e. without delay;
- the TRV shall be at least equal to or exceeding the required TRV;
- the voltage source shall have a sufficient power to avoid excess damping of the transient process by the post arc current.

Synthetic testing allows in general testing at one particular arcing time per operation. In order to cover the full extinguishing window, it may be necessary to use reignition circuits.

10.1.2 Transformer method

The circuit for the transformer method also known as a Skeats circuit or duplicate circuit consists of two transformers and some additional equipment such as an auxiliary circuit-breaker. A schematic diagram of the test circuit including the TRV controlling components is given in Figure 57.



Key

D	voltage divider	T_2	high voltage transformer
AB	auxiliary circuit-breaker	R_3, C	oscillatory circuit for the control of the TRV
G	short-circuit generator	R_1	current limiting resistor
MB	master circuit-breaker	TB	test circuit-breaker
MS	making switch	Sh	current measuring shunt
T_1	short-circuit transformer		

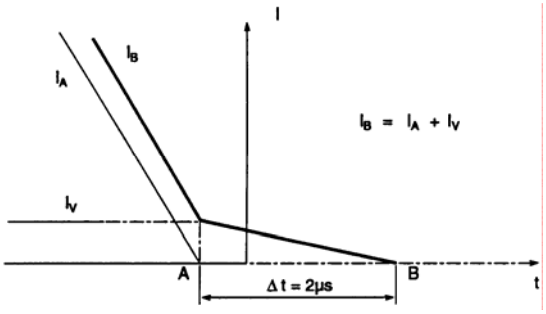
Figure 57 - Duplicate circuit

The current through the test circuit-breaker consists of the currents I_A and I_V. The small and resistive current I_V (in the high-voltage circuit) will delay the current zero through the test circuit-breaker (see Figure 58). The current I_V will be forced to zero by the arc voltage with a time constant given by

$$\Delta t = \frac{L_V}{R_V}$$

A resistor with a high resistance value will give a short time constant, but may damp the TRV. The best solution is a voltage dependent resistor.

When performing an interruption test in this circuit, both auxiliary and test circuit-breaker will operate at the same current zero.

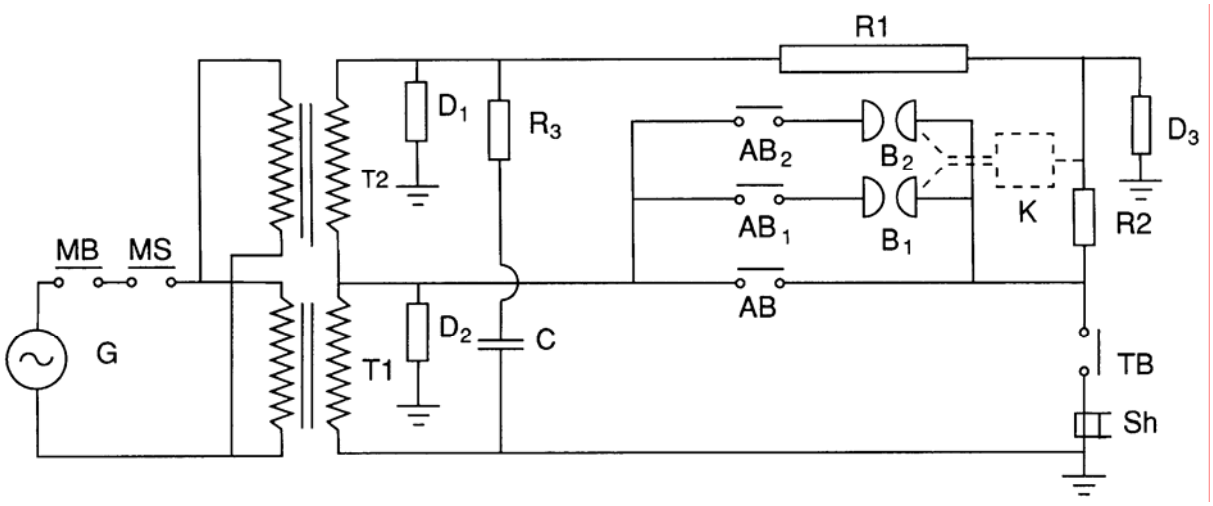


I_A	current in the high-current circuit
I_V	current in the high-voltage circuit
I_B	current through the test circuit-breaker
A	interruption of the auxiliary circuit-breaker
B	interruption of the test circuit-breaker

Figure 58 - Currents in the duplicate circuit around current zero

During the short-circuit and arcing interval the current is fed from the short-circuit generator through the test circuit-breaker via the auxiliary circuit-breaker. The auxiliary circuit-breaker interrupts at a time A in Figure 58 and when the test circuit-breaker interrupts at time B, the TRV from the high-voltage source will be applied across the test circuit-breaker.

In order to be able to test more than one current zero per test, the test circuit can be modified in accordance with Figure 59.



Key

AB_1 - B_1, AB_2 - B_2	multi-loop reignition circuits
AB	auxiliary circuit-breaker
K	control unit for the spark gaps B_1 and B_2
D_1, D_2, D_3	voltage dividers
R_2	resistor

Figure 59 - Duplicate circuit with multi-loop reignition circuits

The circuit works as follows (for interruption): At the start of the test all auxiliary circuit-breakers (AB) as well as the test circuit-breaker (TB) are closed. At the first tested current zero AB and TB will operate. If TB fails to interrupt, a small resistive current starts to flow in the high-voltage circuit, building up a voltage across R_2. This voltage is used to trigger the multi-loop reignition spark gap B_1 causing the short-circuit current to start to flow through AB_1 and TB. Half a cycle after the first tested current zero, the TB gets another chance to interrupt. Should the TB also fail to interrupt at this current zero, spark gap B_2 can be triggered giving the test circuit-breaker a third chance.

NOTE - The multi-loop reignition circuit can also be used to give a test circuit-breaker the correct stresses during a closing operation. A close-open test starts with TB and AB in the open position and AB_1 and AB_2 in the closed positions. In this case the test circuit-breaker is closed against the correct voltage. When the pre-arc starts in the TB, spark gap B_1 is triggered by the voltage drop across the resistor R_2 and the short-circuit current starts to flow. For practical reasons AB is always closed after B_1 and B_2 are triggered (to avoid excess burning of the spark gaps).

Summarizing, the duplicate circuit has the following advantages:

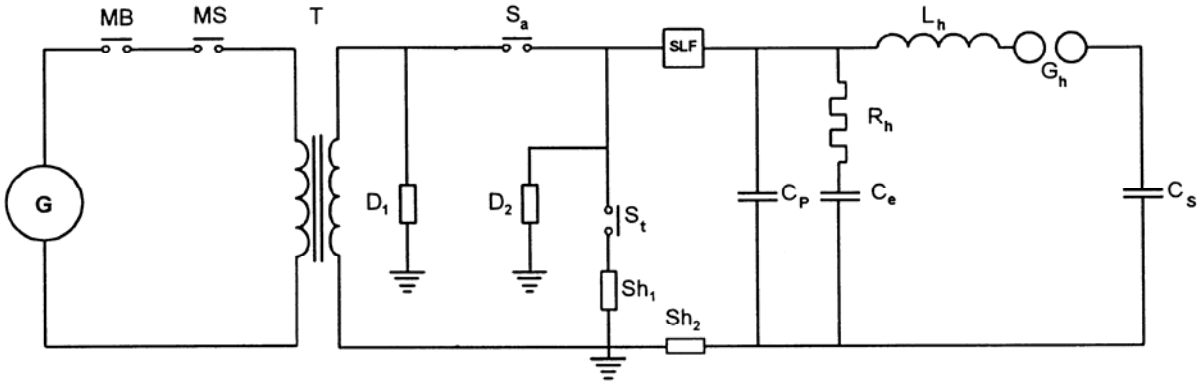
- more than one current zero can be tested per test;
- gives correct stresses at a closing operation.

A negative point of this circuit is, that it does not give the correct thermal stresses at the time of interruption. For tests where attention has to be paid to the thermal failure mode (e.g. short-line fault), the circuit is not valid. Interruption tests can therefore only be performed on oil circuit-breakers, since they are insensitive to thermal stresses.

10.1.3 Current injection method

The current injection method is the preferred method in accordance with IEC 62271-101.

The test circuit is built up with one high-current circuit and one high-voltage circuit. A diagram of the test circuit is given in Figure 60.



Key

G	generator	C_s	capacitor bank supplying injected current
MB	master circuit-breaker	C_p, C_e	capacitor controlling TRV characteristic
MS	making switch	R_h	resistor controlling TRV characteristic
T	transformer	G_h	spark gap of high-voltage circuit
S_a	auxiliary circuit-breaker	L_h	inductance of high-voltage circuit
S_t	test circuit-breaker	$D_{1, 2}$	voltage divider
SLF	artificial line	$Sh_{1, 2}$	low-ohmic shunt

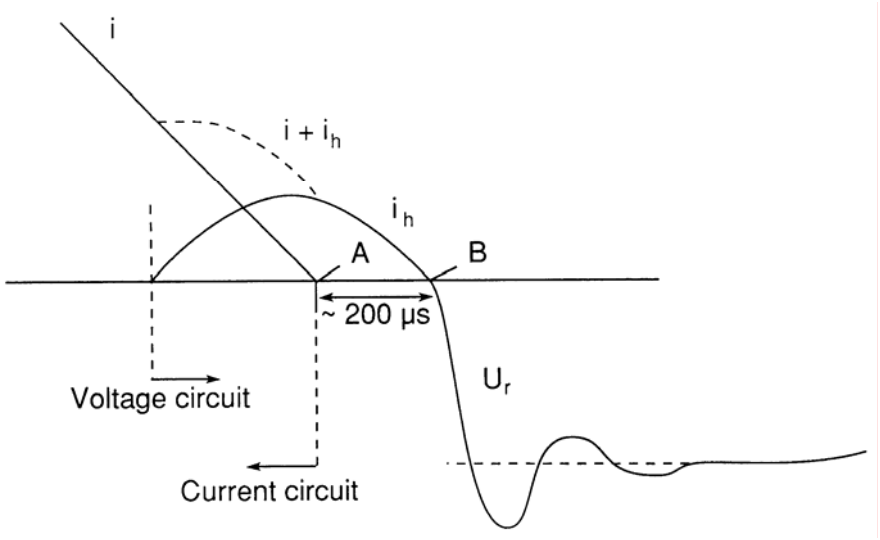
Figure 60 - Current injection circuit

In the current injection circuit the high-voltage circuit consists of a charged capacitor C_s, a spark gap G_h and an oscillatory circuit (consisting of L_h, R_h C_e and C_p).

When the spark gap is triggered, a discharge current will flow from the charged capacitor C_s via the inductance L_h through the test circuit-breaker. The spark gap is triggered just before the current zero at which the circuit-breaker is tested, see Figure 61. When the circuit-breaker has interrupted, the TRV will be determined by the oscillatory circuit.

The current through the test circuit-breaker consists of a contribution from the high current circuit (i) and the high-voltage (current injection) circuit (i_h), hence the total current through the test circuit-breaker is $i + i_h$. As can be seen in Figure 61, the high-current and high-voltage circuits are overlapping each other.

The auxiliary circuit-breaker interrupts at time A. At time B the total current is interrupted by the test circuit-breaker and the recovery voltage starts to rise with parameters u_c and t_3, i.e. a two parameter TRV. When the transitory part of the recovery voltage is damped out, the recovery voltage stays at a d.c. level (determined by the amplitude factor of the circuit).

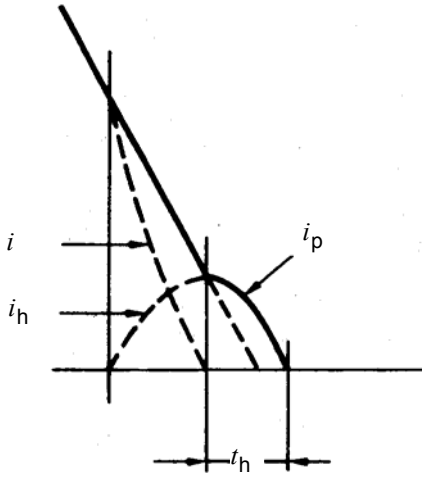


i	current in the high-current circuit
i_h	current from the current injection circuit
$i + i_h$	total current through the test circuit-breaker
U_r	recovery voltage
A	interruption of the auxiliary circuit-breaker
B	interruption of the test circuit-breaker

Figure 61 - Currents and voltages associated with the current injection method

The test is valid if di/dt is equal to the value associated with the power frequency (50 or 60 Hz) and if the shape of the TRV is not less severe than the specified TRV.

The timing of the current injection is described in IEC 62271-101. The requirement is that the main current zero (A in Figure 61) shall occur between the peak and the first current zero of the injected current (B in Figure 61). The maximum allowable time between the main current zero and the current zero of the injected current is 500 µs. The shortest time interval between the main current zero and the current zero of the injected current should be 200 µs in order not to overstress the circuit-breaker (the di/dt of the current to be interrupted may then be too high for the circuit-breaker). The limits of the injection timing for the circuit described in Figure 60 are given in Figure 62.



$t_h \leq ¼\ T_h$, where T_h is the duration of one period of injected current

$t_h \leq 500\ \mu s$

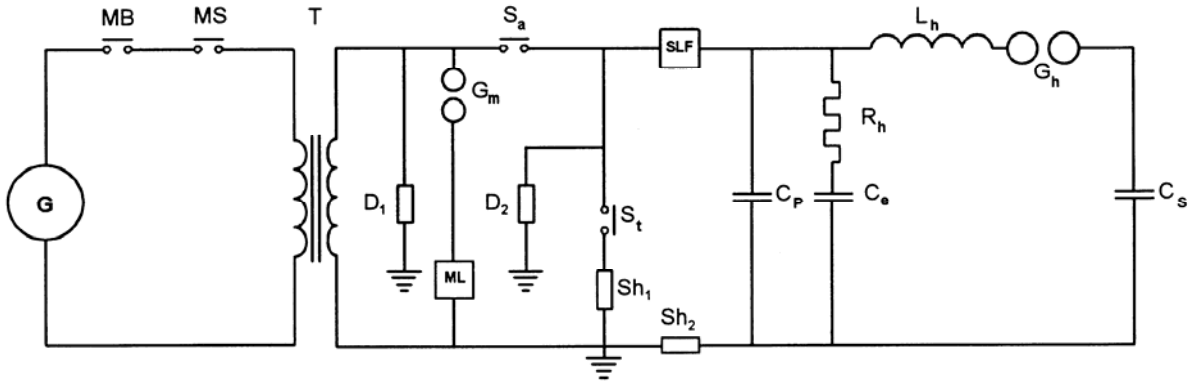
i	current in the auxiliary circuit-breaker
i_h	injected current
i_p	current in test circuit-breaker
T_h	duration of one period of injected current
t_h	time during which the arc is fed only by the injected current

Figure 62 – Timing of current injection for the circuit in Figure 60

The circuit-response is measured by a current impulse injection. The capacitor C_s is charged to a voltage of approximately 100 V and the spark gap is triggered. The current is interrupted by an ideal circuit-breaker (diode) and the voltage response is measured.

When testing the test circuit-breaker, the arcing time has to be predetermined. When testing arcing times longer than around 12 ms, use is made of multi-loop reignition circuits (see Figure 63).

The multi-loop reignition circuit (ML) is built up by charged capacitors and a spark gap and it produces a rapid change of di/dt close to a current zero, preventing the test circuit-breaker from interrupting too early at current source voltage only.



G	generator	C_s	capacitor bank supplying injected current
MB	master circuit-breaker	C_p, C_e	capacitor controlling TRV characteristic
MS	making switch	R_h	resistor controlling TRV characteristic
T	transformer	G_h	spark gap of high-voltage circuit
S_a	auxiliary circuit-breaker	L_h	inductance of high-voltage circuit
S_t	test circuit-breaker	$D_{1, 2}$	voltage divider
G_m, ML	multi-loop reignition circuit	$Sh_{1, 2}$	low-ohmic shunt
SLF	artificial line		

Figure 63 - Current injection circuit with multi-loop reignition circuit

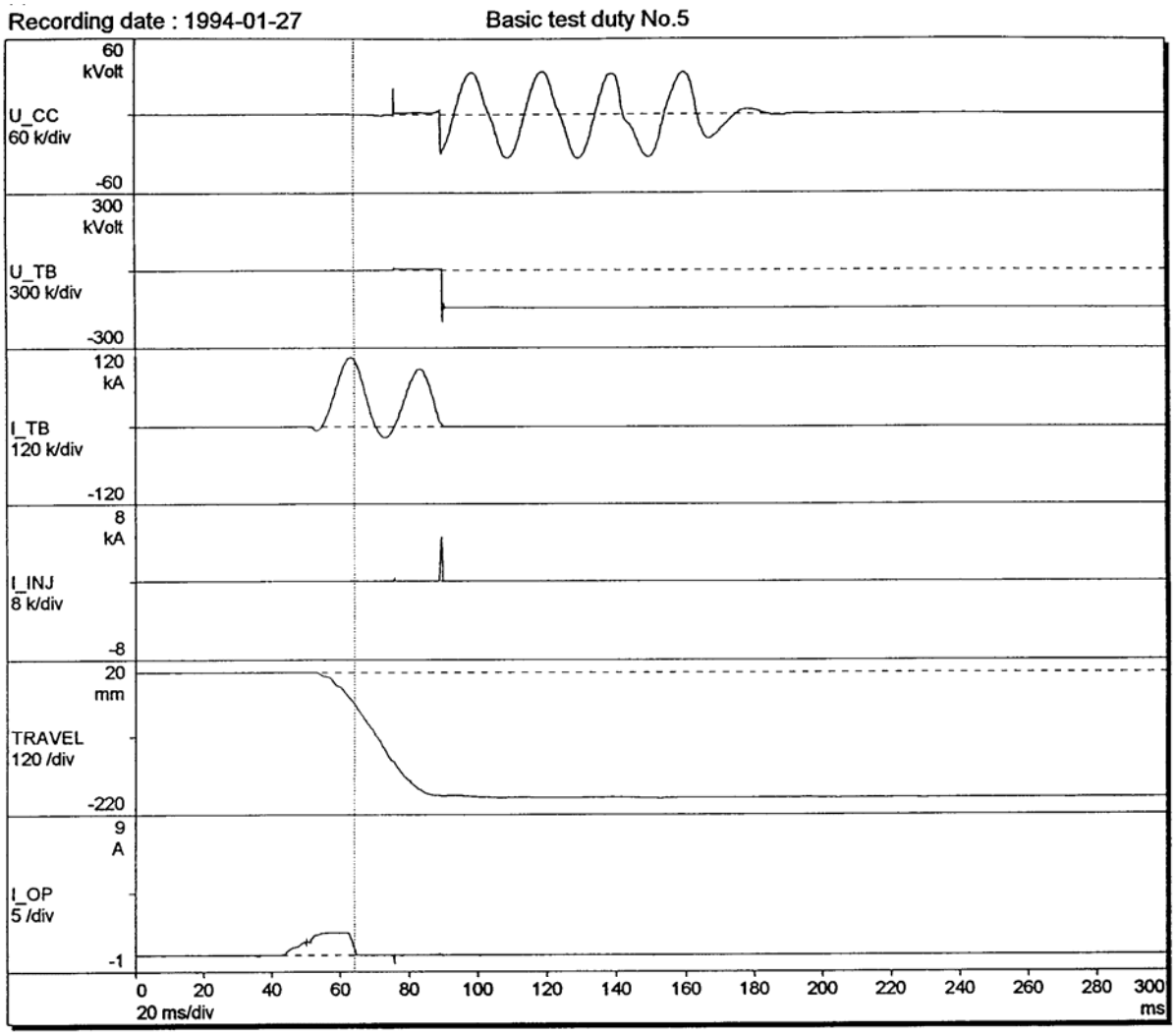
Four periods can be defined around current zero:

- high current interval;
- period of strong interaction;
- dielectric recovery;
- period of stationary stresses.

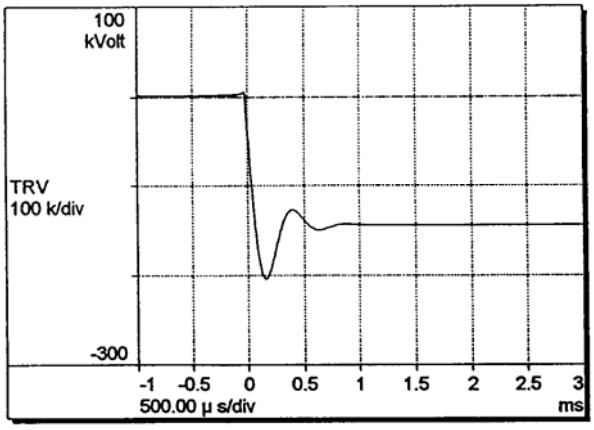
When studying the four periods, the stresses are equal to those obtained at a direct test, except for the period of stationary stresses, where the d.c. recovery voltage makes it more severe for the test circuit-breaker.

When interrupting an asymmetrical current, the current zero and voltage peak do not coincide as in the symmetrical case. This will affect the TRV peak value (will be lower). Furthermore, the di/dt at current zero is different (lower) from the symmetrical case, which will affect the rise of recovery voltage. Both IEC and ANSI/IEEE state derating factors for the TRV and di/dt when performing interrupting tests with asymmetrical current. The derating factors are dependent on the degree of asymmetry at current zero which in its turn is dependent on the time constant of the network (45 ms) and the arcing time.

Figure 64 gives an example of a recording from a test using the current injection circuit.



Record number : 00644450			
Breaking Current a.c. Component	I	41.4	kA
Breaking Current d.c. Component	I d.c.	46.0	kA
Percentage d.c. Component	% d.c	78.7	%
Time of Injected Current Only	Th	557.4	µs
Injection Current Peak	I inj	4.6	kA
Source Voltage RMS	U	23.7	kV
Recovery Voltage DC (Tp/8)	U d.c.	144.8	kV
TRV Peak Voltage	Uc	204.6	kV
Amplitude Factor	AF	1.41	----
Arcing Time	Ta	25.8	ms
Break-time	Tb	46.6	ms
Opening Time	To	20.8	ms
Speed	VB	7.9	m/s
Contact Travel	D	195.4	mm



U_CC source voltage (D_1)

U_TB transient recovery voltage (D_2)

I_TB current through test circuit-breaker (Sh_1)

I_INJ injected current (Sh_2)

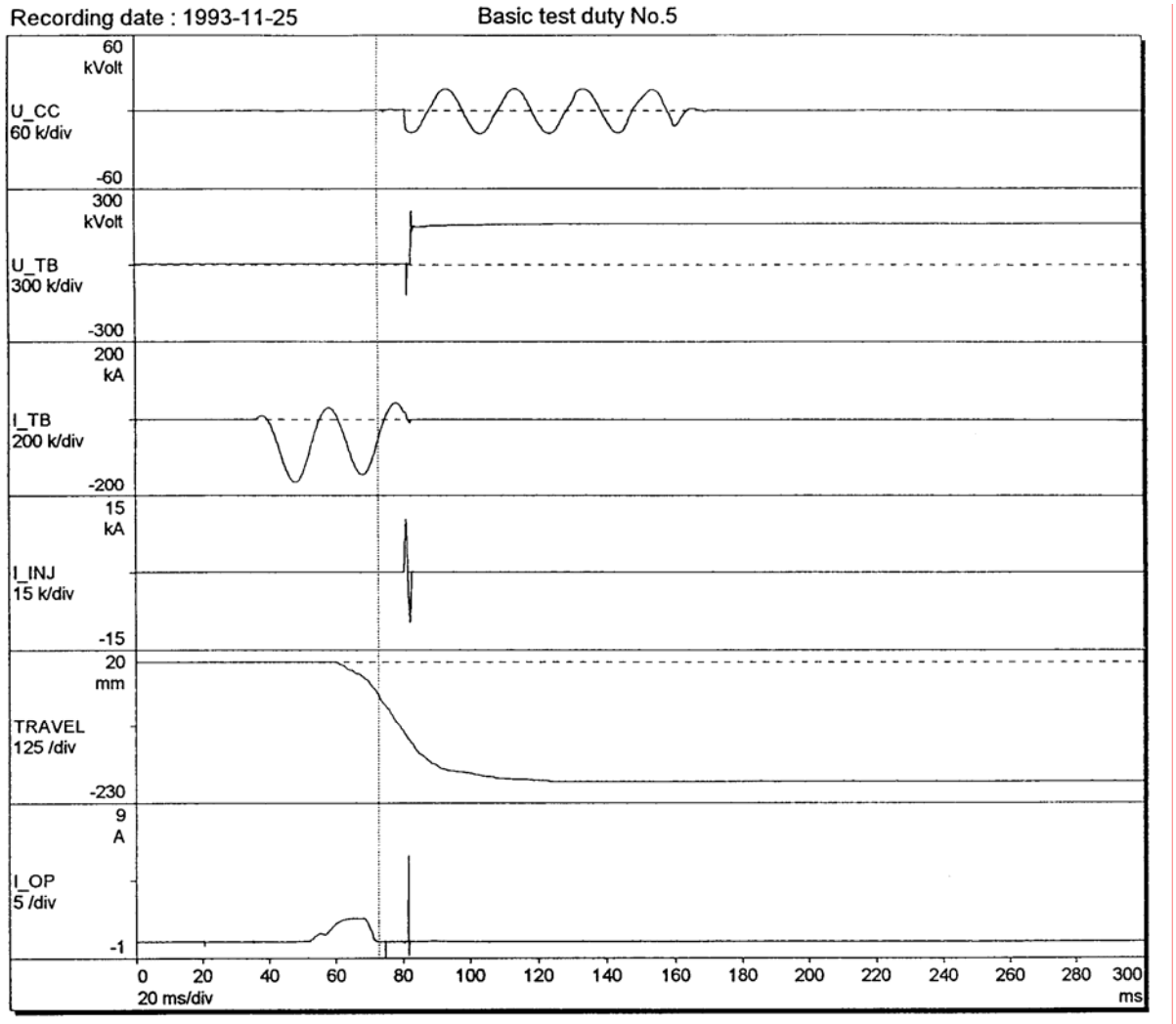
TRAVEL contact travel

I_OP current through opening coil

Figure 64 - Oscillograms from a short-circuit current breaking test using the current injection circuit

If the test circuit-breaker should fail to interrupt, only the injected current from the high-voltage circuit will continue to flow through the test circuit-breaker, since the auxiliary circuit-breaker has interrupted the short-circuit current. The energy associated with the injected current is not high enough to destruct the test circuit-breaker. The cause of the failure can be determined when inspecting the circuit-breaker, since no evidence has been destroyed.

A dielectric failure may look like the example given in Figure 65.



Record number : 00644039			
Breaking Current a.c. Component	I	64.2	kA
Breaking Current d.c. Component	I d.c.	51.0	kA
Percentage d.c. Component	% d.c	56.2	%
Time of Injected Current Only	Th	306.3	µs
Injection Current Peak	I inj	10.4	kA
Source Voltage RMS	U	12.3	kV
Recovery Voltage DC (Tp/8)	U d.c.	--	kV
TRV Peak Voltage	Uc	--	kV
Amplitude Factor	AF	--	----
Arcing Time	Ta	8.9	ms
Break-time	Tb	29.7	ms
Opening Time	To	20.9	ms
Speed	VB	7.8	m/s
Contact Travel	D	195.3	mm

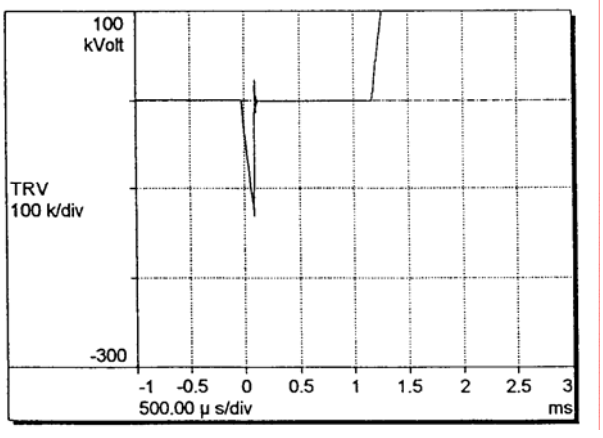


Figure 65 - Oscillogram showing a dielectric failure

An example of a thermal failure is given in Figure 66.

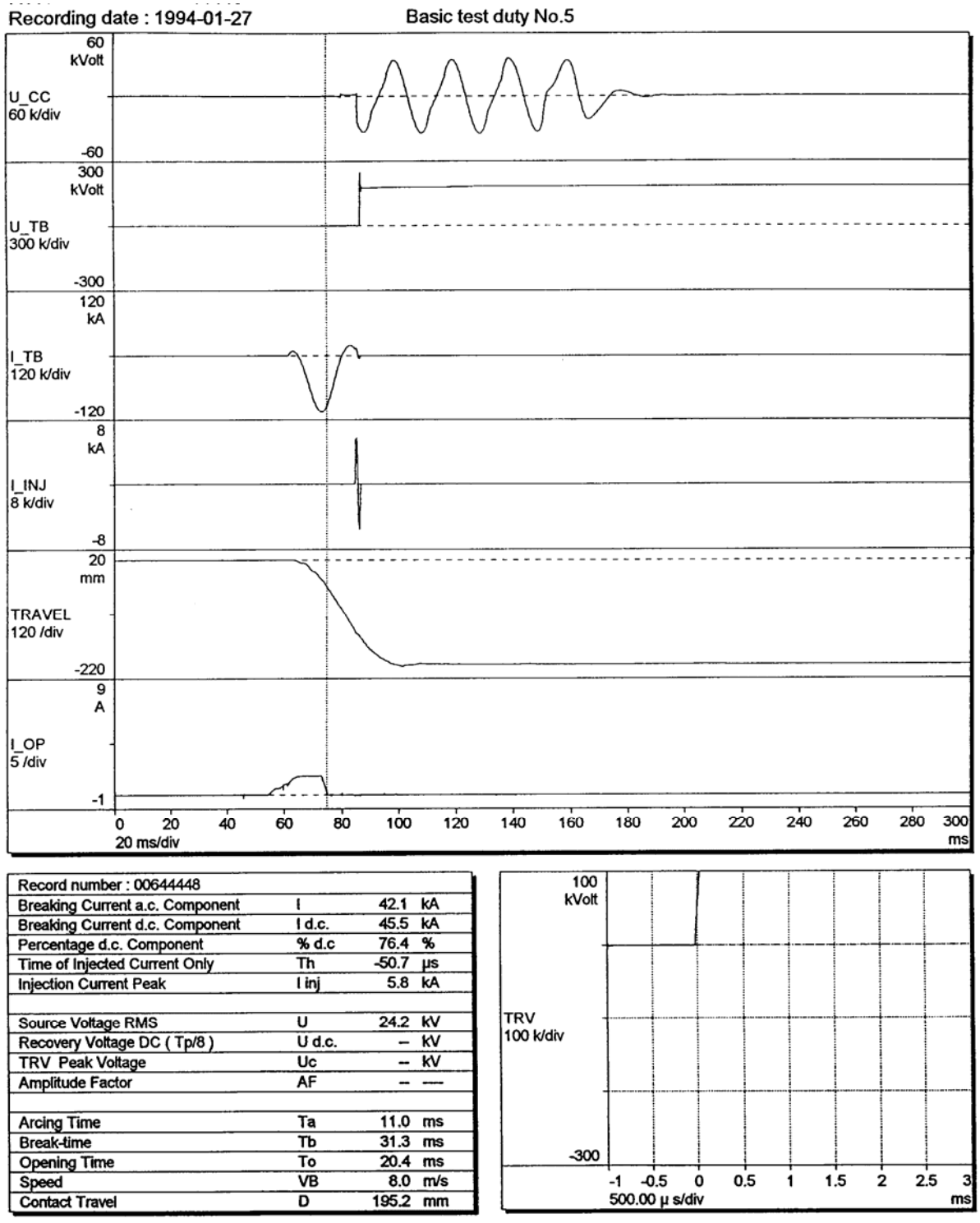


Figure 66 - Oscillogram showing a thermal failure

It takes some time to recharge and reset the high voltage circuit. If no two identical high voltage circuits are available, the auto-reclosing duty cycle (O - 0,3 s - CO) has to be performed in at least two steps:

1 one single opening operation with the correct stresses;

2 an O - 0,3 s - CO operation with current injection in the last opening operation. The first opening operation takes place at the voltage of the high current source only with the same arcing time as determined under 1. The closing operation takes place at the voltage of the high current source;

3 one closing operation shall be performed with the symmetrical short-circuit current and one closing operation shall be made at the correct applied voltage and the maximum making current available at that voltage (giving the correct prearcing).

NOTE The auxiliary circuit breaker and the test circuit-breaker shall be of the same type (air blast, oil or SF_6), otherwise the interaction of the test circuit-breaker with the test circuit in the critical interval around current zero will be disturbed by the behaviour of the auxiliary circuit-breaker.

In order to be able to test with a four parameter TRV, the high voltage circuit has to be extended with additional capacitors and inductances.

When performing unit tests on a circuit-breaker pole consisting of two series connected breaking units, it is common practice to use one breaking unit as test circuit-breaker and the other unit as an auxiliary circuit-breaker in the way as shown in Figure 67.

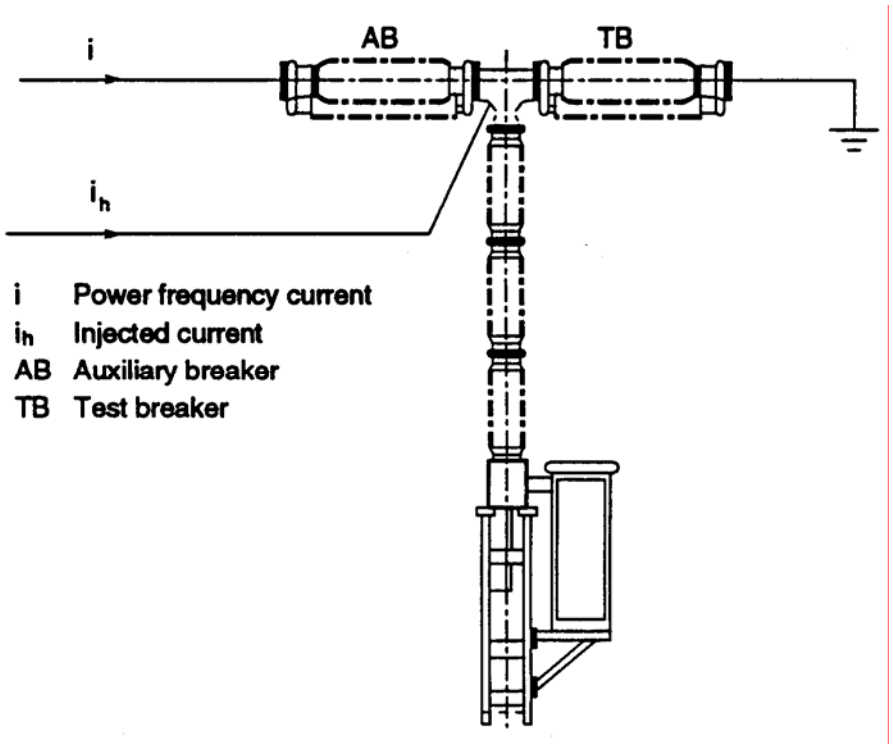


Figure 67 - Connection of a circuit-breaker pole consisting of two breaking units for unit testing

This arrangement has some advantages:

- both the test circuit-breaker and auxiliary circuit-breaker are of the same type;
- both breaking units are affected by the arcing and the operating mechanism will therefore be correctly stressed during opening and closing, hence no adjustment of the operation energy is needed.

Summarizing, the current injection method has the following advantages:

- non destructive, in the case of a circuit-breaker failure;
- testing can be performed at any frequency;
- the circuit is valid for all types of circuit-breakers.

Some features may be considered as negative. These are the following:

- only one current zero/test can be tested during a single operation;
- closing operations can only be performed at reduced voltage if the circuit is not completed with a circuit giving the correct stresses at closing.

10.1.4 Voltage injection method

Similar to the current injection method the test circuit consists of one high-current circuit and one high-voltage circuit. A diagram is given in Figure 68. As the high-voltage circuit is switched in after the short-circuit current interruption the high-current circuit provides the entire short circuit current for the test circuit-breaker TB and, also, after current zero, the first part of the transient recovery voltage (TRV). The oscillatory elements C_i and L_i are tuned to obtain correctly the rate-of-rise of the TRV during the first microseconds.

Test circuit-breaker and auxiliary circuit-breaker AB interrupt the current simultaneously. A capacitor C_h across the auxiliary circuit-breaker transmits the transient recovery voltage of the high-current circuit to the test circuit-breaker.

The high-voltage circuit, being in parallel to the auxiliary circuit-breaker, consists of a charged capacitor C_s and the oscillation circuit L_h C_h. The spark gap G_h is triggered by means of a voltage dependent control circuit c_m, vc with the measurement spark gap G_m. This switches in the high-voltage circuit in such a way that the specified TRV is continued and that there will be no delay between the current stress and the voltage stress (Figure 69). Thus, the voltage across the test circuit-breaker consists of the sum of two voltages, one being the power frequency recovery voltage of the source of the high current circuit and the other the injected voltage.

A multi-loop reignition circuit ML is used to test with long arcing times.

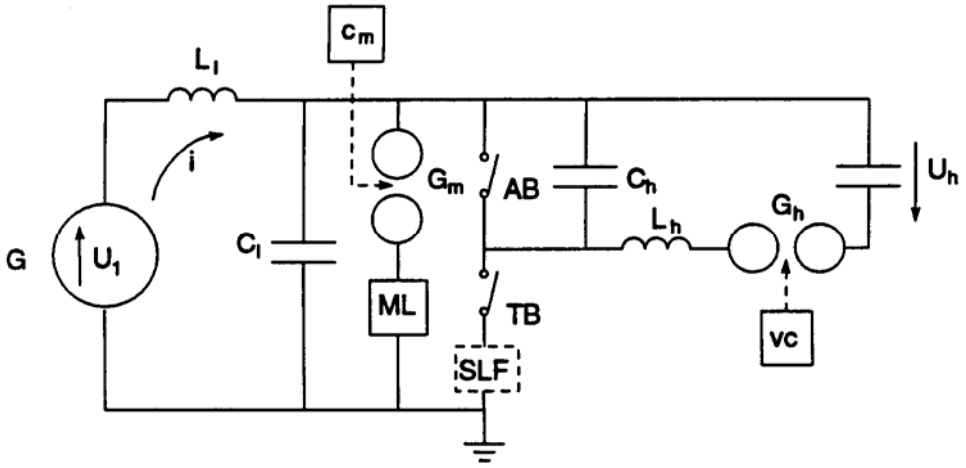
The conditions for testing duties with asymmetrical current and for performing the auto-reclosing duty cycle as well as to test with a four parameter TRV are the same as described for the current injection method. Also, it is strongly recommended to use an auxiliary circuit-breaker of the same or similar type as the test circuit-breaker.

Tests with the voltage injection method are non destructive as in case of a failure of the test circuit-breaker to interrupt only the current from the charged capacitor C_s flows through TB. The current of the high-current circuit must be of the rated power frequency.

The application of the voltage injection method is limited to test conditions in which dielectric failures (reignitions more than several 10s µs after current interruption) dominate and thermal failures (reignitions in the first few µs after current zero) do not occur. This makes the voltage injection method suitable for testing duties like terminal fault and out-of-phase. For these cases extensive investigations have proven the equivalence to direct testing and testing with the current injection method.

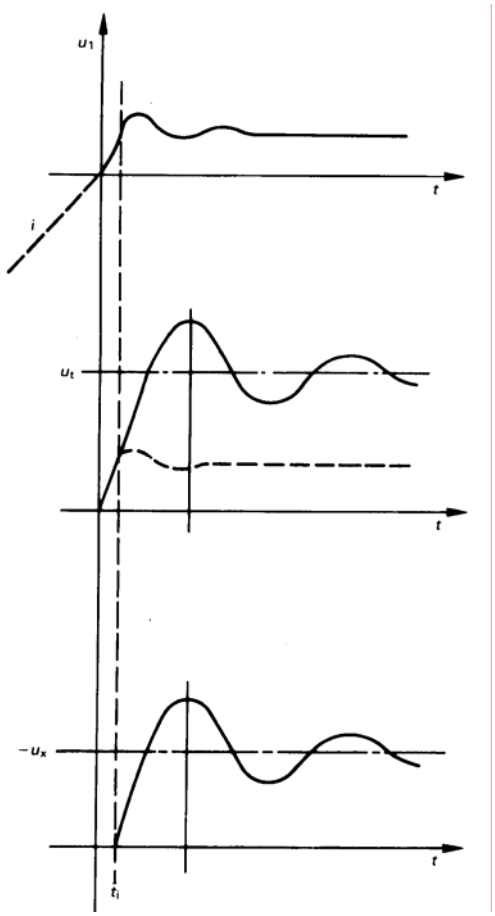
As the voltage injection method is not suited to simulate realistically the thermal phase of the recovery process, i.e. the phase immediately after current interruption, it should not be applied for tests under short-line fault conditions and for tests with ITRV.

The advantage of the voltage injection method is that a much smaller capacitor bank C_s can be used as it has to provide the TRV, only, and not an injection current. Therefore, it is often used to test circuit-breakers for very high rated voltages when the large capacitor bank of a current injection test circuit would be uneconomic.



G	short-circuit generator
L_1	current limiting reactor
L_1, C_1	oscillatory circuit for source side TRV
ML	multi-loop reignition circuit
G_m, G_h	spark gaps
c_m, vc	control unit for firing sequence of spark gaps
AB	auxiliary circuit-breaker
TB	test circuit-breaker
SLF	artificial line for short-line fault tests

Figure 68 - Voltage injection circuit



i power-frequency current in the test and auxiliary circuit-breaker

u_1 transient recovery voltage from power-frequency current circuit

u_t voltage across the test circuit-breaker

u_x voltage across the auxiliary circuit-breaker

t_i instant of voltage injection

Figure 69 - TRV waveshapes in a voltage injection circuit

10.1.5 Circuits for capacitive current switching tests

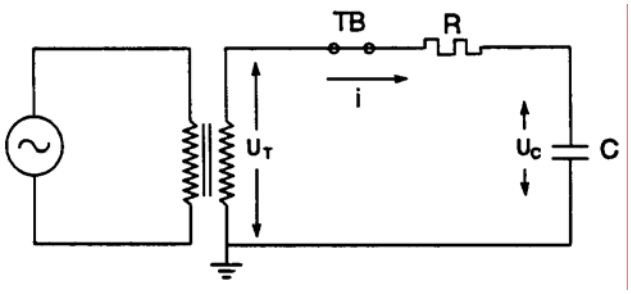
The synthetic circuits described above are used to "extend" the short-circuit power of a high-power laboratory with limited capacity.

The major factor for capacitive current switching is the frequency of voltage and test current. When simulating 60 Hz conditions using a 50 Hz source, the test voltage has to be increased by 44 % to ensure that the recovery voltage during the first half cycle exceeds the required 60 Hz recovery voltage. This results in a too high voltage stress on the circuit-breaker.

In Figure 70 an example is given of a synthetic test circuit that is based on 50 Hz, but results in approximately 60 Hz stresses on the circuit-breaker.

As can be seen in Figure 70 a resistor is used in series with the capacitive load. The resistance value is chosen such that a phase shift of 30 electrical degrees is obtained between voltage and current (see Figure 71).

This circuit has a disadvantage in that it tends to prolong the shortest arcing times, which makes it easier for the circuit-breaker to interrupt without restrikes.



U_T voltage across transformer

TB test circuit-breaker

R resistor causing phase shift

C capacitive load

u_C voltage across the capacitive load

Figure 70 - Synthetic test circuit for 60 Hz capacitive current switching tests using a 50 Hz source

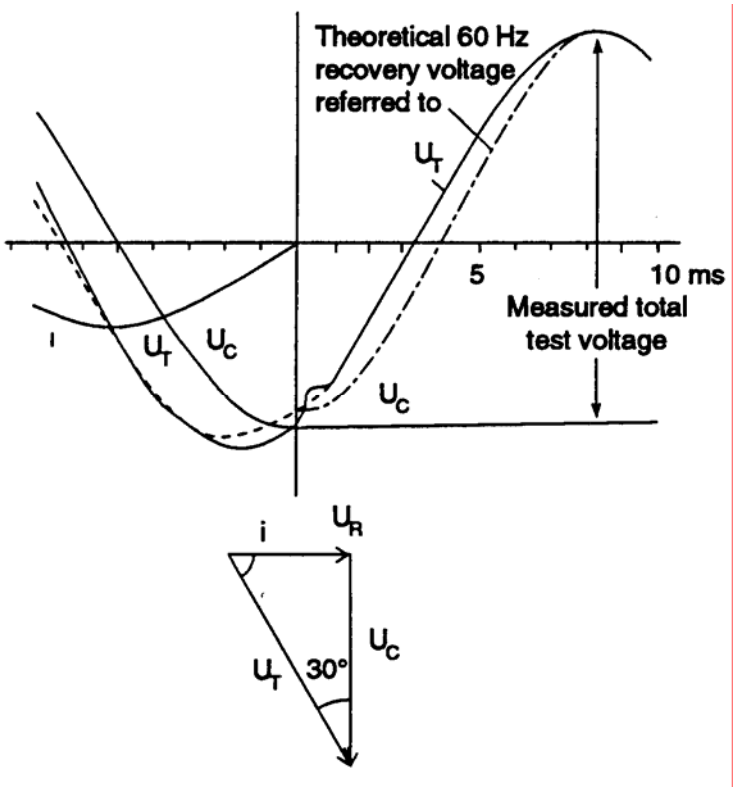
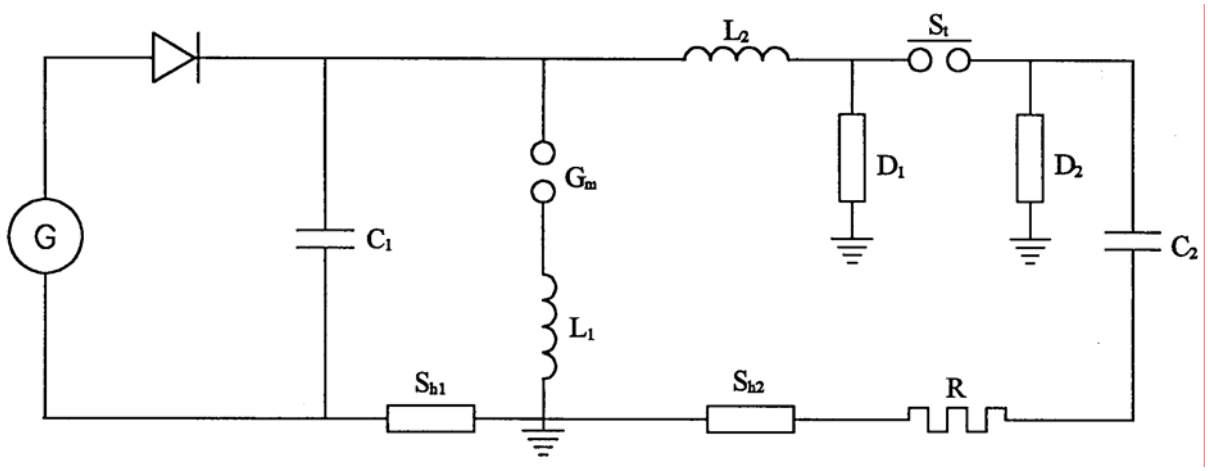


Figure 71 - Voltages obtained in the test circuit of Figure 70

Another example of a synthetic test circuit used to perform capacitive current switching tests at different frequencies is given in Figure 72.



G	generator	$D_{1, 2}$	voltage divider
C_1, C_2, C_3	capacitor	$Sh_{1, 2}$	low-ohmic shunt
G_m	spark gap	S_t	test circuit-breaker
L_1, L_2	inductance	C_2	capacitive load to be interrupted
R	circuit for regulation of voltage jump		

Figure 72 - Synthetic test circuit for capacitive current switching tests at different frequencies

In the circuit shown in Figure 72 capacitor C_1 is charged to a voltage determined by the testing voltage and current. When the spark gap (G_m) is triggered, capacitor C_1 is discharged across the circuit consisting of L_1, L_2, R, and C_2. The frequency of the discharge current f_d is equal to

$$f_d = \frac{1}{2\pi\sqrt{L_1(C_1 + C_2)}}$$

with $L_1 >> L_2$ and $C_1 >> C_2$

where C_1, C_2, L_1 and L_2 are the values of the capacitance and reactance, respectively.

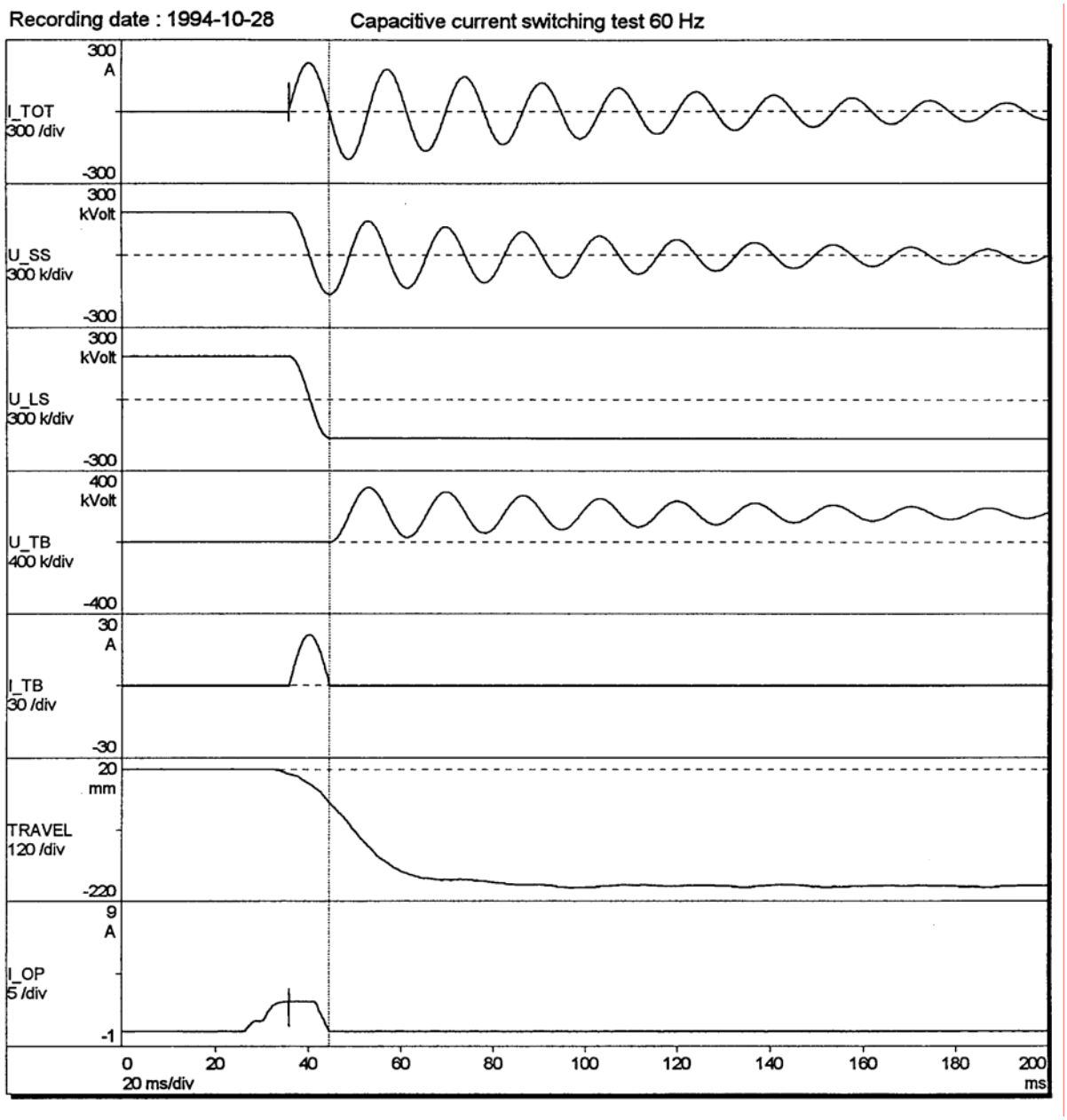
The frequency of the recovery voltage f_r is given by:

$$f_r = \frac{1}{2\pi\sqrt{L_1 C_1}}$$

For a given r.m.s. value of the testing current I_c the following is applicable:

$$I_c = \frac{U_{charge}}{Z_c}$$

where $Z_c = 1/\omega C_1$.



I_TOT	discharge current (Sh_1)
U_SS	voltage supply side (D_1)
U_TB	recovery voltage across the test circuit-breaker
I_TB	current through test circuit-breaker (Sh_2)
TRAVEL	contact travel
I_OP	current through opening coil

Figure 73 - Typical current and voltage waveshapes obtained in the circuit of Figure 72

As can be seen from the oscillogram, this circuit has a number of disadvantages:

- due to the high damping factor, the recovery voltage is not a 1-cos wave;
- the voltage cannot be maintained during 300 ms;
- in the transition from short arcing times to long arcing times the source voltage must be raised to obtain the correct recovery voltage. Should the circuit-breaker then interrupt with

a short arcing time, the recovery voltage will be too high and the circuit-breaker may restrike.

The circuit will, however, give the correct stresses in the first period following interruption and is therefore accepted as an alternative by some utilities.

10.2 Synthetic making tests

The making duty generally has more implications for the switching device than for the system. Due to arcing activity (‘pre-arcing’) in the period from the breakdown between the approaching contacts (‘pre-strike’) until the galvanic contact touch, the contact system faces considerable arcing stress.

The principle is outlined in Figure 74, where the process of making of a short-circuit current is outlined. The decaying dielectric strength of the contact-gap is indicated by two straight lines (RDDS1, RDDS2).

Two extreme situations are indicated:

- the first, (RDDS1) leading to the maximum pre-arcing time, occurring after pre-strike near phase voltage peak and initiating a symmetrical current;
- the second (RDDS2) is the minimum pre-arcing time, when pre-strike occurs near voltage zero and causes a fully asymmetrical current.

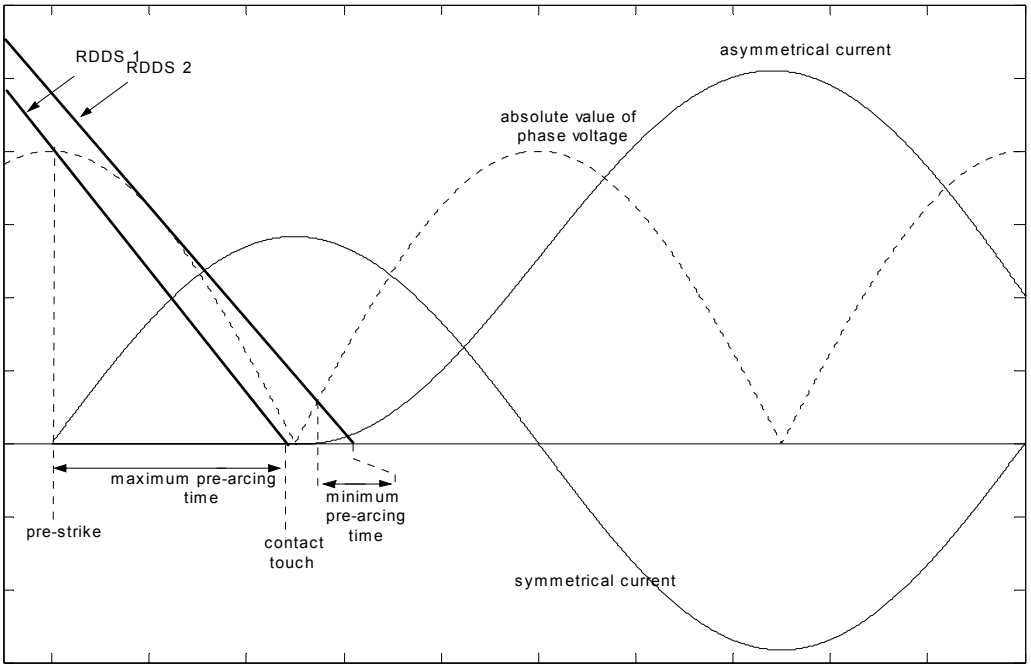


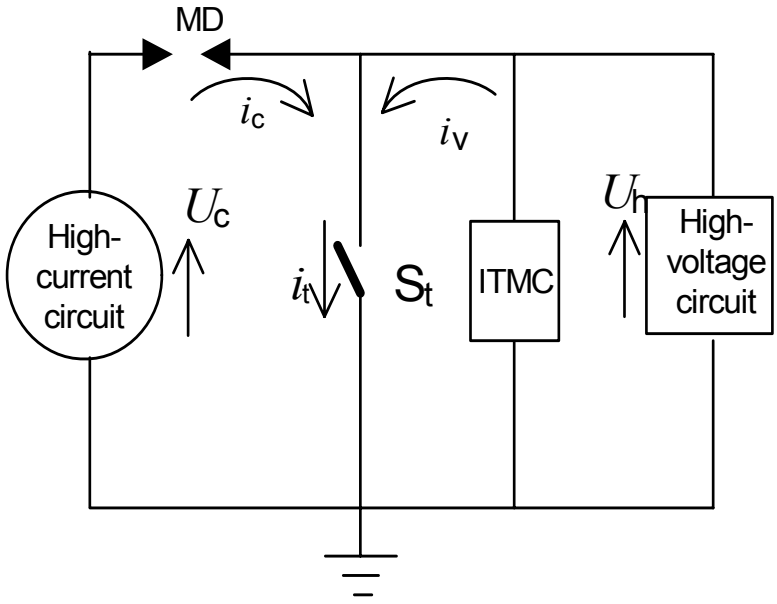
Figure 74 - Principal outline of symmetrical and asymmetrical current after making

The second situation is only possible when closing speed is sufficiently high, whereas slow contact approach inevitably leads to pre-strike near voltage maximum and symmetrical current. It can easily be understood that the pre-arcing stress in the first situation is considerably higher than in the second. An appropriate design of contact system and mechanism should prevent unacceptable contact welding and wear.

The contact system must deal with the presence of forces originating from high magnetic fields, pressure from arcing and frictional forces of (eroded) contacts.

10.2.1 Single-phase making tests

For circuit-breakers with a separate mechanism for each pole the making tests can be carried out in a single-phase direct circuit. This circuit supplies both the appropriate voltage and short-circuit current. Due to limitations of the laboratory, the making tests can be made in a single-phase synthetic circuit where the appropriate voltage just before prestrike comes from a high-voltage source and the short-circuit current comes from a circuit with a reduced voltage. The basic circuit is outlined in Figure 75.

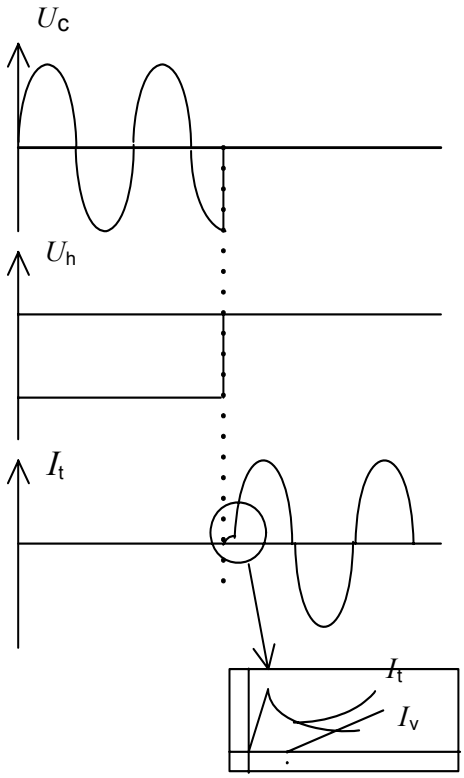


Key

U_c	Voltage of current circuit	S_t	Test circuit-breaker
MD	Making device (triggered spark gap)	ITMC	Circuit for initial transient making current
i_c	Current in the current circuit	U_h	Applied voltage
i_t	Current in the test circuit-breaker	i_v	Initial transient making current

Figure 75 - Principal circuit for single-phase synthetic making tests

An example of an oscillogram showing the voltage and current traces of a single-phase synthetic making test are outlined in Figure 76.



Key

U_c	Voltage of the current circuit
U_h	Applied voltage
i_t	Current through the test circuit-breaker
I_v	Initial transient making current

Figure 76 - Voltages and current in a single-phase synthetic making test

10.2.2 Three-phase making tests

Three-phase making tests may be essential to verify the ability of a three-pole circuit-breaker with common mechanism to close and latch, since the mechanism has to operate against the pressure from pre-arcing in all three phases.

An example of a test, where the two requirements are fulfilled in one single direct test is given in Figure 77.

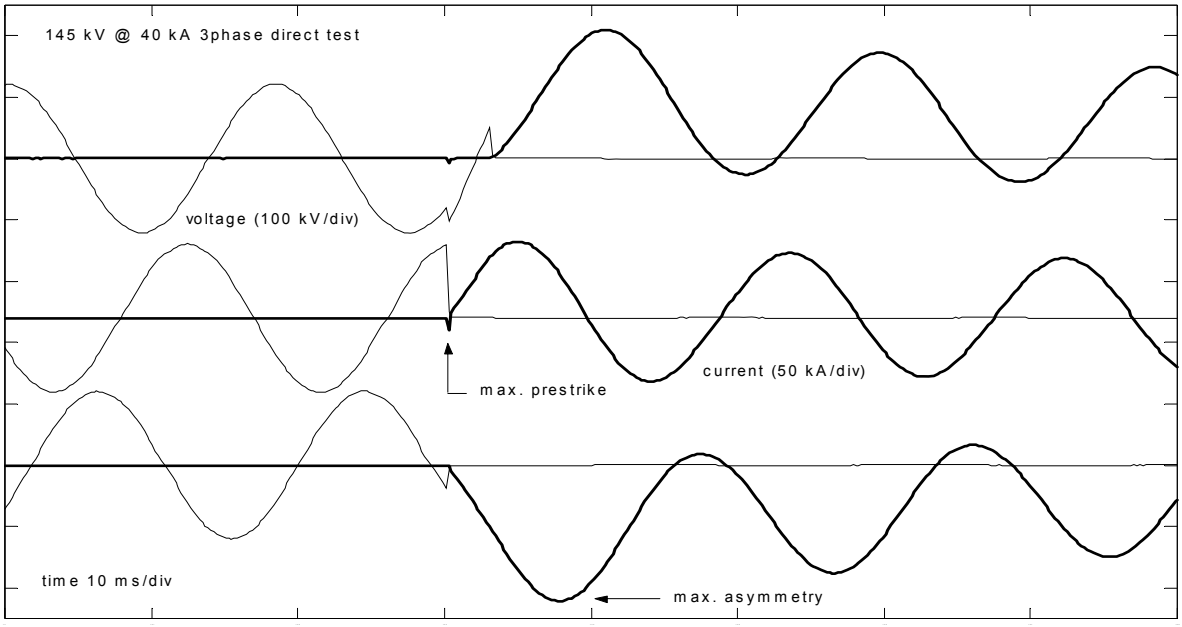


Figure 77 - Current through (thick lines) and voltage across the circuit-breaker (thin lines) during a direct three-phase test of a 145 kV, 40 kA circuit-breaker, combining maximum pre-strike and maximum asymmetrical peak in one test

The circuit for a three-phase synthetic making test is almost similar to a three-phase synthetic test circuit for breaking. In the present practice for synthetic making tests, two separate voltage sources are applied to generate the suitable voltage against which the circuit-breaker must close in order to provoke pre-strike. With this circuit, synthetic three-phase make tests can be performed. The basic circuit is outlined in Figure 78.

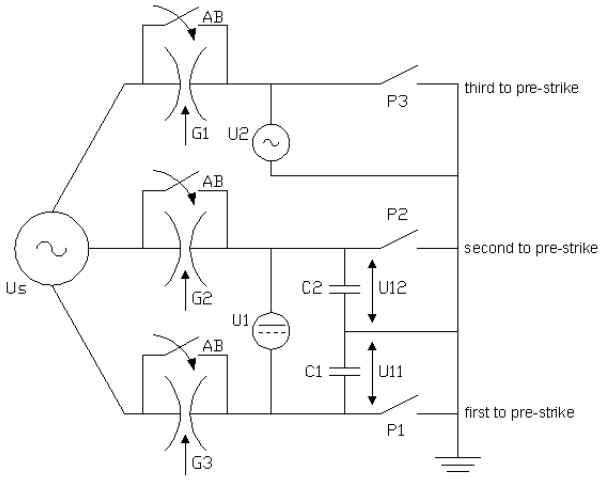


Figure 78 - Principal circuit for three-phase synthetic making tests

The oscillogram of a full-scale test with this circuit is shown in Figure 79.

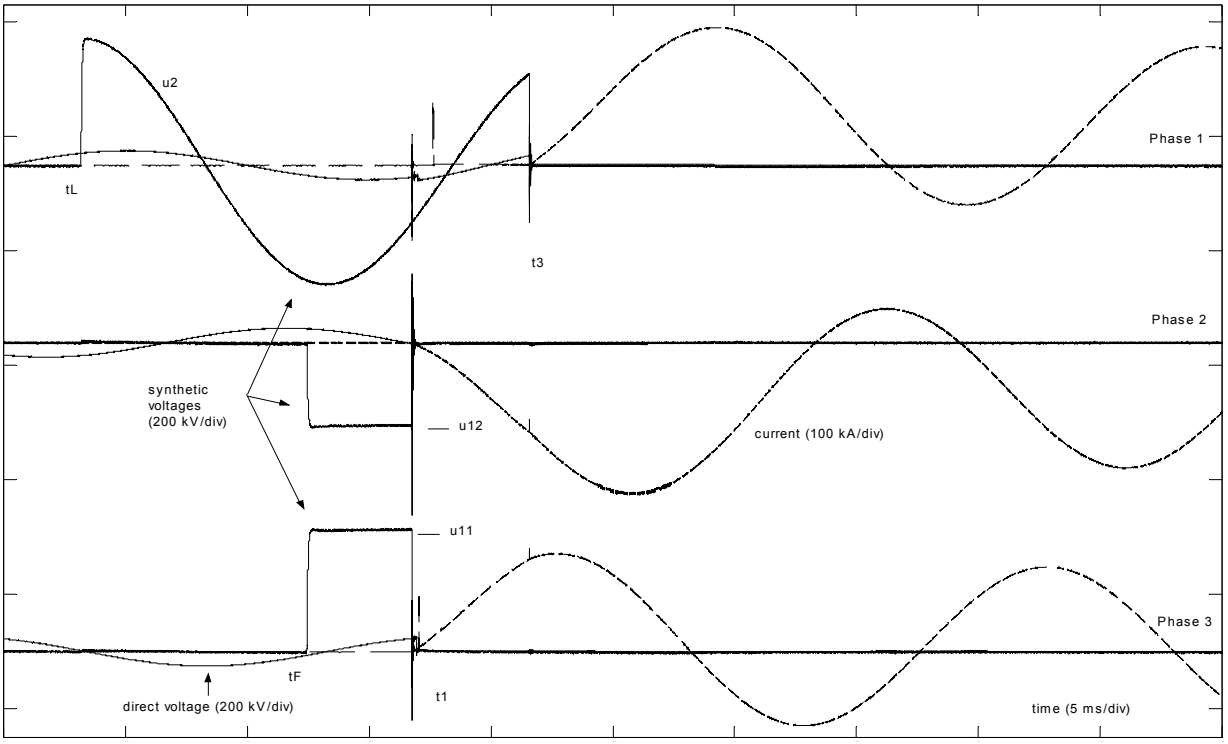


Figure 79 - Oscillogram of actual full-power three-phase synthetic make test. For symbols see text

In Figure 78, the three-phase source U_s (short-circuit transformers) represents the high-current source, supplying the main current at reduced voltage (approximately 30 kV, 'direct voltage' in Figure 79) to the test-object poles P_1, P_2, P_3. The two synthetic voltage sources (pre-charged capacitor banks) are represented in Figure 78 as U_1 and U_2. These sources are activated by triggered gaps.

Prior to the full-scale tests, the pre-arcing times are determined under low power condition (high-voltage only), so that the expected order of pre-strike is known.

The DC source U_1 is positioned between the first and second phase to pre-strike, and has a voltage $U\sqrt{2}$, graded by the capacitors C_1 and C_2 so that the first phase to prestrike has a voltage of $U\sqrt{(2/3)}$, the peak value of the rated voltage (u11 in Figure 79). U_1 is activated at t_F approximately 10 ms prior to the expected pre-strike. By applying DC voltage, pre-strike at maximum voltage is ensured, thus implying maximum pre-arcing time.

Upon pre-strike in phase 3 at t_1, the total voltage of U_1 suddenly transfers to the second phase to pre-strike, resulting in pre-arcing in this phase, simulating the phase-to-phase interaction in three-phase systems. This process can be seen clearly in Figure 80 as a peak in the "synthetic voltage" of phase 2 at a time very shortly after t_1. Since this peak is 45 % higher than the (1 p.u.) pre-strike voltage of phase 3, it can be assumed safely that phase 2 also prestrikes.

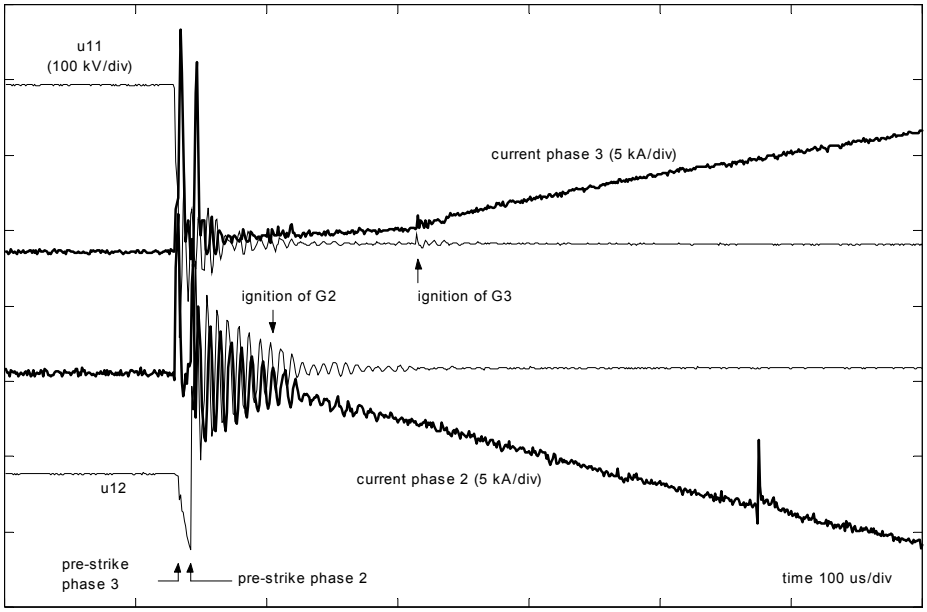


Figure 80 - Expansion of the time period where the high-current circuit starts to supply current after pre-strike of the poles P_3, P_2 of the test object

U_2 is an AC source across the last phase to pre-strike, generated by the discharge of a pre-charged capacitor through a reactor with a high quality factor. This source is activated at t_L some 20 ms before the expected pre-strike in the last phase. The peak voltage of this source is targeted at $U\sqrt{}(2/3)$ and is synchronized practically in phase with the correspondent direct phase-to-earth voltage. This source must be an AC source, in order to prove withstand of the AC peak voltage and to allow a delayed pre-strike (at t_3) in this phase with respect to the two other phases.

Immediately after the breakdown of voltage in the breaker, spark gaps G1, G2 and G3 are automatically activated by current sensors that activate trigger circuits for each gap separately. Ignition delay is usually smaller than 100 μs, and the sources U1 and U2 must be designed such that they can sustain the arc in the test-object until the ignited gaps start to conduct the main short-circuit current. Another 5 ms later, the auxiliary circuit-breakers (AB) are closed to transfer the current from the spark gaps to the AB, thus reducing the thermal stress on the spark gaps.

10.3 References

[1] IEC 62271-101 (2006): High-voltage switchgear and controlgear – Part 101: Synthetic testing

10.4 Bibliography

Biermans (J.), The Weil Circuit for the testing of high-voltage circuit-breakers with very high rupturing capacities. CIGRE 1954, Report 102.

Damstra (G.C.). Three-phase synthetic make test circuits. Colloquium CIGRE SC 13, Sarajevo, Paper 27 (1989).

Bonfanti (I.), Aldrovandi (G.), Kuhnhard (G.), Pliet (H.). Nouvelles applications d'utilisation de circuits synthétiques au CESI et à l'IPH. CIGRE Session 1992, Rapport 13-201 (1992-08).

Janssen (A.L.J.), te Paske (L.H.), Smeets (R.P.P.). Limitations of high-power testing methods for EHV and UHV circuit-breakers. CIGRE Session 2002, Rapport 13-105 (2002).

Daigneault (G.), St-Jean (G.), Landry (M.). Comparing direct and synthetic tests for interruption of line-charging capacitive current. IEEE Transactions on Power Delivery, vol. 16, N°3 (2001-07).

Manganaro (S.), Rovelli (S.), A new circuit for synthetic auto-reclosing test duties under short-circuit conditions on high power circuit breakers. IEEE Transactions on Power Apparatus and Systems Vol.96 (1977-10).