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STATIC SYNCHRONOUS SERIES COMPENSATOR (SSSC)

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Static Synchronous Series Compensator (SSSC)

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INTRODUCTION

CHAPTER 1. UNDERSTANDING STATIC SYNCHRONOUS SERIES COMPENSATOR (SSSC) CONCEPT

1.1 OPERATING PRINCIPLES

The *SSSC* is a reactive power series compensator employing a Voltage-Sourced Converter (VSC) in series with the transmission line, as shown in Figure 1.1. This operating mode emulates a controlled series reactive compensation (such as obtained with the Thyristor-Controlled Series Capacitor (TCSC)), but provides wider control range as it can operate equally at capacitive or inductive operating domains as well as it can operate just as voltage source. Thyristor based FACTS controllers, like TCSC, are based on impedande control, so they are dependent on the line current. The SSSC can operate as a voltage source, which garantees series compensation independent of the line current.

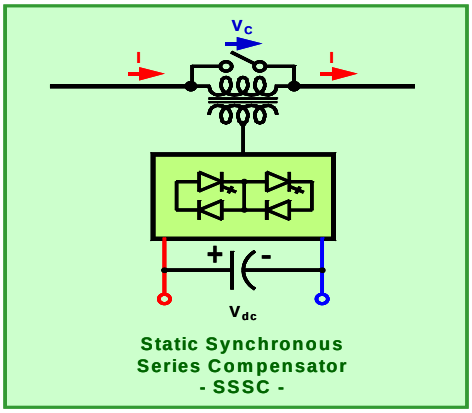

Figure 1.1 Schematic diagram of SSSC

The VSC within the SSSC is operated in synchronism with the transmission line *current*. The voltage generated by the VSC is kept in quadrature with the line current, lagging or leading it by 90 degrees. The injection of a lagging voltage with respect to the line current emulates a series capacitor, whereas a leading voltage emulates a reactor in series with the line. Thus, the SSSC can provide either series capacitive or series inductive compensation, without any rating increase or additional reactive components, by its inherent capability to reverse the polarity of the output voltage it generates. The quadrature relationship between the output voltage of the SSSC and the line current ensures substantially zero real power exchange between the SSSC and the ac system, except for the small amount (about 1% at full output) required to replenish the internal losses of the converter. This power is drawn from line by the converter, by a small (typically less than one degree) deviation from the ideal 90°, to keep the dc capacitor charged without an external dc power supply.

The capacitive compensation in effect injects a voltage in series with the line that is in phase opposition to the voltage produced by the line current across the series line reactance. As a result, the voltage across the series line reactance is forced to increase, as if its inductance was reduced, causing a proportional increase in the line current and the corresponding transmitted power, as illustrated in Figure 1.2. Similarly, inductive compensation (when the SSSC's output voltage leads the line current) injects a voltage in phase with the voltage across the line reactance. As a result, the voltage across the line reactance decreases, as if its inductance was increased, causing the line current and the corresponding transmitted power to proportionally decrease. The line current and the corresponding power increase or decrease is proportional to the magnitude of

the series compensating voltage relative to the voltage across the series line reactance. Traditionally, this is expressed by the *degree of series compensation,* which is defined as the impedance ratio of the series line reactance to the effective series capacitor, or, equivalently, the amplitude ratio of the voltage across the series line reactor to the series compensating voltage. The adjustment of the converter voltage amplitude can be accomplished by the control of the dc voltage through the momentary charge or discharge of the dc capacitor. Alternatively, the voltage amplitude can be adjusted internally in the converter by pulse-width-modulation, or other techniques, from a fixed (regulated) dc voltage.

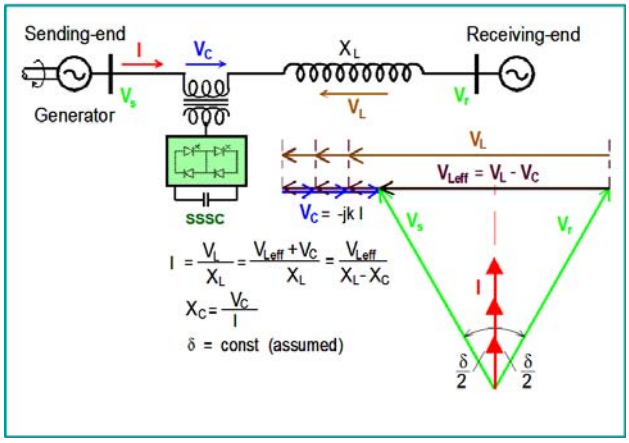

Figure 1.2 Vector diagram illustration for capacitive and inductive operation modes of the SSSC

The SSSC can control the effective transmission line impedance by injecting a controllable compensating voltage in quadrature with the line current to emulate a series capacitor or reactor. Emulated capacitive compensation will decrease the effective series line impedance, whereas emulated inductive compensation will decrease it. Thus the SSSC can increase or decrease steady-state power flow or change it dynamically to counteract dynamic disturbances in order to increase transient stability and damp power oscillation.

1.2 BASIC CHARACTERISTICS

Due to the almost ideal voltage source characteristic of the VSC, the SSSC can provide capacitive or inductive compensating voltage independent of the line current, up to its specified voltage rating. Thus the SSSC can maintain the rated maximum capacitive or inductive compensating voltage in the face of changing line current, theoretically in the total operating range of zero to I_{max}, as illustrated in Figure 1.3. (The practical minimum is the line current value at which the SSSC is still able to absorb enough power to replenish its operating losses.)

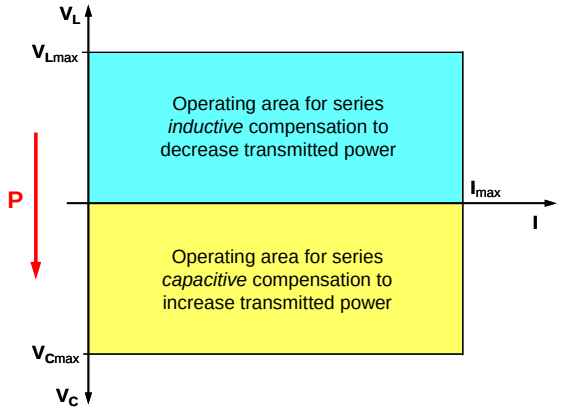

Figure 1.3 Operating range Characteristics of SSSC

The transmitted power versus transmission angle, i.e., the P_q-δ characteristic of the SSSC at various per unit values of the compensating voltage, V_q, (which may be capacitive or inductive) is shown in Figure 1.4. This figure illustrates that the unique capability of the SSSC in maintaining the maximum compensating voltage independent of line current, results in a wide control range for the transmitted power at a given transmission angle, and provide the means to force the desired power flow under the condition of insufficient or changing transmission angle. (The reader should recall that the compensating voltage produced by a conventional series capacitor changes in proportion with the line current and, consequently, with the transmission angle.) It is observable in Figure 1.4 that the SSSC is also able to decrease the transmitted power; in fact, with suitable rating, it can actually reverse the direction of power flow.

Since the SSSC emulates the line compensation of the series capacitor by the direct injection of the required compensating voltage at the fundamental system frequency, without reproducing the impedance versus frequency characteristic of a physical capacitor, it is, in contrast to the series capacitor, unable to form a classical series resonant circuit with the inductive line impedance to initiate sub-synchronous oscillations. In other words, independent of whether the SSSC is operated in the capacitive or inductive compensating domain, it is seen by the system as a (zero-impedance) voltage source in series with a small inductive impedance (the leakage impedance of the coupling transformer). Because of its fast response, the SSSC could theoretically provide effective damping of sub-synchronous oscillation by suitable control, should the condition for sub-synchronous oscillation be established by (existing) series capacitors.

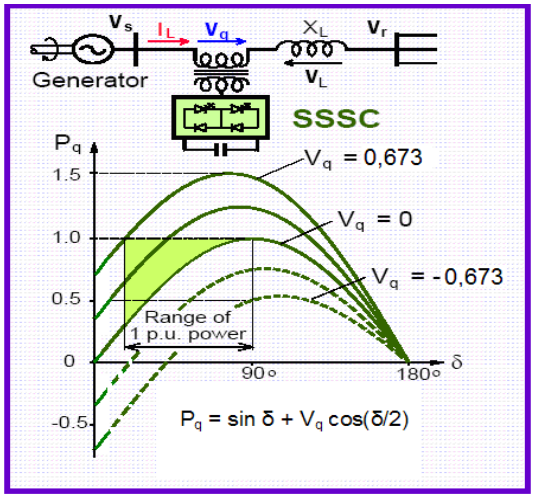

Figure 1.4 P_q-δ characteristic with SSSC

A comparison of the basic operating characteristic of the SSSC to that of the STATCOM reveals their duality: In a given operating range, determined by the rating of the VSC employed, the series-connected SSSC can maintain reactive compensating *voltage* independent of the line current, whereas the shunt-connected STATCOM can maintain reactive compensating *current* independent on the transmission line voltage.

1.3 APPLICATIONS

The SSSC is one of the most powerful FACTS controllers for power flow control. Although it can provide transmission line voltage regulation by the control of the effective line impedance, particularly for the end-voltage of a radial line, the primary purpose of the SSSC is usually the direct, and dynamic, control of the transmitted power in a given line. The main applications within the broad area of adjustable or dynamic power flow control are as follows:

- ***Compensation of long transmission lines.*** Because of the relatively large series inductance of long transmission lines and the correspondingly large transmission angle required, the voltage profile substantially droops towards the mid-point with increasing line current, causing heavy flow of reactive power and an uneconomically low limit on the transmittable real power. Series capacitive compensation is the most effective means to increase the transmittable power by reducing the overall transmission impedance and angle. To handle changing load conditions and line contingencies, the series compensation may need to be variable. In addition, concerns of sub-synchronous resonance may limit the safe degree of series compensation by conventional capacitors. The SSSC can provide an economical solution in combination with conventional series capacitor banks to provide a vernier control by adding to, or subtracting from, the fixed compensation provided by the capacitors, and also to increase the immunity against sub-synchronous oscillation

- ***Equalization of power flow in lines and prevention of loop-flows of real power.*** The inherent capability of the SSSC to decrease as well as to increase (real) power flow in the line makes it eminently suitable to equalize line power flows and prevent loop-flows

of power. Both of these allow higher power transmission, and thus higher utilization of the power system, without thermal limit problems.

- ***Receiving end voltage regulation of a radial line***. The receiving end-voltage of a radial line varies with the load and, in particular, with the power factor of the load due to the reactive line impedance. The SSSC can be used to regulate the end-voltage of a radial line by controlling the degree of series compensation so as to keep the end-voltage constant in face of changing load and load power factor. (Note that, although the end-voltage can be regulated, the load power factor cannot be corrected by series compensation.)

- ***Improvement of transient stability and dynamic stability (power oscillation damping)***. Transient stability improvement and power oscillation damping by the shunt-connected STATCOM is achieved through the increase and subsequent decrease of the transmission line (mid-point) voltage during the accelerating and decelerating swings of the disturbed machine(s). The powerful capability of the series-connected SSSC to control the transmitted power can be utilized more effectively to increase the transient stability limit and to provide power oscillation damping. In these applications the SSSC is controlled to force the line current and power flow to increase, by rapid injection of the necessary compensating voltage, when the relevant machines in the system accelerate, and, conversely, force the line current and transmitted power to decrease when the machines decelerate. The function of rotational stability improvement can be, of course, combined with other power flow objectives relevant to the dynamically stable power system (e.g., power flow optimization, line current equalization, etc.).

CHAPTER 2. COMPARISON OF SSSC WITH OTHER TECHNOLOGIES

This chapter presents a brief comparison of SSSC and other technologies like Fixed Series Capacitor, Fixed Series Reactor, Phase-Angle Regulator (PAR), Thyristor-Controlled Series Capacitor (TCSC) and Gate-Controlled Series Capacitor (GCSC) and the Magnetic Energy Restorer Switch (MERS). The comparison shown below is for the case of conventional long transmission lines, however with equivalent length smaller than ¼ of wavelength (1250 km and 1500 km, respectively, for 60 Hz and 50 Hz system).

2.1 FIXED SERIES CAPACITOR

Figure 2.1 shows a transmission system with fixed series capacitive compensation, which naturally has no controllability and, therefore, has no flexibility. Figure 2.2 shows the compensation characteristics for three different level of fixed capacitive compensation. The operating area of an SSSC is a rectangle in the V-I plane as shown in Figure 2.2 and for the fixed capacitive compensation we have only a fixed line for each value of the compensation capacitance. In this compensation, the larger the capacitive reactance the larger will be the transmitted power.

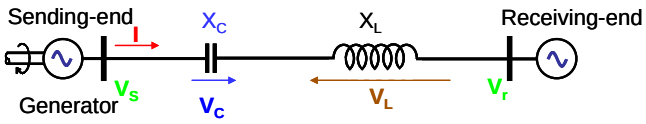

Figure 2.1 Fixed capacitor compensation

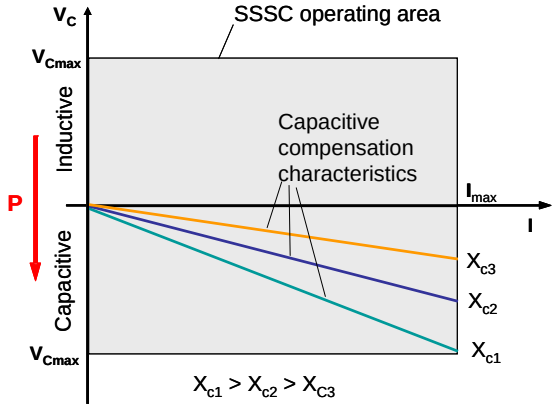

Figure 2.2 Fixed capacitive compensation characteristics

2.2 FIXED SERIES REACTOR

Figure 2.3 shows a transmission line with fixed inductive compensation, which is not very common as it works in a way to decrease the transmitted power as shown in Figure 2.4. As in the case of fixed capacitive compensation the power transmission characteristics is given just by a line for each compensation level and the larger the reactance the smaller the transmitted power.

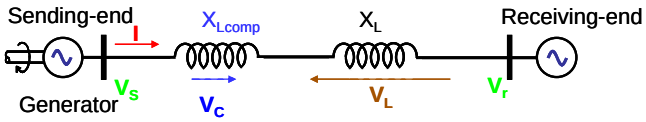

Figure 2.3 Transmission system with fixed inductive compensation

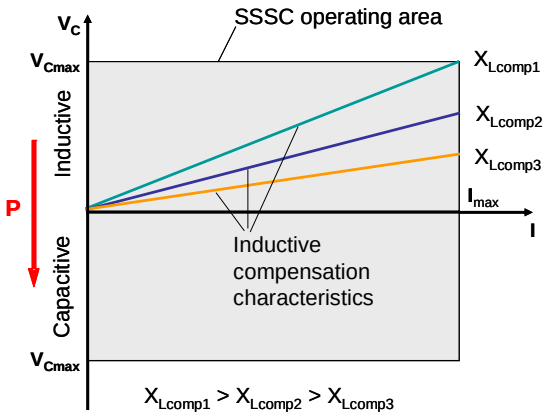

Figure 2.4 Fixed inductive compensation characteristics

2.3 PHASE ANGLE REGULATOR (PAR)

Figure 2.5 shows a transmission system with a Thyristor Controlled Phase Angle Regulator (TCPAR). The TCPAR shown in this figure is composed of a transformer with primary winding connected in shunt between two phases and three secondary winding connected in series with the other phase. The voltage injected in series with the line is the sum of the voltages in the three secondary windings controlled by thyristors valves. The winding that is fully connected adds a sinusoidal voltage in series with the line. The winding that is partially connected has its voltage controlled by the firing angle of the thyristors.

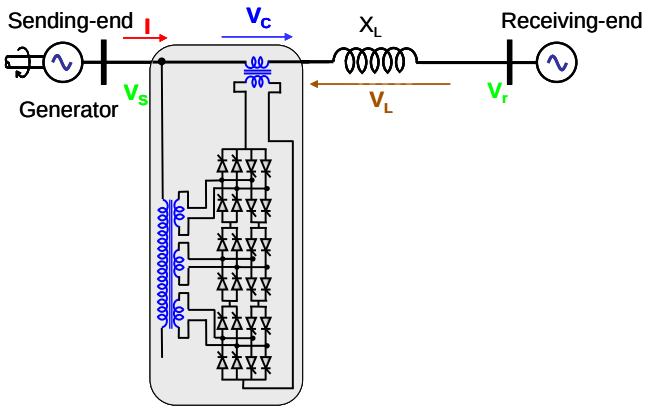

Figure 2.5 Transmission line with phase angle regulator

Figure 2.6 shows the phasor diagram of the sending-end voltage V_S and the compensating voltage V_C. This compensation voltage can have +90° or -90° phase difference with respect to

the sending-end voltage V_S. Different from the SCCC, the phase angle of the compensating voltage of a TCPAR can lead the current phasor or lag it by an angle that does not need to be in quadrature. Therefore, depending on this phase difference, the series transformer may have to inject or absorb active power, which is supplied or absorbed by the shunt winding.

If we compare the operating area of the TCPAR considering voltage and current magnitudes with the case of SSSC we will find that they are basically equal. That is, the voltage can vary from zero to its maximum value and the same happens with the current. Therefore, the operating area in the VxI plane is a rectangle like in the case of SSSC. The difference is that in the case of SSSC the compensation voltage is always in quadrature with the line current while in the TCPAR this angle between compensation voltage and current can have any value. However, this phase difference is not controllable. It appears as a function of the current phase with respect to the sending-end voltage. Depending on the number of secondary windings and the switching control of the thyristor, the TCPAR may present higher level of low-order harmonic components injected in series with the line. However, the number of secondary windings are chosen in a way that harmonics are kept in an acceptable range.

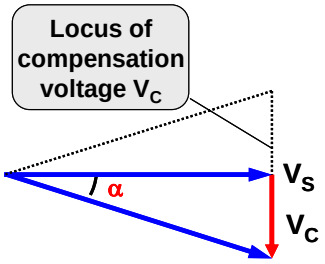

Figure 2.6 Phasor diagram for the phase angle compensation

2.4 THYRISTOR-CONTROLLED SERIES CAPACITOR (TCSC)

The SSSC, as presented previously, is a device based on voltage-sourced converters (VSC) and, therefore, can operate in a rectangular area in the VxI plane, that is, it has a wide controllability range as seen in the previous section. The TCSC, on the other hand as explained by Hingorani and Gyugyi [2.1], is a device based on the concept of impedance control as explained in [2.1]. The control device is the thyristor which is a semiconductor switch, at least, one generation older than the switch used in the SSSC. However, due to its relatively low cost, there are various examples of actual applications around the world for power oscillation damping or power flow control. Gama, Angqüist, and Ingeström [2.2] presented a paper on the commissioning of a TCSC for power oscillation damping in the Brazilian North-South transmission line.

Figure 2.7 shows a transmission system with a TCSC in series. This figure shows that this series device is composed of a fixed series capacitor in parallel with a Thyristor Controlled Reactor (TCR). If the thyristors are not conducting only the capacitor is in series with the line. If the thyristors are switched on with a given firing angle the current and voltage waveforms can be as shown in Figure 2.8. The reactor current, in Figure 2.8(a), has a pulse like waveform. This current flows through the capacitor producing a current waveform as shown in Figure 2.8(b). Figure 2.8(c) shows the capacitor voltage waveform where we can see that some harmonic content is present in the voltage that is in series with the line. However; in general, harmonic generated by the thyristor switching is not a serious problem if the reactor and capacitor size, as well as firing angle, are correctly chosen.

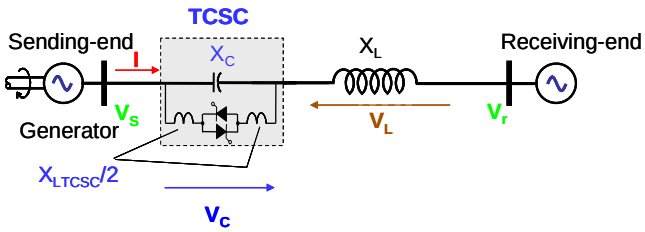

Figure 2.7 Transmission line with Thyristor-Controlled Series Capacitor (TCSC)

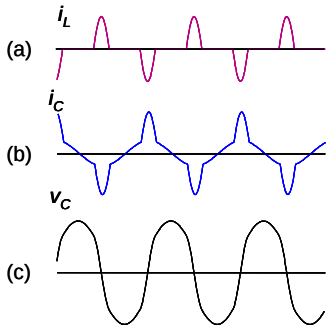

Figure 2.8 Current and voltage waveforms in a TCSC

The equivalent impedance of the fixed capacitor in parallel with the thyristor controlled reactor may produce equivalent impedance that may be capacitive or inductive as shown in Figure 2.9. This figure shows the equivalent impedance of a TCSC for firing angle varying from 90° to 180°. For firing angle close to 90° the equivalent impedance is inductive and for firing angle close to 180° it is capacitive. At about the middle of the range of 90° to 180°, the fixed capacitor and the controlled reactor present a resonance and the device can not be operated in this region because too large current may flow in the LC circuit. When the TCSC operates with capacitive characteristics, normally the firing angle has a minimum limit that produces the maximum compensating capacitive impedance Z_{max}. In Figure 2.9 this limit is slightly below 150°. This device has minimum compensating impedance Z_{min} that is given by the capacitor alone when the firing angle of the thyristors is equal to 180°, that is, the thyristors are off. Then, the capacitive continuous impedance control range goes from Z_{min} to Z_{max}.

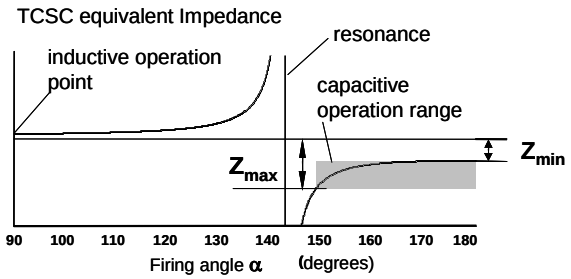

Figure 2.9 TCSC equivalent impedance characteristics as function of the thyristor firing angle

In some cases, when it is necessary to decrease the transmitted power in the line, the TCSC can be operated with firing angle equal to 90° and it will present inductive characteristic. In this operating condition the firing angle is not varied, therefore, there is no continuous control in the inductive side.

The TCSC operating area in the VxI plane is shown in Figure 2.10. In the capacitive region it can be controlled continuously from Z_{min} to Z_{max}, which is represented by the area defined between the lines for Z_{min} and Z_{max}. If the TCSC is designed for power flow control it can operate in any point of this area continuously without problem of overheating the capacitor, reactor, or the thyristors. On the other hand, if the TCSC is designed only to damp power oscillations it may operate continuously on the line defined by Z_{min} and operate for short time (few seconds) in the area between Z_{min} and Z_{max}. In this last case, a capacitor with smaller VA rating may be used as compared with the case of power flow control.

Comparing the TCSC with SSSC with the information given above allows us to conclude that:

(i) the operating area of the TCSC is much smaller than the SSSC in the capacitive region;

(ii) in the inductive region the TCSC operating characteristics is reduced to a line only as compared to a rectangle in the case of SSSC;

(iii) TCSC may present problem of internal resonance that has to be avoided.

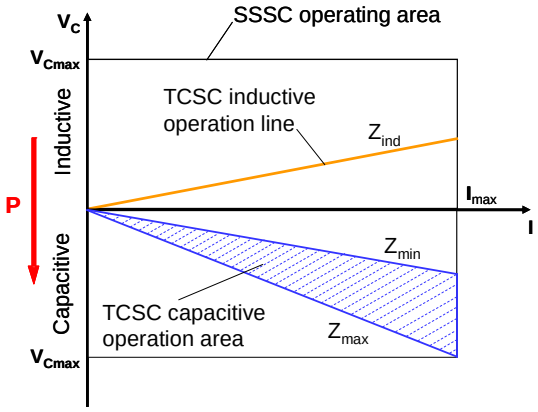

Figure 2.10 TCSC operating area

Despite the advantages of the SSSC as compared with the TCSC, this thyristor based device is still used as a practical option when wide range of controllability of the SSSC is not necessary. When low cost is an objective the TCSC is also a good option.

2.5 GATE-CONTROLLED SERIES CAPACITOR (GCSC)

Figure 2.11 shows a transmission line with a Gate-Controlled Series Capacitor connected in series. This is a device also based in the concept of variable impedance and it was originally presented by Karady et al. [2.3] and they called it as "continuously regulated series capacitor". Later, Souza et al. [2.4] introduced the name "GTO-Controlled Series Capacitor" which was adopted by Hingorani and Gyugyi [2.1]. However, due to the fact that different switching device can be used, provided it can be turned off, recently Edris [2.5] has changed "GTO-Controlled" to "Gate-Controlled". In all cases the acronym GCSC was kept to make a contrast with TCSC.

The diagram in Figure 2.11 shows that the GCSC has a very simple structure with basically one capacitor and parallel switches. These switches, in facts, operate as a dual thyristors. These dual thyristors and the capacitor in parallel is exactly the dual circuit of a thyristor controlled reactor (TCR), where a reactor is in series with a thyristor valve. In the case of TCR the control is done by the firing angle. However, in the case of GCSC the switches are turned on automatically always its voltages crosses zero and they have to be turned off to insert the capacitor in series with the line. Therefore, instead of firing angle, in the GCSC the turn-off angle is used.

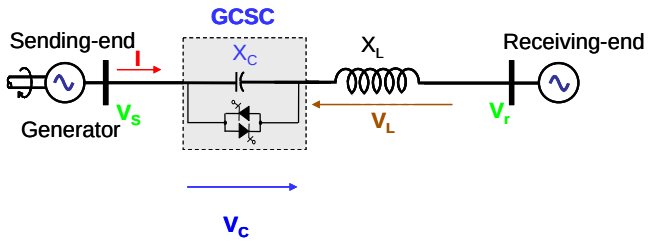

Figure 2.11 Transmission line with a Gate-Controlled Series Capacitor (GCSC)

One interesting point here is that the TCR is a device theoretically well-matched for shunt connection whereas the GCSC is well-matched for series connection. One advantage of the GCSC over the TCSC is the fact that it does not need reactor and, therefore, it may be a more compact device. Souza et al. [2.6] presented a detailed comparison between GCSC and TCSC. If a perfect dual circuit of the TCSC is to be produced, then a reactor has to be connected in series with the capacitor in parallel with the switches. However, this option may not be necessary as the line is normally inductive and putting more series inductance has no meaning except to increase the cost of the compensation device.

Figure 2.12 shows the current and voltage waveforms in the transmission line and in the capacitor of the GCSC. The line current is assumed sinusoidal. As explained above, when the voltage on the capacitor crosses zero the switches are turned on and this voltage is kept null until the switch is turned off at a given turn-off angle. If voltage and current waveforms are compared in a GCSC and in a TCR it is possible to see that they are dual waveforms. That is, the current waveform in a shunt connected TCR has the same shape as the voltage waveform in the series connected GCSC and the voltage waveform (line voltage) on the TCR has the same shape as the current in the GCSC (line current).

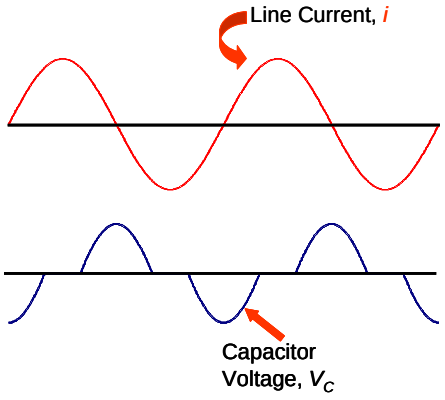

Figure 2.12 Current and voltage waveform in the GCSC

Figure 2.13 shows the equivalent capacitive reactance of the GCSC as a function of the turn-off angle. This figure shows that this reactance is nonlinear and varies smoothly from its maximum value to zero. No resonance problem is present.

Figure 2.14(a) shows the GCSC operating area in the V-I plane for the case where the maximum capacitor voltage occurs for the maximum line current. In this case, the operating area of the GCSC is similar to that of the TCSC with two differences: (i) the minimum capacitive reactance is zero and (ii) there is no inductive reactance (because no reactor was inserted in series). This device has a smaller control range when compared with the SSSC, although it is wider than in the case of the TCSC. The GCSC has fewer components than the TCSC and is much less complex than the SSSC. Figure 2.14(b) shows the GCSC operating characteristics for the case where the capacitor maximum voltage occurs for a line current smaller than its maximum value. In this case the capacitor voltage has to be controlled by the turn-off angle to avoid steady-state overvoltage, except if a high compensation voltage is necessary for a short time, for power oscillation damping, for example.

The SSSC is more flexible and operates in a wider range than the GCSC. The GCSC may be a good option in situation where there is no need of inductive compensation and the compensation can be done by a controlled impedance instead of controlled voltage source as in SSSC.

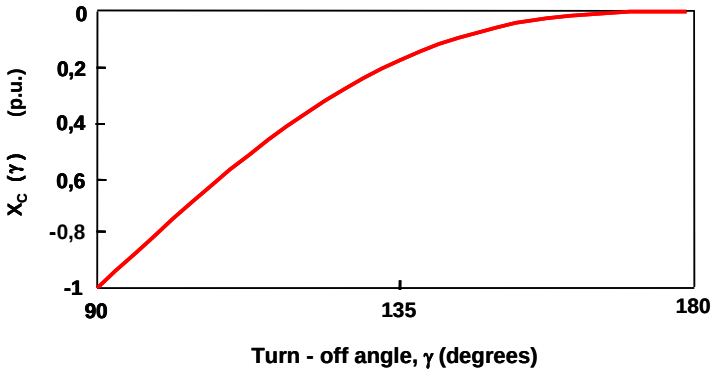

Figure 2.13 Equivalent reactance of the GCSC

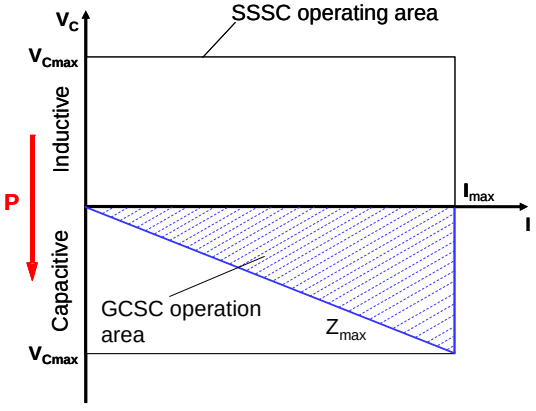

Figure 2.14 GCSC operating area

2.6 MAGNETIC ENERGY RECOVERY SWITCH (MERS)

The Magnetic Energy Recovery Switch (MERS) is a new configuration that has been recently suggested for use in power system transmission application for controlling power flow [2.7, 2.8]. The configuration of the MERS is shown in Figure 2.15. It consists of 4 forced commutated switches and a dc-capacitor in each phase. The configuration is similar to a single phase full bridge, but the operation differs and the size of the capacitor is several times smaller.

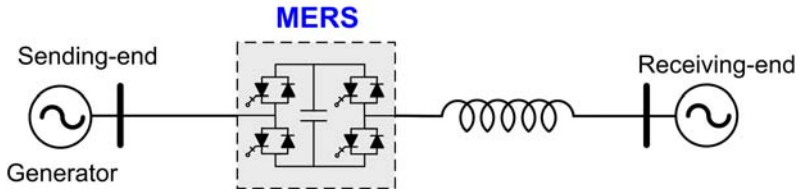

Figure 2.15 Configuration of the Magnetic Energy Recover Switch

By controlling the current path through the device (Figure 2.16) can the device behave like a controllable capacitive voltage source. This is performed by using line frequency switching; meaning one switch is turned on and off only once during and electrical 50 or 60 Hz cycle.

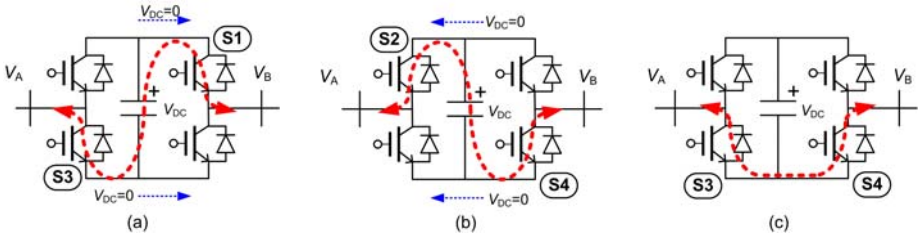

Figure 2.16 Switching pattern

The timing of the gate signals is performed such that the size of the by-pass area and the size of the minimum dc-voltage are controlled (Figure 2.17). As a result, the basic device characteristic becomes like a series connection of a variable capacitor and a voltage source. This is due to the size of the by-pass area directly translates to an equivalent reactance and the minimum dc-voltage translates to a series injected voltage [2.7]. With the dc-voltage reference set to zero, the device behaves like a GCSC at the fundamental frequency. But in contrast to the GCSC, even with low currents, the rated voltage can be injected by increasing the dc-voltage reference.

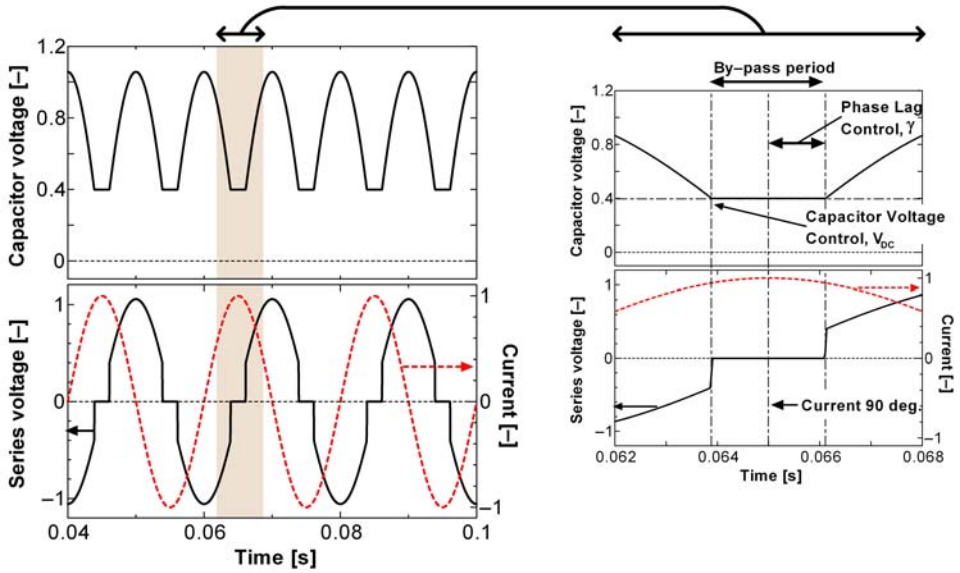

Figure 2.17 Basic control and resulting equivalent circuit of MERS

By optimizing the combination of reactance and series injected voltage can the distortion in the injected voltage be decreased. The resulting harmonic distortion in the whole voltage-current operating range of the MERS is shown in Figure 2.18. The distortion is given in per unit related to the rated series compensation voltage and is shown as a contour plot. The worst distortion occurs for low line currents and high series voltage injection. The distortion for the GCSC will be the same as for the MERS in the lower right triangle part of the MERS operating area.

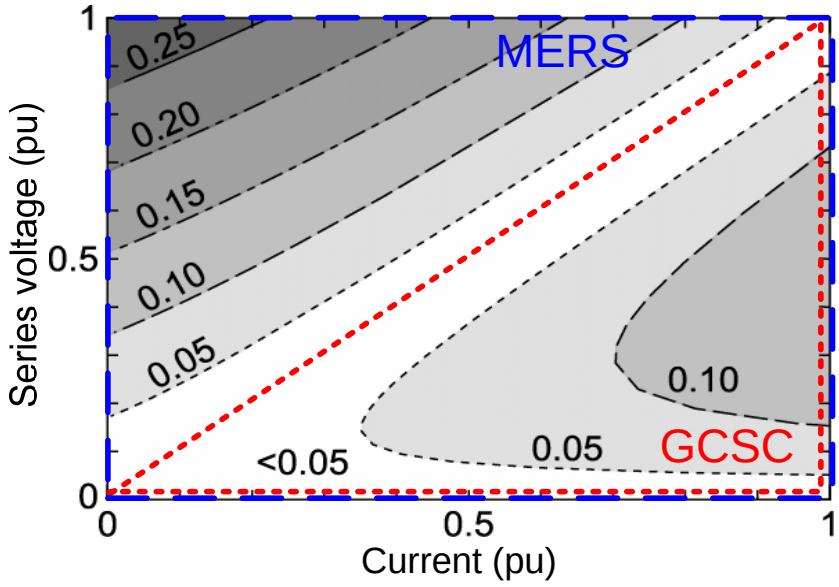

Figure 2.18 Harmonic distortion in per unit related to rated voltage

The sub-harmonic characteristics of the MERS have been investigated with simulations by studying the resulting voltages with current injection at various sub-harmonic frequencies

added on top of a 50Hz frequency component [2.8]. The resulting impedance characteristics can, for a given set-point, be seen in the left part of Figure 2.19. The device has a mainly resistive characteristic in most of the frequency range, indicating good immunity regarding sub-synchronous resonance. The difference to the reactance of a fixed series capacitor is also indicated. The reason it is possible for the MERS to have a resistive component in the sub-harmonic frequency domain without any energy storage is due to the corresponding phase shift for the 50 Hz component. With a dc-offset in the current during a 50Hz cycle will the phase of the injected series voltage be slightly changed, resulting in a small negative 50Hz resistance component. This supplies sufficient energy to be able to inject a resistive voltage in the sub-harmonic frequency domain. The current and series voltage curves for a 10 Hz current component case is shown in the right part of Figure 2.19. The 10 Hz component has been extracted and it can be seen that the current and voltage components are almost in phase, meaning a highly resistive characteristic.

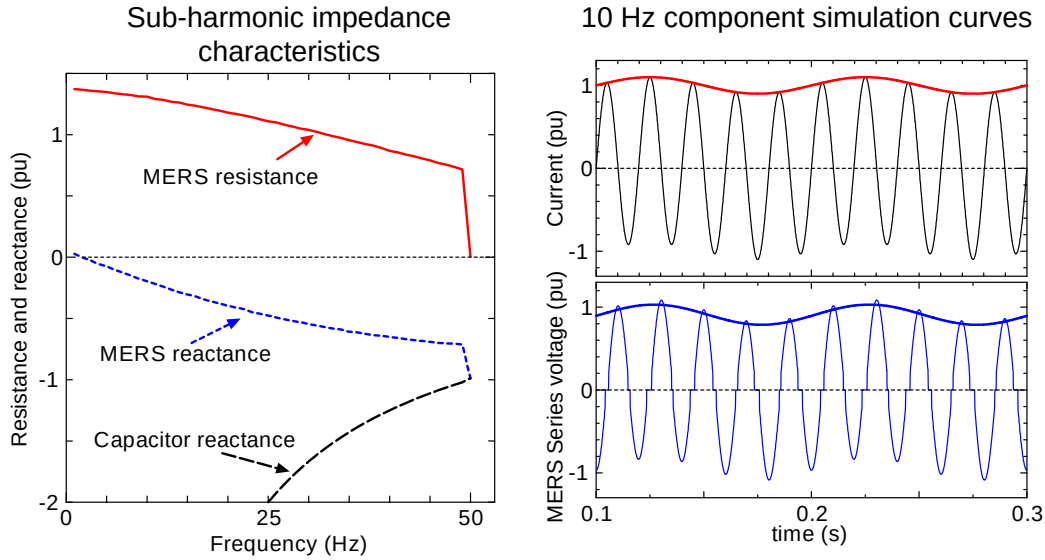

Figure 2.19 Sub-harmonic characteristics of the MERS

The following observations can be made when comparing the SSSC and the MERS:

- The operating range of the MERS is equal the operating range of the SSSC in the capacitive range, meaning half of the total SSSC operating range.
- Both the MERS and the SSSC have good sub-harmonic characteristics
- The MERS has a simpler and more compact configuration than the SSSC, with no series injecting transformer and small capacitor.
- The injected harmonics are potentially lower for the SSSC than for the MERS
- The basic control of the MERS is equivalent to a capacitor and a reactive voltage source in series, while the SSSC is equivalent to a pure reactive voltage source.

2.7 DYNAMIC FLOW CONTROLLER (DYNAFLOW)

By combining the thyristor controlled series capacitor/reactor or the thyristor switched series capacitor/reactor and a phase-shifting transformer, PST, a new FACTS system is suggested. The main advantages of this system are that:

- Controllability even at low transfer levels
- Dynamically controllable
- Rating is split between several modules and future upgrades, changes, are possible
- The weight of each of the building blocks is limited
- Power oscillation damping and transient control

The Dynaflow concept so far is presented in several conference papers and it is believed more optimization of networks and interconnections increases the market for controllable devises such as Dynaflow.

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PART II
TOPOLOGIES, HARMONICS, AND MODELING

CHAPTER 3. VOLTAGE SOURCE CONVERTER (VSC) TOPOLOGIES

The key component of a SSSC is a three phase VSC. There are several different types of VSCs that could be used in SSSC. This chapter will give a brief summary of the types of VSC's.

Traditionally, VA rating increase is accomplished by selecting the most powerful semiconductor devices and use device series connection to increase the voltage. More recently, series connection of converter is becoming more popular than series connecting devices because of the inherent advantage of reduced voltage harmonics. This type of VSC is called multilevel VSC and will be the focus of this chapter.

3.1 MULTILEVEL VOLTAGE SOURCE CONVERTER TOPOLOGIES

The behavior of multilevel converters can be summarized by examining the behavior of how the output voltage is synthesized from a constant capacitor voltage (DC bus). The first type of capacitor-voltage synthesized-based multilevel converter is called a diode-clamped multilevel converter. The second type of capacitor-voltage synthesized-based multilevel converter is called a flying-capacitor multilevel converter. Finally, the last major type of capacitor-voltage synthesized-based multilevel converter is a cascaded converter with separate DC sources.

3.2 DIODE-CLAMPED MULTILEVEL CONVERTER

The diode-clamped multilevel converter (DCMC) makes use of capacitors in series to divide the DC bus voltage into a distinct set of voltage levels. For example, in order to produce a *m*-level phase voltage, a diode-clamped inverter needs *m*-1 capacitors on the DC bus. A three-phase, five-level diode-clamped inverter is shown in Figure 3.1. The DC bus consists of four capacitors: C_1, C_2, C_3, and C_4. For a DC bus voltage V_{dc}, the voltage across each capacitor is divided by the number of DC bus capacitors. The device voltage stress will be limited to one capacitor voltage level or $V_{dc}/4$, through clamping diodes [3.1-3.4].

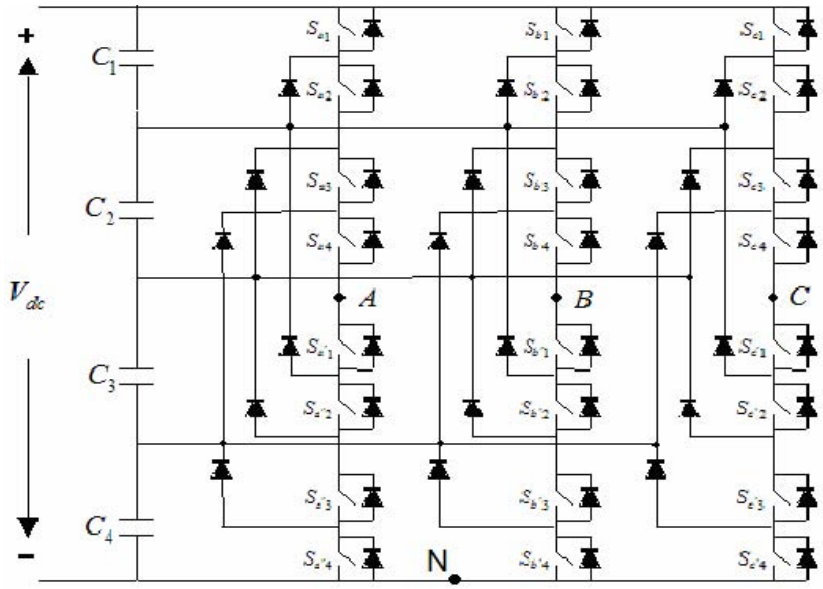

Figure 3.1 A three-phase, five-level diode-clamped converter

In order to explain how the staircase-shaped converter output voltage is synthesized, the neutral point N is used as the reference point for the converter output phase voltage. Using the five-level converter shown in Figure 3.1, there are five possible switch combinations that can be used to generate a five level voltage from point A to point N. Table 3.1 is used to illustrate the five possible switching states of the converter as well as their corresponding output phase voltage [3.1-3.4].

From Table 3.1, a 1 is used to represent a condition when the converter switch is on, and a 0 represents a condition when the converter switch is off. For each phase leg, a set of four adjacent switches is on at any given time. There are four complementary switch pairs in each phase, i.e., S_{a1}-$S_{a'1}$, S_{a2}-$S_{a'2}$, ..., and S_{a4}-$S_{a'4}$ [3.1-3.4].

Table 3.1
Diode-clamped five-level converter voltage levels and their switch states

Output V_{AO}	Switch State							
	S_{a1}	S_{a2}	S_{am-1}	S_{am}	$S_{a'1}$	$S_{a'2}$	$S_{a'm-1}$	$S_{a'm}$
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_3=V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2=V_{dc}/4$	0	0	0	1	1	1	1	1
$V_1=0$	0	0	0	0	1	1	1	1

3.3 FLYING-CAPACITOR MULTILEVEL CONVERTER

A flying-capacitor multilevel converter (FCMC), as shown in Figure 3.2, makes use of a ladder type structure of DC capacitors. The voltage across each capacitor differs from the voltage on the next capacitor. In order to generate an *m*-level staircase output voltage, *m*-1 capacitors in the DC bus are needed. The structure of each phase leg is the same. The size of the voltage increments between two capacitors is used to determine the number of levels of the converter's output voltage [3.5-3.8].

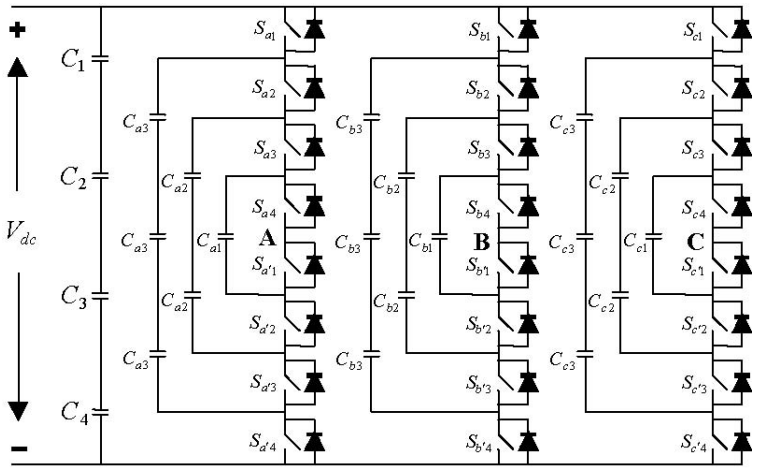

Figure 3.2 A three-phase, five-level flying-capacitor converter topology

Figure 3.2 shows three inner capacitors (C_{a1}, C_{a2} and C_{a3}) in phase A that are used for voltage balancing purposes. It must be noted that the capacitors used for voltage balancing purposes are different from phase to phase whereas all three phases of the flying-capacitor topology share the same DC link capacitors. Table 3.2 shows one possible combination for the switching states of the flying-capacitor topology. It must be noted that there is more than one possible set of switch combinations that can generate the desired converter output voltage. Due to this fact, the FCMC has more flexibility than the DCMC [3.5-3.8].

Table 3.2
A possible switch combination of the voltage levels and their corresponding switch states (flying capacitor)

Output V_{AO}	Switch State							
	S_{a1}	S_{a2}	S_{am-1}	S_{am}	$S_{a'1}$	$S_{a'2}$	$S_{a'm-1}$	$S_{a'm}$
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	1	1	1	0	1	0	0	0
$V_3=V_{dc}/2$	1	1	0	0	1	1	0	0
$V_2=V_{dc}/4$	1	0	0	0	1	1	1	1
$V_1=0$	0	0	0	0	1	1	1	1

3.4 CASCADED-MULTILEVEL CONVERTERS

Finally, the last major type of capacitor-voltage synthesized-based converters discussed is the cascaded multilevel converter (CMC). The CMC consists of several cascaded identical converters with separate DC sources. The primary function of the CMC is to synthesize a desired output voltage from the separate DC voltage sources. There are several different types of DC sources that can be used in the CMC, such as batteries, fuel cells, and solar cells. For SSSC application, only a capacitor is needed since no real power exchange is expected with the line. One of the most popular applications of the CMC is the high-power AC power supplies and adjustable-speed motor drives. One of the benefits of this converter topology is that the multilevel topology eliminates the use for any additional clamping diodes or voltage balancing capacitors. Figure 3.3 shows a diagram of a single-phase CMC [3.9-3.35].

Each single-phase CMC is associated with a number of identical H-Bridge converters. The converter output voltages of each H-Bridge converter are connected in series with one another in the same phase. If the switch combinations of switches S_1-S_4 are varied, it is possible to generate three different converter output voltage levels ($+V_{dc}$, $-V_{dc}$ and 0). For the CMC topology, the number of output phase-voltage levels is defined as m = 2N+1, where N is the number of separate DC sources [3.9-3.35].

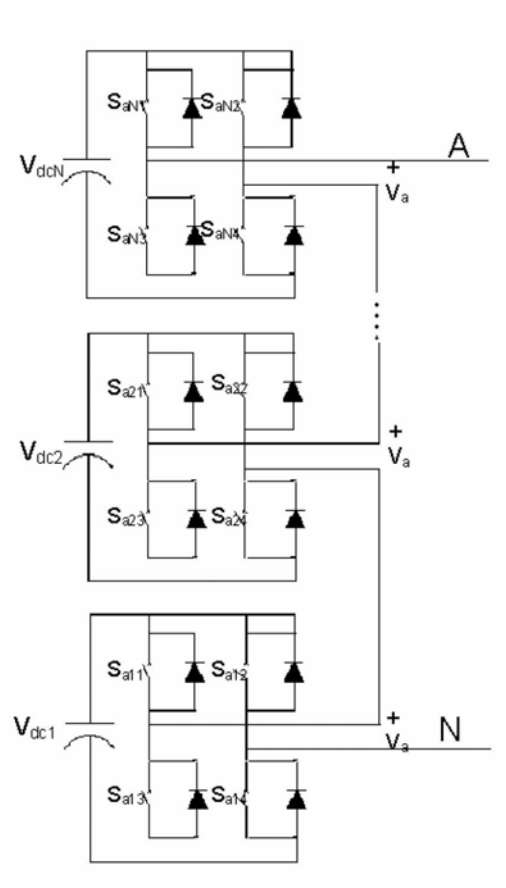

Figure 3.3 Single-phase structure of the cascaded-multilevel converter

For a three-phase system, the output voltage of the three cascaded inverters can be connected in either wye or delta configurations. A wye-configured m-level converter using a CMC with separated capacitors is shown in Figure 3.4.

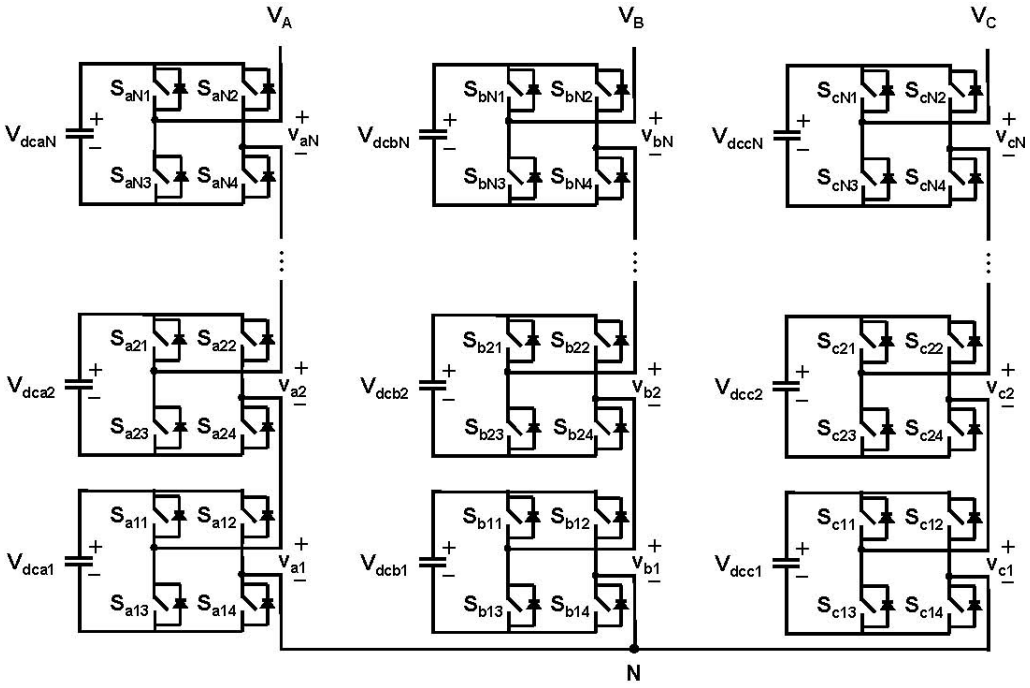

Figure 3.4 A general three-phase wye-configuration CMC

3.5 SSSC BASED ON CMC

Multi-level VSCs were developed to overcome the inadequacy in power semiconductor voltage ratings so that they can be applied to high-voltage electrical systems such as FACTS and custom power system applications [3.12] and [3.36]. Figure 3.5 shows again the three well-known multi-level voltage source converter topologies discussed above. According to [3.37] and [3.38], for reactive power compensation or in the case of the SSSC, reactive voltage support, the CMC with separate dc capacitors is the most favorable topology. The CMC topology does not need clamping diodes and the balancing capacitors that the diode clamped converter and the flying capacitor converter need. For this reason, the CMC requires fewer primary components. The CMC is constructed by identical converter modules. For example, for a three-phase, three-level SSSC, there would be three identical converters needed for each phase. Thus, the desirable amount of reactive voltage support for the SSSC can be adjusted by simply connecting different numbers of the identical hardware modules together. The primary disadvantage of the diode-clamped topology and the flying-capacitor topology is that the same layout cannot be used to expand the converter to higher power levels. Extra clamping diodes and balancing capacitors are needed for these topologies.

Figure 3.6 shows a diagram of a seven-level CMC connected in series with the power grid to illustrate what a CMC-based SSSC might look like. Three H-bridge converters are used in each phase, hence a total of nine H-bridge converters are used. In Figure 3.6, a three-phase coupling transformer is used. Two purposes are served by the transformer: provide voltage isolation between the power grid and the power converter, and provide voltage and current scaling. A practical system will also include a by-pass switch across the transformer to allow operation of the line when the SSSC is not used or taken out for service.

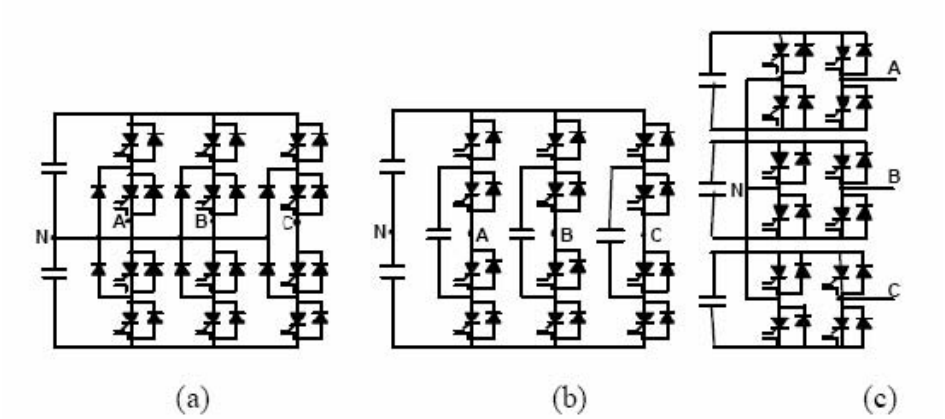

Figure 3.5 Three types of three-phase multi-level voltage source converters: (a) diode-clamped converter, (b) flying capacitor converter, and (c) cascaded converter

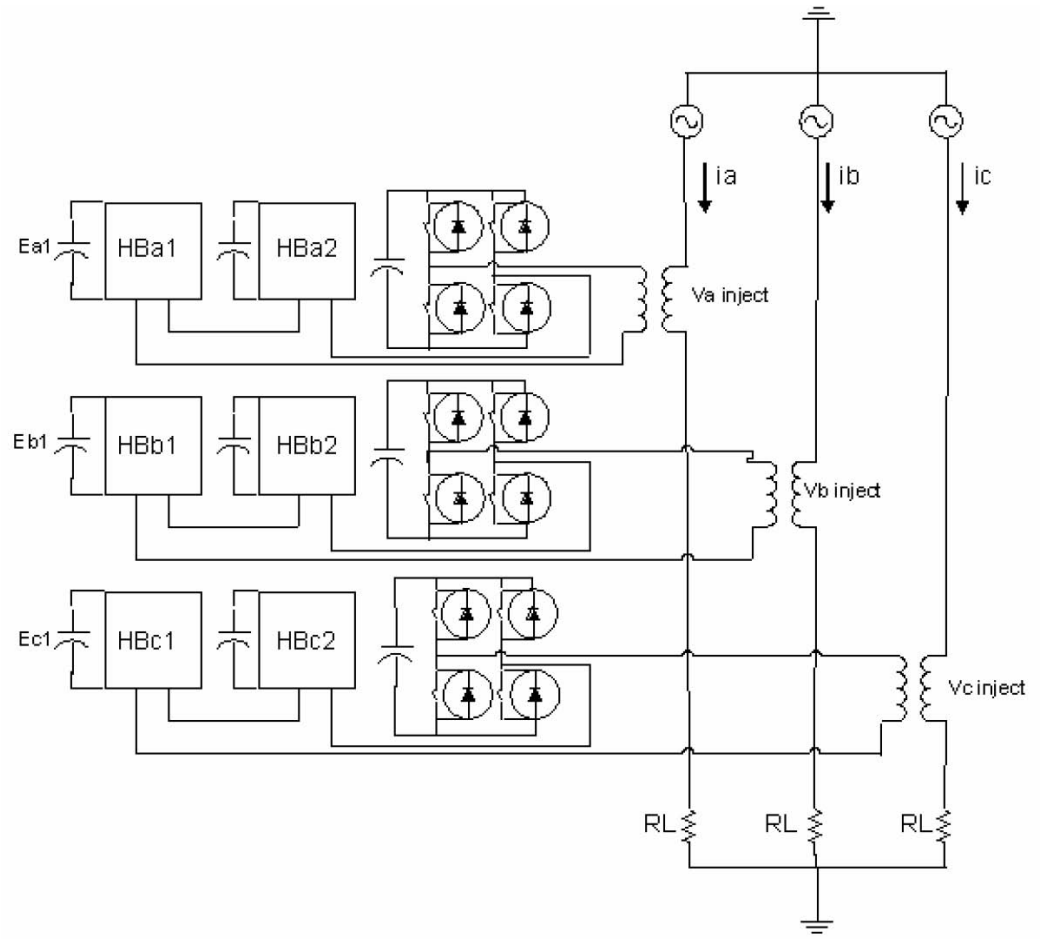

Figure 3.6 Seven-Level Cascaded Multi-Level Converter Configured as a SSSC

3.6 SINUSOIDAL OUTPUT GENERATION IN CMC

There are three ways that the CMC can generate good sinusoidal output waveforms with low harmonics. First, the switching frequency is kept low (e.g., 60 Hz) and is constant for all H-bridge converters, but more H-bridge converters are used to decrease the total harmonic distortion (THD) in the output waveforms. This accomplishes two objectives: first, the switching loss of the power switch is minimized and second, the output voltage THD is also minimized. This method also results in increased output voltage. Hence, the total VA rating increases linearly with the number of H-bridge converter. Second, the number of converter levels is kept constant and the switching frequency is increased to reduce the output voltage harmonics. For this approach, the limiting factor is the increased switching loss in the power semiconductor devices that are ultimately limited by the maximum thermal handling capability of the cooling system. Third, the number of converter levels is increased as well as the switching frequency [3.39-3.43]. For practical purposes the first approach is more suitable for high-voltage applications such as SSSC.

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CHAPTER 4. BASIC VSC STRUCTURES FOR SSSC AND HARMONIC GENERATION

4.1 INTRODUCTION

This chapter presents some discussion on Voltage-Sourced Converters (VSCs) [4.1] for SSSC applications. It is not a complete review, but tries to present the basic characteristics, issues, and possibilities.

Figure 4.1 (a) shows an ideal static synchronous series compensator (SSSC) modeled as a controllable voltage source V_q connected in series with a lossless ac transmission line. In this figure, V_S and V_R are the sending-end and receiving-end transmission line voltages, respectively, I is the line current and X_L is the ac line equivalent reactance (Ω). The by-pass switch Sw provides an alternative path to the load current when the SSSC is out of operation.

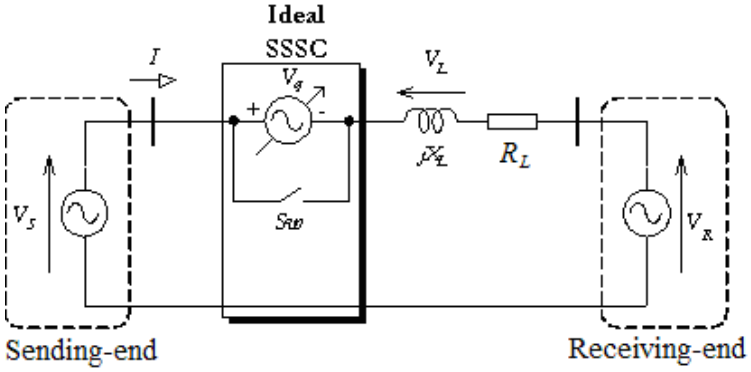
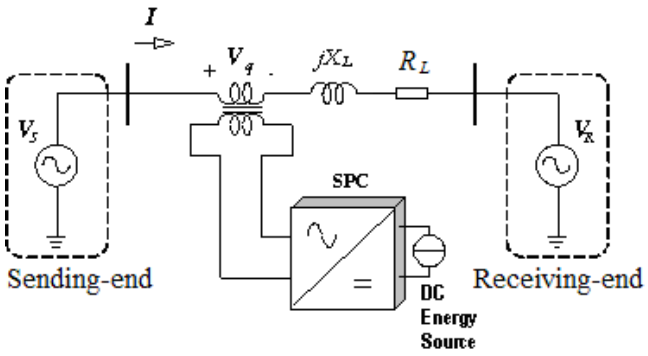


Figure 4.1 Single-line diagram of lossless transmission ac line with an ideal SSSC

In Figure 4.2(a) the ideal SSSC was replaced by a Static Power Converter (SPC). The SPC has its AC terminals connected with the transmission line by a series transformer and its DC terminals connected to a DC source. Ideally the SSSC can synthesize any series compensation voltage if the maximum converter output voltage and current is not exceeded. The type of the DC source, showed in Figure 4.2(a), will be used to classify the static converter. This classification will be discussed in the next section. Figure 4.2 (b) and (c) show two operating conditions where the series voltages generated by the SSSC are $\mp\pi/2$ rad phase-shifted with respect to the line current, respectively. In the Figure 4.2 (b) the voltage V_q lags the line current I by $\pi/2$ rad. In this case the SSSC can be viewed as a series capacitor bank, compensating the transmission line reactance voltage drop, consequently increasing the transmitted power. In the other case, Figure 4.2 (c), the voltage V_q leads the line current I by $\pi/2$ rad. Thus, the SSSC operates as a reactor bank in series with the ac line, decreasing the transmitted power.



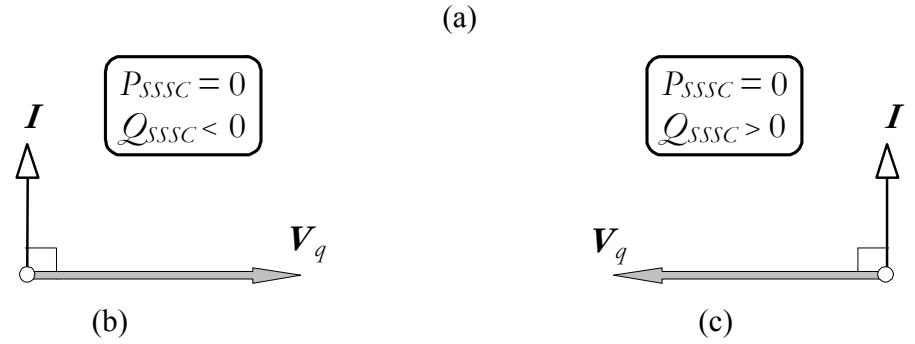


Figure 4.2 (a) Equivalent single-line diagram of the SSSC; (b) phasor diagram for capacitive compensation characteristic and (c) for inductive compensation characteristic

In Figure 4.2, the SSSC does not absorb or supply real power in series with the ac transmission line. However, the series compensating voltage might have its phase continuously varied to force the SSSC to absorb or to supply small amount of real power in series with the ac line. This characteristic is necessary to control the energy stored in the DC link of the SPC to vary the magnitude of series voltage V_q, considering that the DC energy source shown in Figure 4.2 is a capacitor or a reactor. Figure 2 shows four possible phasor diagrams for the SSSC series voltage and the line current. In the first and fourth quadrants the SSSC is absorbing while in the second and third quadrants it is supplying real power to the power system. Because the reactive power can be controlled independently of the SSSC real power, in the first and second quadrants the SSSC operates with an inductive characteristic (V_q leads I) and in the third and fourth quadrants it has a capacitive compensation characteristic (V_q lags I).

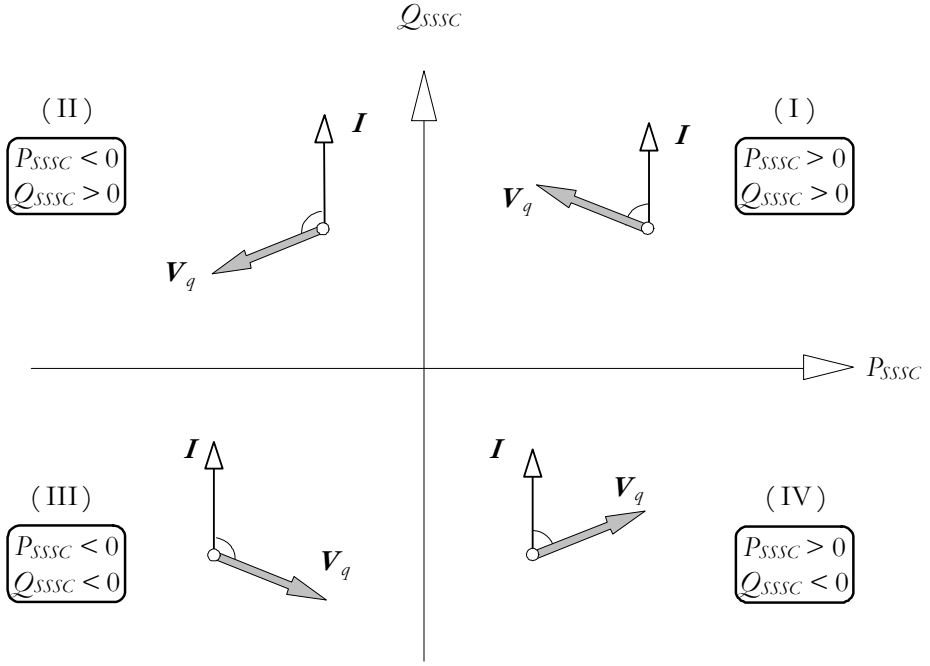


Figure 2.3 SSSC operating characteristics: quadrants (I) and (IV) SSSC absorbing real power; quadrants (II) and (III) SSSC supplying real power; quadrants (I) and (II) SSSC with inductive reactive power; and quadrants (III) and (IV) SSSC with capacitive reactive power

4.2 FORCED-COMMUTATED DC-AC STATIC CONVERTERS

Forced-commutated DC-AC static converters are power electronic devices that use in their structure self-commutated semiconductor switches. These semiconductor switches can be turned on and turned off through electrical signals applied to their gate terminals. They are also called inverters in the literature and they can be classified as voltage-sourced or current-sourced type converters.

The Voltage-Sourced Converter (VSC) has a unidirectional voltage source connected to its DC terminals while the Current-Sourced Converter (CSC) has its DC terminals fed by a unidirectional current source. Since the forced-commutated switches turn-on and turn-off times are electrically controlled, the VSC and CSC can be viewed as an equivalent independent voltage or current source, respectively, working with bidirectional real and reactive powers flow on their AC terminals.

As mention above, the DC link source of the VSC imposes a unidirectional voltage across the converter semiconductor switches. Thus, reverse biased diodes should be connected in parallel with each converter forced-commutated switch making all of them bidirectional for current flow. Figure 4.4 shows an example of a switch consisting of a GTO Thyristor anti-parallel to a diode. However, others types of switches could be based on IGBT or IGCT. This characteristic assures that the real and the reactive powers could flow from/to the converter terminals to/from the power system. On the other hand, in the CSC, if the forced-commutated switches have no reverse voltage blocking capabilities, diodes should be connected in series with them to guarantee bidirectional voltage characteristic for the switches, because the DC current source at the DC link is unidirectional.

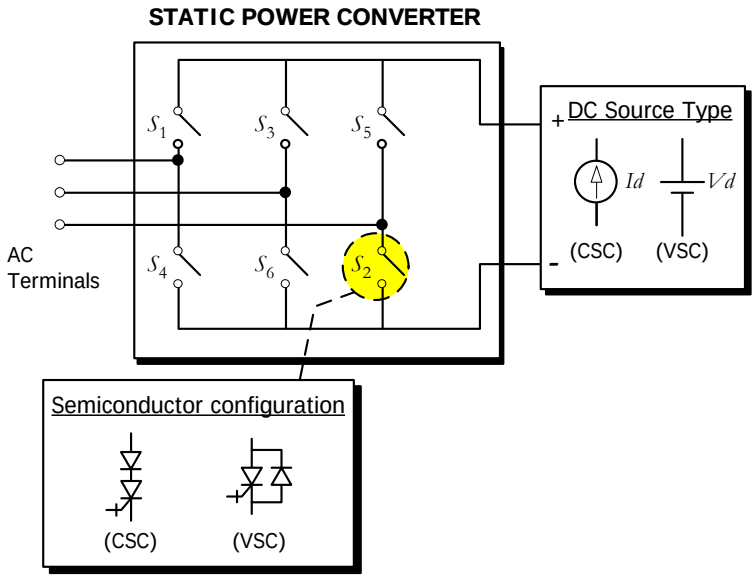


Figure 4.4 Basic structure of a three-phase dc-ac static forced-commutated converter

Ideally, both VSC and CSC converter types could be used in high power applications. However, the CSC has a lower efficiency because of the losses due to the flow of DC current through the converter semiconductor switches. These losses are higher in view of the fact that the DC link current should have its maximum value even when the converter output load is low. Thus from this point on, only VSC will be considered to synthesize the SSSC. This tendency is also observed in the design of other high-power FACTS devices reported in the literature and actually in operation **Erreur ! Source du renvoi introuvable.**.

4.3 BASIC VSC TOPOLOGY

Figure 4.5 shows the basic topology of a three-phase VSC (VSC-3ϕ). The VSC-3ϕ has six forced-commutated switches (e.g., GTOs, but could be IGBT or IGCT). In high power applications, each forced-commutated switch with its reverse biased diode, shown in this figure, is formed by the connection of many lower capacity semiconductor devices in series and in parallel. The DC energy source shown in Figure 4.2 is replaced by a charged DC capacitor. This changing is possible because the converter will generate or absorb only reactive power in its AC terminals.

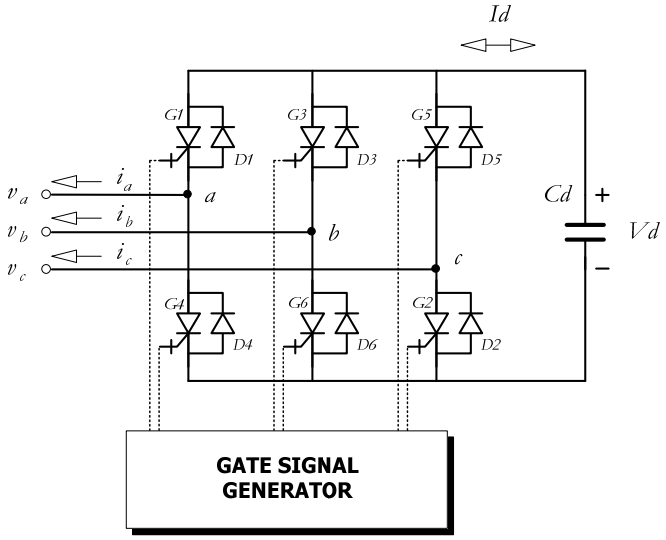


Figure 4.5 Basic topology of a three-phase VSC (VSC-3ϕ)

If the converter has to absorb a large amount of real power in its AC terminals, an energy dissipation scheme should be connected at the converter DC terminals in such a way as to maintain the DC link voltage constant or within the limits that would not affect the semiconductor switches. Otherwise, if the real power absorbed in a given time interval is to be returned to the AC system during the next cycles, the VSC ought to be designed with an energy storage system which could be, for example, a large DC capacitor bank or batteries.

Ideally, the semiconductor switches of the same VSC branch are controlled in complementary manner. Thus, when the switch in the upper side of the branch is turned on the switch in the lower side is turned off and vice-versa. However, in practical applications, there is a small transition period during that both semiconductor switches are blocked. That is, one switch will not conduct until the other goes to off-state. This procedure assures that the DC capacitor will not be short circuited damaging the VSC semiconductors.

Figure 4.6 and 4.7 show two connection schemes for a VSC-3ϕ. The secondary side terminals of the transformers could be connected in wye (Y) or delta (Δ) while the primary coils have their terminals series connected with the AC transmission line. The signals P_{ref} and Q_{ref} are the real and reactive power references that the SSSC should control in series with the AC line. It is also possible to operate the SSSC to inject a constant voltage V_q or to emulate a constant reactance X_q in series with the compensated AC line.

In these figures the by-pass switches could be formed by the connection of two thyristor valves in anti-parallel. They provide a path to the currents to flow in the secondary coils of the transformers when the gate signals of the semiconductor switches of the VSC are blocked. However, if the SSSC is to stay out of operation for a long period of time, mechanical switches connected in parallel with primary terminals of the transformers should be design to by-pass the SSSC. Surge arresters and metal oxide varistor (MOV) should also be designed to be connected in parallel with the SSSC to protect the semiconductor against power system over voltages.

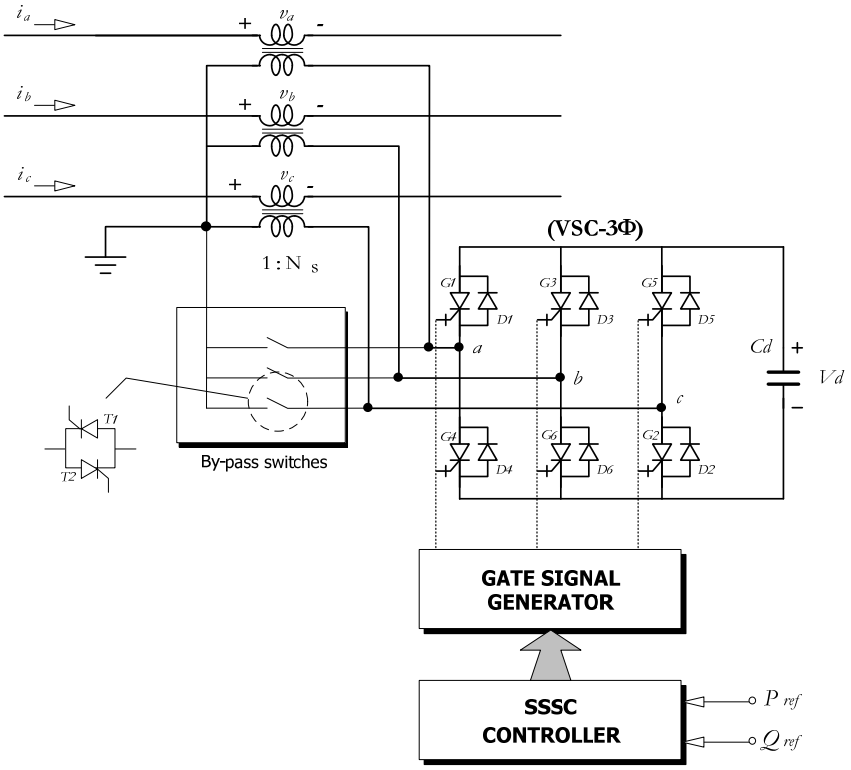


Figure 4.6 Wye (Y) transformer configuration for the connection of the SSSC

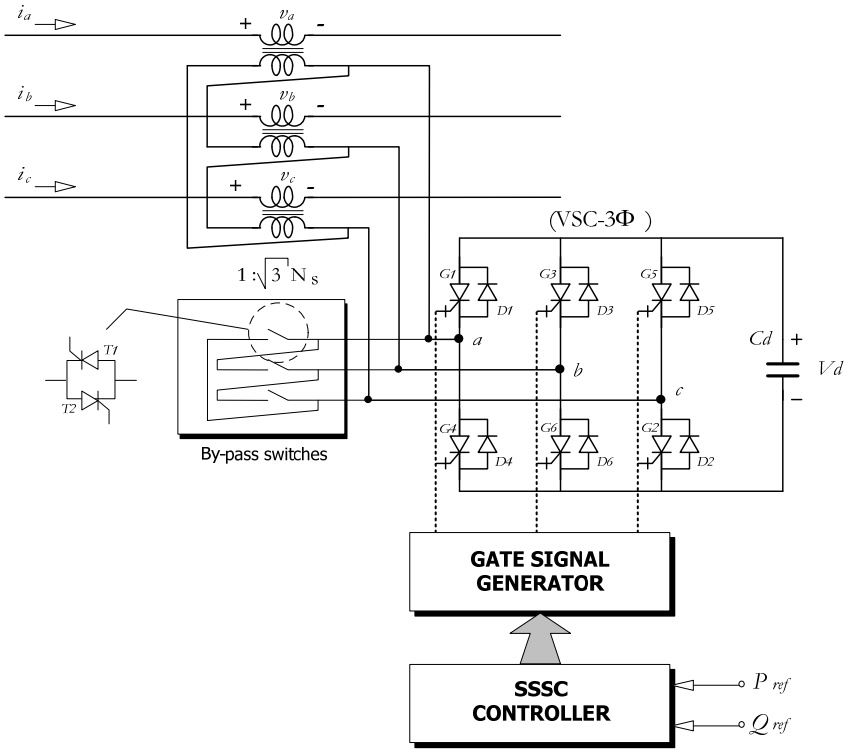


Figure 4.7 Delta (Δ) transformer configuration for the connection of the SSSC

An alternative to the SSSC synthesis is the utilization of three single-phase converters (VSC-1ϕ), with their DC terminals connected in parallel to the same DC capacitor Cd, as shown in Figure 4.8. However, it has the ability of an independent control of each series compensating voltage. It also does not need any by-pass switch when the SSSC is out of operation. An alternative path for the current could be obtained, for example, by turning on both upper and blocking both lower semiconductor switches of each VSC-1ϕ as shown in Figure 4.9 for phase "a".

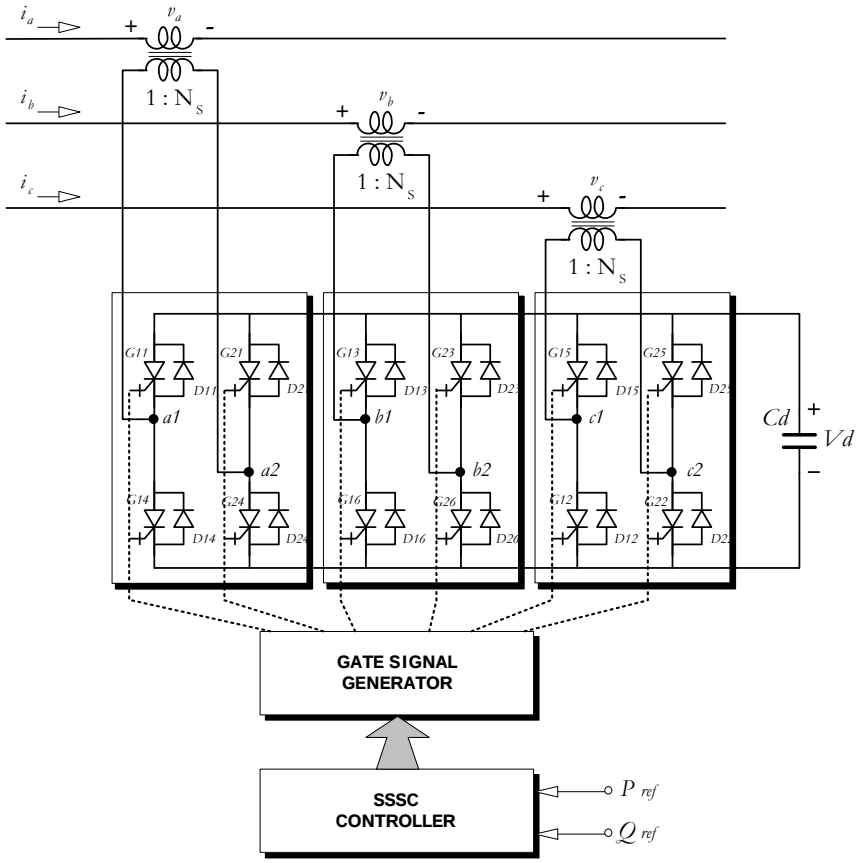


Figure 4.8 SSSC configuration based on the connection of three single-phase VSC

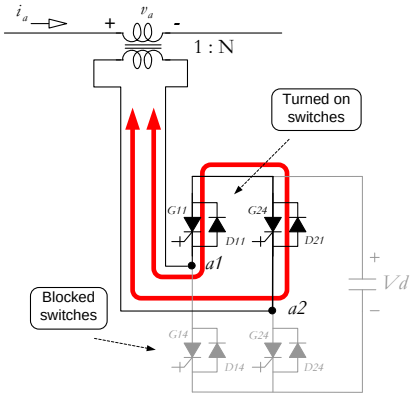


Figure 4.9 Phase "a" scheme for the SSSC out of service

4.4 BASIC VSC SWITCHING STRATEGIES

Considering the switching frequency strategy used to control the output voltages of the VSC topologies, presented in the previous section, they can be classified as in Table 4.1.

Table 4.1 VSC switching frequency classification

1. Pulse Width Modulation VSC (VSC - PWM);
2. Square wave VSC (or 6-pulse VSC).

4.4.1 Pulse Width Modulation VSC (VSC-PWM)

In the pulse width modulation (PWM) technique, the VSC semiconductor switches are turned on and off many times per cycle of the fundamental voltages generated by the VSC. The continuous control of the on and off periods of the VSC semiconductor switches makes it able to generate ac output voltages, with controllable magnitude, phase, and frequency, from a DC voltage

Anticipating that semiconductor forced-commutated switches will be used to design high-power and high-frequency PWM converters, many researchers have proposed FACTS devices models, based on VSCs that switch with frequencies around 1 kHz [4.5-4.7]. These high-frequency PWM strategies generate high-order harmonics that are easily filtered with small passive filters. Table 4.2 classifies the PWM control strategies according to their basic characteristics.

Table 4.2 Classification of PWM strategies.

1.	Fixed (or constant);
2.	Programmable;
3.	Real time.

In the fixed PWM scheme the VSC works with a fixed number of commutations per cycle. The switching frequency of the semiconductor devices is normally generated by a voltage oscillator.

The programmable PWM scheme groups the methods that use selective harmonic elimination (SHE) or harmonic minimization techniques. In this scheme the switching angles are calculated to cancel one or more harmonics or to reduce the total harmonic distortion at the VSC output terminals. These angles are stored in non-volatile memory.

In the real-time PWM scheme, the turn-on and turn-off times of the semiconductor switches are determined "*on-line*" through the comparison of a reference voltage with a carrier wave. This scheme groups the Sinusoidal PWM (SPWM), the digital sampled PWM, and the Space Vector PWM (SVPWM), among others. In contrast with the fixed and programmable modulation schemes, that have good results in steady state, the real-time PWM scheme presents better results in transient situations while it may have more switching losses in steady state.

4.4.2 Sinusoidal PWM

Figure 4.10(a) shows an example of this method where a triangular carrier wave (v_{tri}), with peak value equal to V_{tri} and angular frequency ω_S (rad/s), is compared with a reference sinusoidal voltage (v^*), with peak value equal to V_{ref} and angular frequency ω (rad/s), that is the output voltage that the SSSC has to generate in series with the AC line. Figure 4.10 shows the synthesized output VSC voltage considering for V_{ref} = 1 pu, V_{tri} = 1 pu, V_d = 1 pu, and $\omega_S = 9\omega$ (rad/s).

Considering the configuration for the DC capacitor as shown in Fig. 4.10, the output phase "a" of the VSC could be written as

if $v^* \geq v_{tri}$,

$$v_{ao} = +\frac{V_d}{2}, \tag{4.1}$$

and, if $v^* < v_{tri}$,

$$v_{ao} = -\frac{V_d}{2}. \tag{4.2}$$

Defining the amplitude modulation index (m_a) as

$$m_a = \frac{V_{ref}}{V_{tri}} \tag{4.3}$$

and the frequency modulation index (m_f) as

$$m_f = \frac{\omega_s}{\omega} = \frac{f_s}{f}, \tag{4.4}$$

the fundamental frequency output voltage within the VSC output switched voltage shown in Figure 4.10(b) is given by

$$v_{ao} = m_a \frac{V_d}{2} \sin(\omega t + \theta), \tag{4.5}$$

where f_S is the triangular carrier frequency (Hz) and f is the reference voltage fundamental frequency (Hz).

The voltages at phases "b" and "c" are similar to that shown in Figure 4.10(b) as given by (4.5) but phase-shifted by -2π/3 and -4π/3 rad, respectively.

In the simulation result presented in this and the following sections, it is assumed that the DC capacitor is large enough to keep a DC voltage free of ripple. The DC voltage without ripples is important to guarantee non-characteristic harmonic content in the VSC output voltages. Also series inductances, connected to each converter phase, are used to diminish the transients due to the switches commutations. These inductances were not drawn in the circuits of the VSCs presented in previous figures for simplicity. In practical applications these inductances can be the leakage inductances of the series connection transformers.

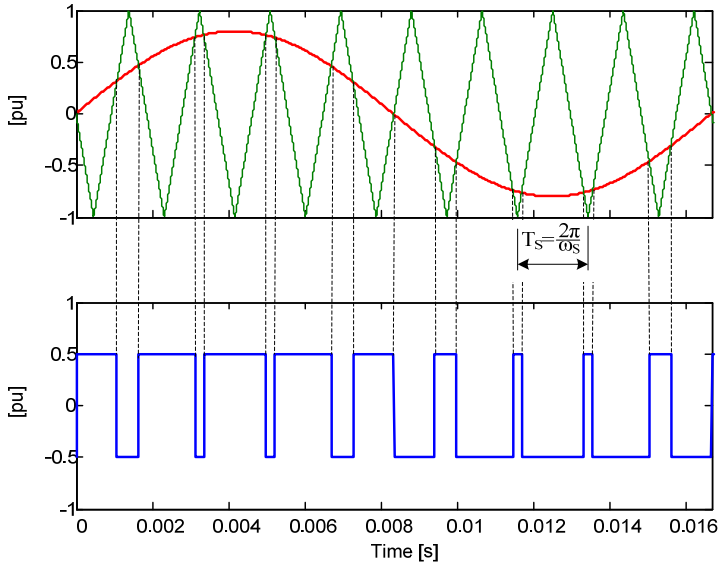


Figure 4.10 Triangular carrier wave (v_{tri}) and sinusoidal reference voltage (v^*); (b) output voltage (v_{ao}) for $m_a = 1.0$ and $m_f = 9.0$

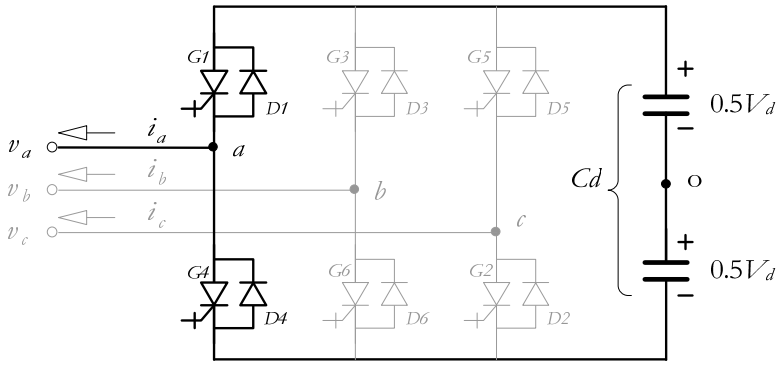


Figure 4.11 Phase "a" of three-phase VSC branch

4.5 VSC-3ϕ WITH SINUSOIDAL PWM

Figure 4.12 shows three-phase sinusoidal reference voltage (v_a^*, v_b^*, and v_c^*) with angular frequency ω (rad/s). The set of reference voltage is compared with only one triangular carrier wave. This procedure helps to cancel some harmonics in the VSC output voltages.

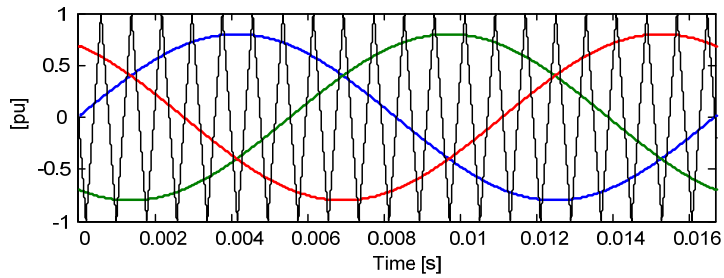
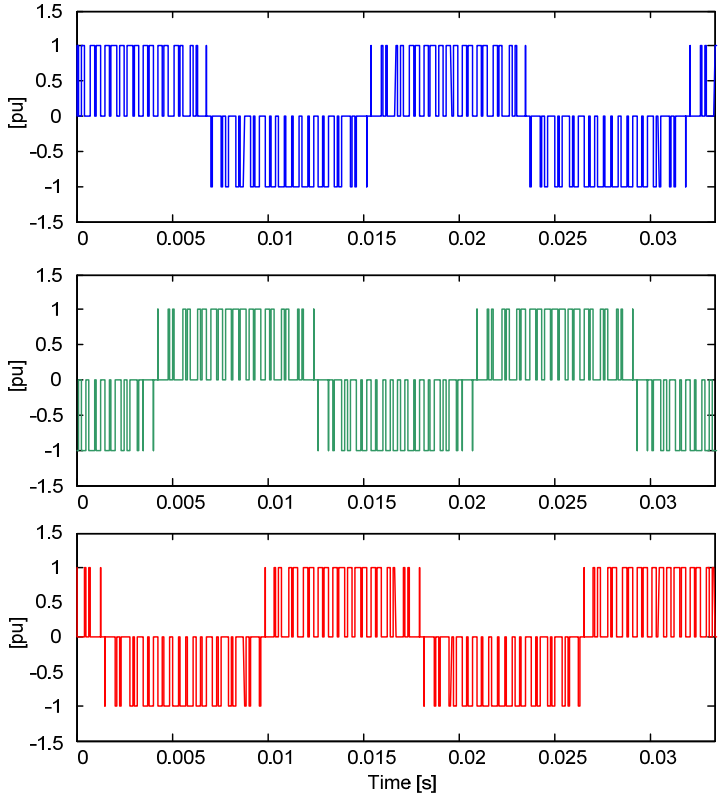


Figure 4.12 Reference voltages and triangular carrier wave ($m_a = 0.8$ and $m_f = 21$)

In Figure 4.13(a), (b) and (c), the line-to-line output voltages of the VSC-3ϕ are obtained from the difference of the terminals voltages of phases "a" and "b", "b" and "c", "c" and "a", respectively. These results were obtained for: ω = 120π rad/s (f = 60 Hz), m_a = 0.8, and m_f = 21.



(a)

(b)

(c)

Figure 4.13 VSC line-to-line output voltages: (a) v_{ab}, (b) v_{bc}, (c) v_{ca}

From (4.5) the fundamental line-to-line output voltages of the VSC-3ϕ can be written as

$$\begin{cases} v_{ab} = (v_{ao} - v_{bo}) = m_a \sqrt{3} \dfrac{V_d}{2} \sin(\omega t + \theta + \pi/6) \\ v_{bc} = (v_{bo} - v_{co}) = m_a \sqrt{3} \dfrac{V_d}{2} \sin(\omega t + \theta - \pi/2) \\ v_{ca} = (v_{co} - v_{ao}) = m_a \sqrt{3} \dfrac{V_d}{2} \sin(\omega t + \theta + 5\pi/6) \end{cases}, \tag{4.6}$$

where θ is a generic phase angle of the synthesize voltages (rad).

Despite of the continuous magnitude control of the output voltages with amplitude modulation index m_a, the line-to-line VSC voltages have harmonics due to the semiconductor switching. Figure 4.14 shows the harmonic spectrum of the VSC output voltage. In this figure there is a fundamental frequency component for m_f = 1 (or 60 Hz). Above this frequency, the harmonics arise as side-bands of the multiples of the switching frequency, that is, $k\omega_s \pm p\omega$ where k and p are positive integers and when k is odd, p is even and vice-versa.

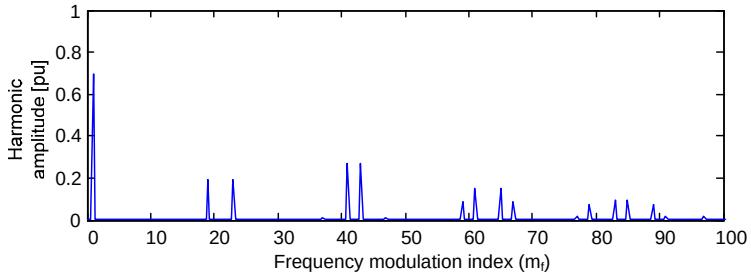
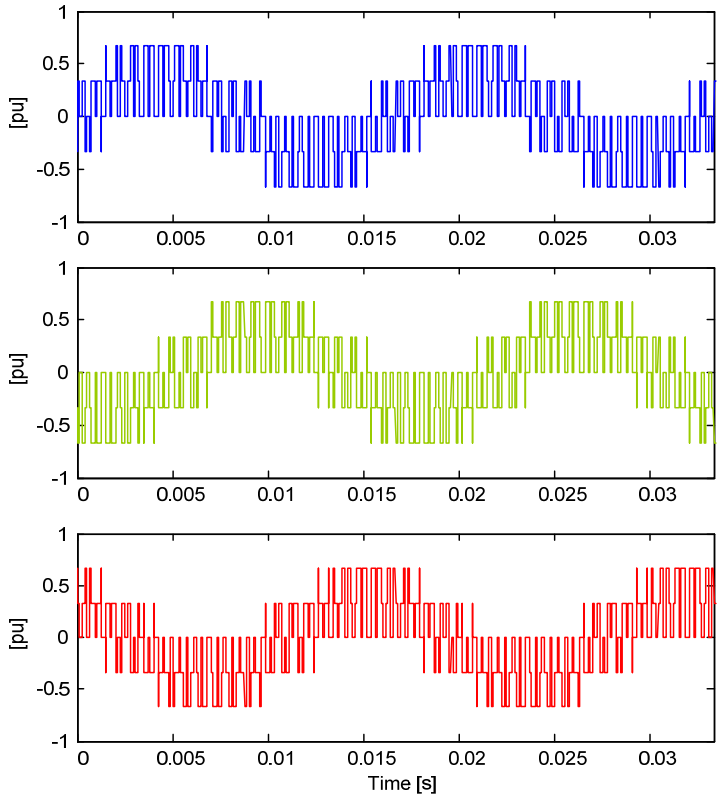


Figure 4.14 Line-to-line voltage harmonic spectrum (m_a = 0.8 and m_f = 21)

Figure 4.15(a), (b) and (c) plots the phase-to-neutral output voltages of the VSC-3ϕ. These voltages are obtained with the VSC connected to an ungrounded wye transformer, as shown in Figure 4.6, or by supplying a wye connected load and assuming ω = 120π rad/s (f = 60 Hz), m_a = 0.8, and m_f = 21.



(a)

(b)

(c)

Figure 4.15 VSC phase output voltages: (a) v_a, (b) v_b, (c) v_c

From (4.6) the fundamental phase voltages of the VSC-3ϕ can be written as

$$\begin{cases} v_{an} = \dfrac{v_{ab}}{\sqrt{3}} = m_a \dfrac{V_d}{2} \sin(\omega t + \theta) \\ v_{bc} = \dfrac{v_{bc}}{\sqrt{3}} = m_a \dfrac{V_d}{2} \sin(\omega t + \theta - 2\pi/3). \\ v_{ca} = \dfrac{v_{ca}}{\sqrt{3}} = m_a \dfrac{V_d}{2} \sin(\omega t + \theta + 2\pi/3) \end{cases} \tag{4.7}$$

As in the previous case the harmonics of the output voltages arise in side-bands of the multiples of the switching frequency, *i.e.*, $k\, m_f \pm p$ (k = 1, 2, 3 … and p = 1, 2, 3 …), see Figure 4.16. However, in this case the fundamental and harmonics components have their magnitudes reduced by a factor of $\sqrt{3}$. Figure 4.17 shows how the lowest order significant harmonics presented in the VSC output voltages varies as function of the modulation index m_a. Note that the magnitudes of the lowest harmonics have a non-linear behavior.

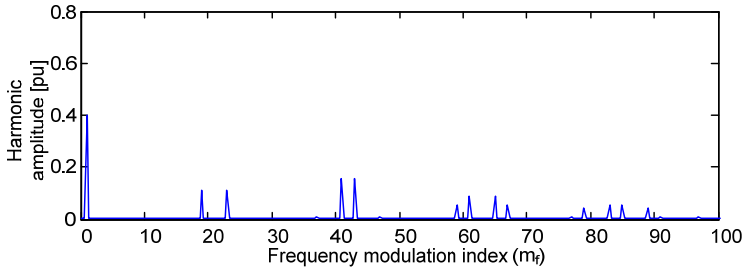


Figure 4.16 Phase voltage harmonic spectrum (m_a = 0.8 and m_f = 21)

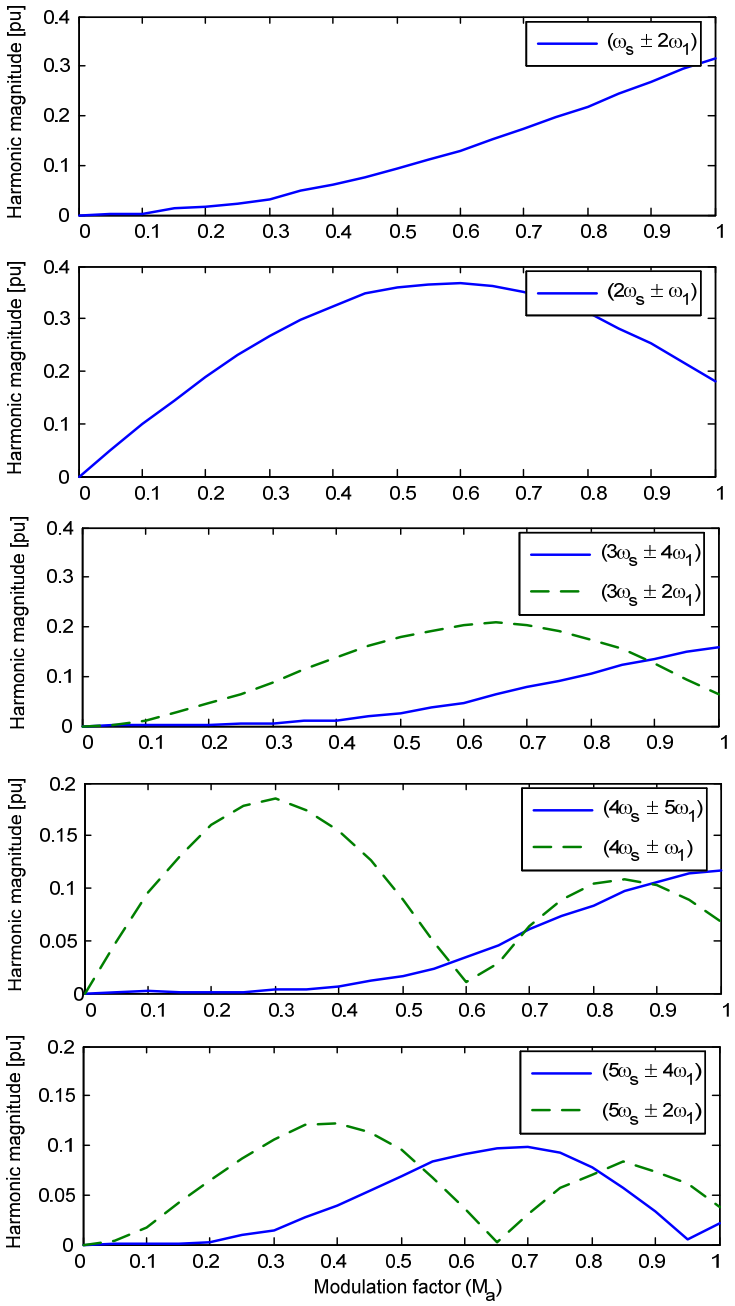


Figure 4.17 Behaviors of the lowest order harmonics in the VSC output phase-to-neutral voltage for the case of sinusoidal PWM

The utilization of a three-phase VSC to synthesize the SSSC has the advantage of needing less semiconductor switches than the single-phase topology shown in Figure 4.8. However, the three-phase topology can have non-characteristic harmonic in their output voltages if the set of reference voltages are unbalanced.

4.5.1 Three-phase VSC transformers connection

The SSSC transformers connect the power system and the VSC, and inject the compensating voltage synthesized by the VSC in series with the transmission line as shown in Figure 4.2(a). Figures 4.18 and 4.19 show two possible configurations where three single-phase transformers, with normalized turn's ratio 1:*N*, have the converter side coils connected in Δ and Y, respectively. Considering the voltages and currents as indicated in Figures 4.18 and 4.19 for steady-state fundamental frequency components, it is possible to conclude that the current through the semiconductor switches for the delta connected transformer is $\sqrt{3}$ times higher than the currents through the transformer coils. In the other case, for the wye connected transformer, the compensating voltage is divided by $\sqrt{3}$. Therefore, the apparent powers at the converter terminals, assuming $0 \le m_a \le 1$, are given by

$$S_{\Delta} = \sqrt{3}\frac{1}{\sqrt{2}}\left(\frac{\sqrt{3}}{2}m_a V_d\right)\sqrt{3}\frac{I_L}{N} \cong 1.837 m_a \frac{V_d I_L}{N}, \tag{4.8}$$

and

$$S_{Y} = 3\frac{1}{\sqrt{2}}\left(\frac{1}{2}m_a V_d\right)\frac{I_L}{N} \cong 1.061 m_a \frac{V_d I_L}{N}. \tag{4.9}$$

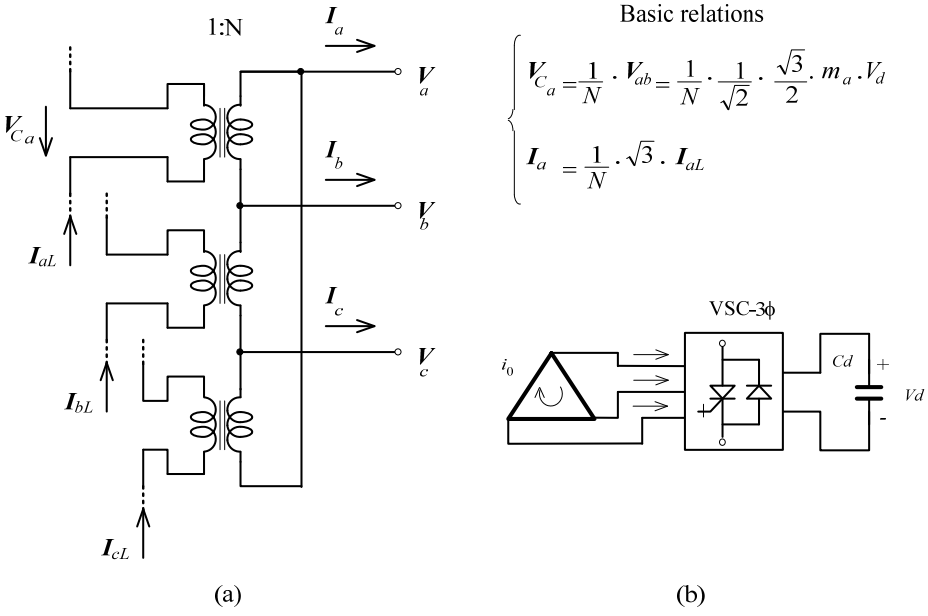


Figure 4.18 (a) Delta connected VSC-3ϕ transformer; (b) simplified diagram

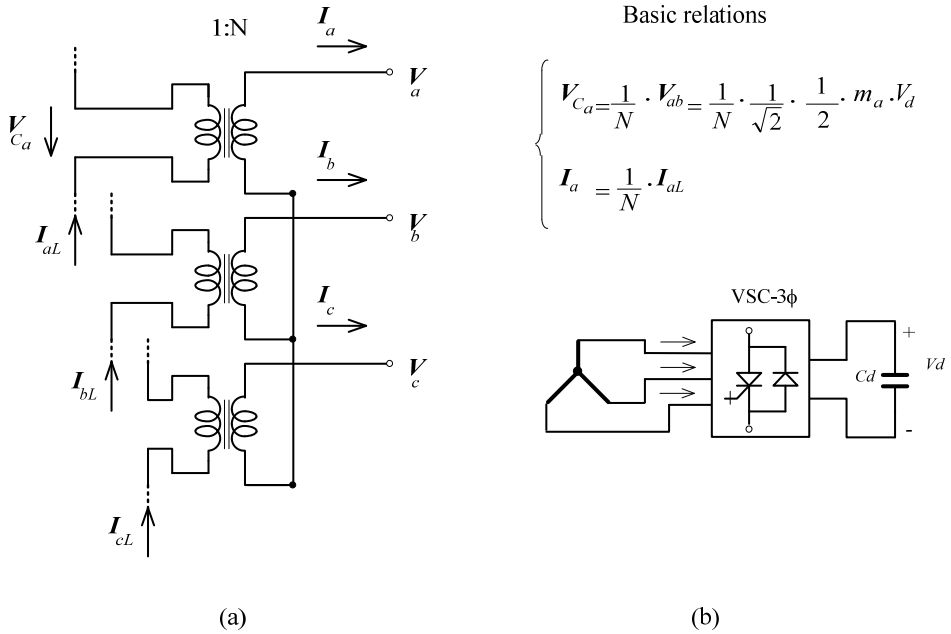


Figure 4.19 (a) Wye connected VSC-3ϕ transformer; (b) simplified diagram

Expressions (4.8) and (4.9) show that, considering the same DC voltage converter V_d, the delta connected VSC-3ϕ injects ($\sqrt{3}$ -1) (approximately 73%) more power in series with the AC line than the wye connected VSC-3ϕ. However its semiconductor switches should be designed to support a current that is $\sqrt{3}$ higher. The delta connected VSC-3ϕ has another interesting characteristic. The delta connected windings provide a natural path for zero sequence current flow as indicated in Figure 4.18, thus blocking it from flowing to the transmission line. This characteristic is important for the case of unbalanced line current operation. If the same characteristic is desired for the wye connected VSC-3ϕ, the neutral node of the transformers should be connected to the midpoint between the VSC DC capacitor. However in this case the zero sequence currents will flow through the DC capacitor and may unbalance the DC voltage in the two capacitors.

The 3×VSC-1ϕ with bipolar output voltage

If each single-phase VSC of Figure 4.8 has its semiconductor branches controlled in a symmetrical way, the output voltages will be switched between $+V_d$ and $-V_d$ and the output voltage waveform is of the bipolar type. Figure 4.20 show the phase "a" VSC output voltage. In this figure $v_{a1} = -v_{a2}$ and the following values were considered: ω = 120π rad/s (f = 60 Hz), m_a = 0.8, and m_f = 21.

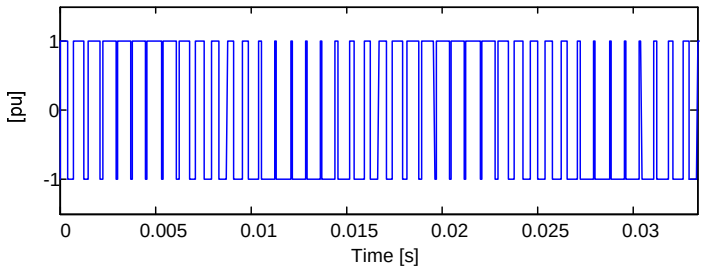


Figure 4.20 Phase "a" output voltage of 3×VSC-1ϕ with bipolar switching scheme (m_a = 0.8 and m_f = 21)

From (4.5) the phase "a" output voltage of 3×VSC-1ϕ is given by

$$v_a = (v_{a1} - v_{a2}) = m_a V_d \sin(\omega t + \theta) \tag{4.10}$$

As in the three-phase configuration the modulation index m_a can be used to control the VSC output voltages. The harmonics become non nulls for frequencies ($k\, m_f \pm p$), where k and p are positive integers and when k is odd, p is even, and vice-versa. Figure 4.21 shows the harmonic spectrum obtained for the voltage shown in Figure 4.20. The magnitudes of the harmonics are normalized in relation to V_d. Figure 4.22 shows how the modulation index m_a affects the most significant harmonics amplitudes for a bipolar switching scheme. The harmonic at the frequency ω_S (rad/s) has the largest magnitude for all m_a between 0 and 1.

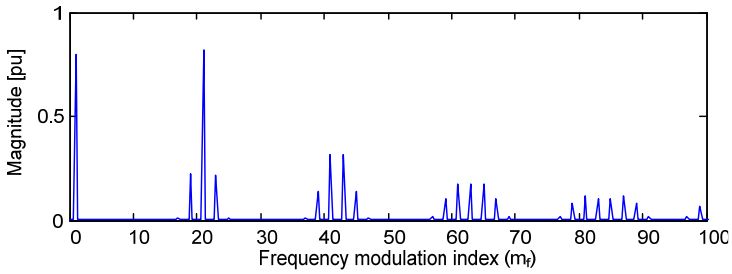


Figure 4.21 Harmonic spectrum of the 3×VSC-1ϕ with a bipolar output voltage (m_a = 0.8 and m_f = 21)

This topology has two times more semiconductor switches and high-amplitude harmonics than the three-phase VSC. The harmonics of each 3×VSC-1ϕ output phase, however, is independent of the switching pattern of the other two converter phases. The reference voltages used to switch the VSC do not need to be balanced and symmetrical.

4.5.2 Three single-phase VSC connection transformers

Figure 4.23 shows the three single-phase transformers used to connect 3×VSC-1ϕ in series with the transmission line. The secondary-side coils of the transformers are connected directly to each single-phase converter. In this figure it is also shown the steady-state relationships of the voltage and current in the primary and secondary sides of the connection transformer considering a 1:N turns-ratio. In this case the apparent power at the converter terminals, assuming $0 \le m_a \le 1$, is given by

$$S_{3\times VSC-1\phi} = 3\frac{1}{\sqrt{2}}(m_a V_d)\frac{I_L}{N} \cong 2.12 m_a \frac{V_d I_L}{N}. \tag{4.11}$$

From (4.11) it is possible to conclude that the power at the 3×VSC-1ϕ output terminals is 15% higher than the output power, given by (4.8), for the delta connected three-phase VSC.

The 3×VSC-1ϕ with unipolar output voltage

In this case the converter branch has their semiconductor switches controlled independently of the state of the others. Two triangular carrier waves, with magnitude V_{tri} and angular frequency ω_S (rad/s), but phase-shifted by π (rad), are used to modulate the reference voltage with magnitude V_{ref} and angular frequency ω (rad/s). Figure 4.24 shows the plots of the two triangular carrier waves and the reference sinusoidal voltage that the converter should synthesize in its terminals. Each triangular carrier wave is used to determine the switching pattern of each VSC-1ϕ branch.

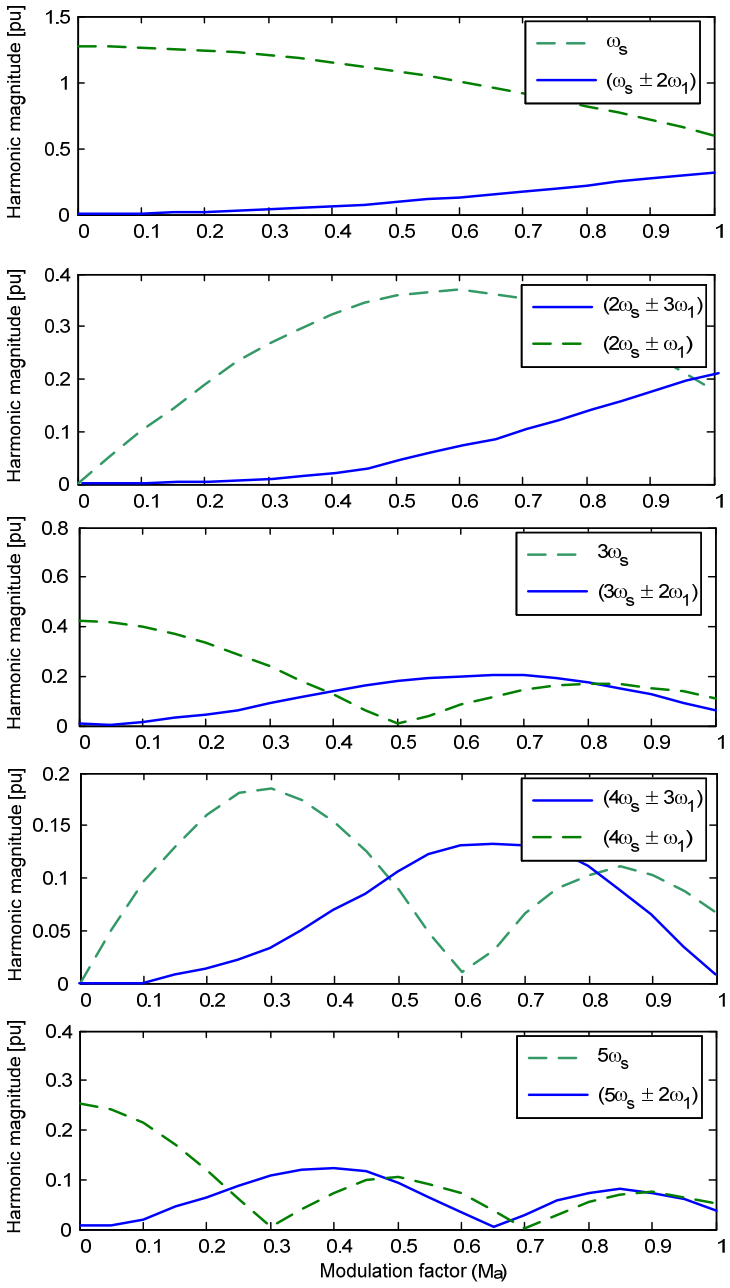


Figure 4.22 Harmonic magnitude behavior of output voltage of 3×VSC-1ϕ with bipolar switching

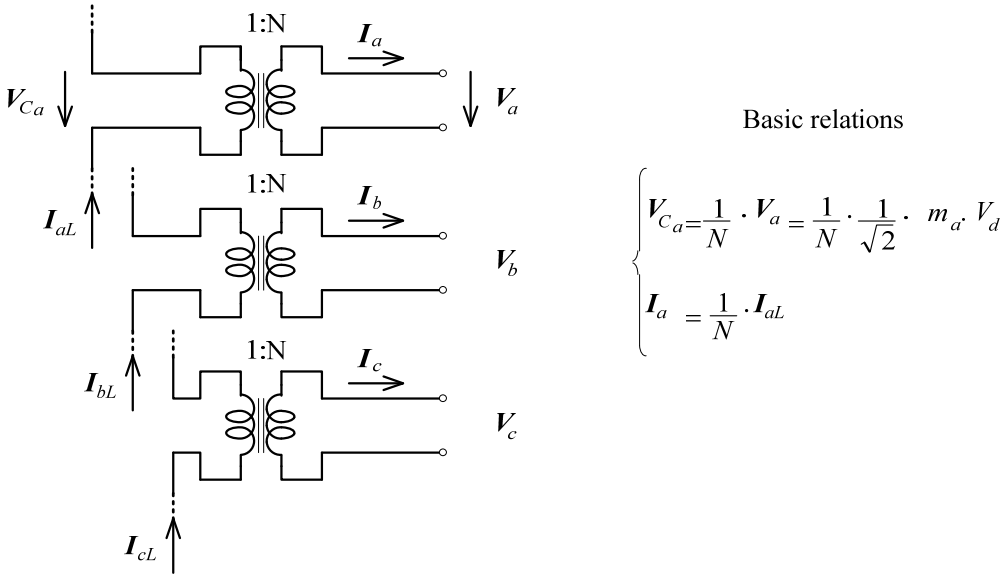


Figure 4.23 Transformer configuration for the connection of 3×VSC-1ϕ

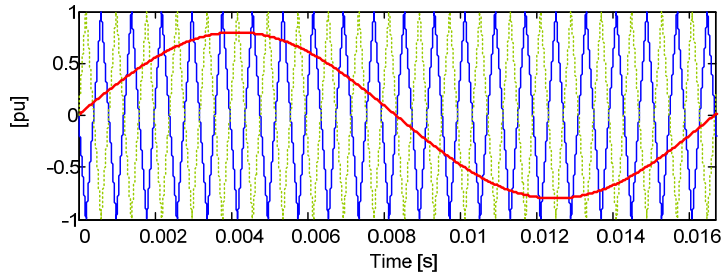


Figure 4.24 Phase "a" reference voltage and triangular carrier waves (m_a = 0.8 and m_f = 21)

Figure 4.25 shows the phase "a" output of a 3×VSC-1ϕ considering ω = 120π rad/s (f = 60 Hz), m_a = 0.8, and m_f = 21. Note that the output voltage is switched between 0 and $+V_d$ for the positive semicycle of the reference voltage and between 0 and $-V_d$ for the negative semicycle of the reference voltage. This voltage waveform is of unipolar type.

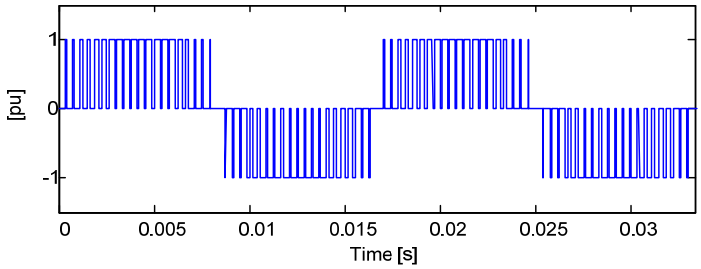


Figure 4.25 Phase "a" output voltage of the 3×VSC-1ϕ for a unipolar switching scheme (m_a = 0.8 and m_f = 21)

The mathematical expression of the fundamental frequency component presented in switched voltage shown in Figure 4.25 can be written as

$$v_a = (v_{a1} - v_{a2}) = m_a V_d \sin(\omega t + \theta) \tag{4.12}$$

Figure 4.26 shows the harmonic spectrum of the unipolar voltage shown in Figure 4.25. The comparison of the spectra in Figure 4.21 and 4.26 shows that the ($k\, m_f \pm p$) harmonics, for k = 1, 3, 5,…, in the unipolar voltage waveform have been canceled. Only the harmonics around the frequency $k\, m_f$, for k = 2, 4, 6,…, have nonzero magnitude.

The lower harmonics in the unipolar voltage waveform are around the frequency $2\omega_S$. It means that the 3×VSC-1ϕ can be viewed as a converter switched with an "equivalent" frequency two times higher. Figure 4.27 shows the plots of the harmonic magnitude as a function of the amplitude modulation index m_a.

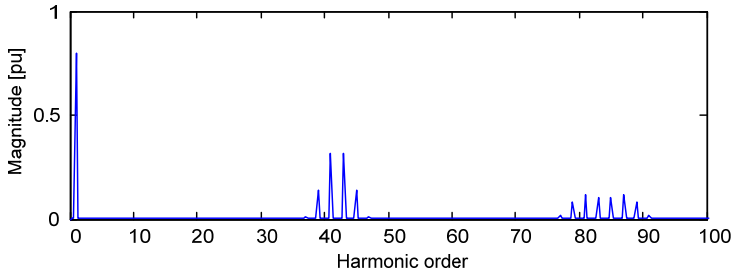


Figure 4.26 Harmonic spectrum of unipolar voltage waveform of phase "a" 3×VSC-1ϕ (m_a = 0.8 and m_f = 21)

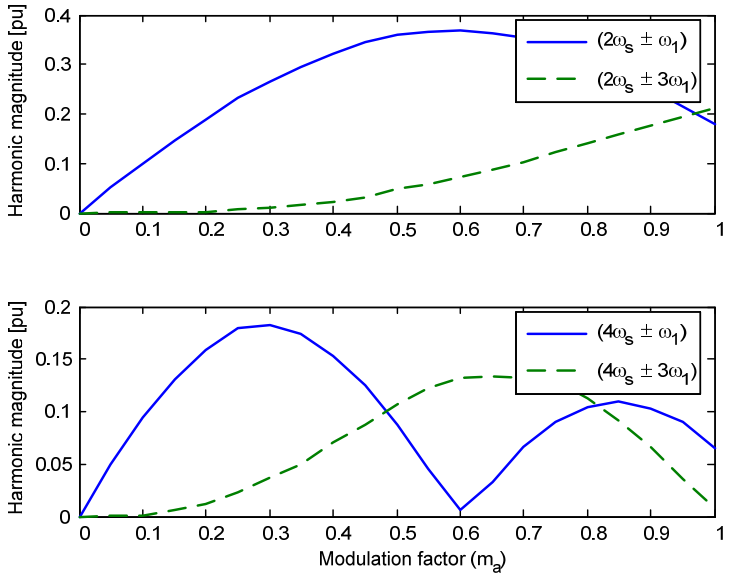


Figure 4.27 Harmonic magnitude behavior for the 3×VSC-1ϕ with unipolar voltage waveform

4.5.3 PWM with selective harmonic elimination

The PWM with selective harmonic eliminations (SHEPWM) is a useful technique to reduce the commutation frequency of VSC semiconductor switches. The turn on and off instants of the semiconductor switches are previously determined as shown in Figure 4.28 to eliminate some specific

harmonics at the VSC the output voltages. These turn on and off angles are calculated off-line and stored in non volatile memories.

Expanding the voltage waveform shown in Figure 4.28 where there are *M* chops (or notches) per half-cycle, the following expression is obtained for the *n-th* harmonic for the VSC output voltage

$$V_n = \left(\frac{4}{n\pi}\right) V_d \left[1 + 2\sum_{k=1}^{M} (-1)^k \cos(n\alpha_k)\right], \tag{4.13}$$

where n is the order of the harmonic to be eliminated; M is the number of notches per half-cycle of the output voltage; and α_k (rad), $k = 1, 2, 3, \ldots$, are the turn on and off angles of the selective harmonic technique.

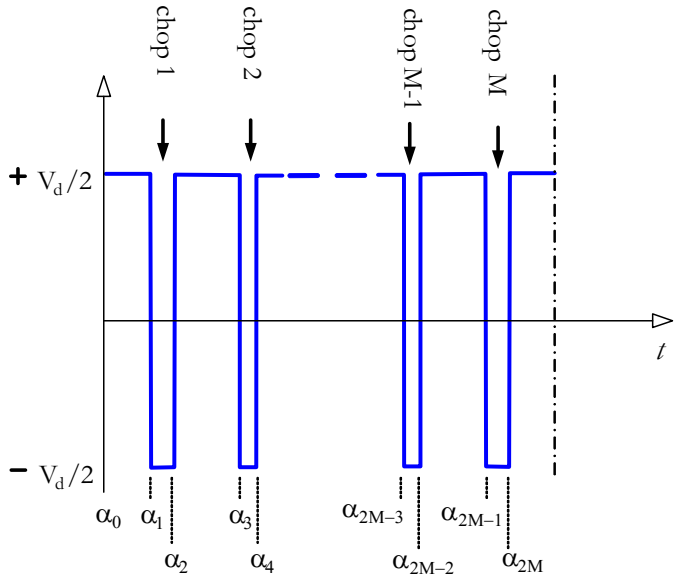


Figure 4.28 Example of pole voltage for selective harmonic elimination

Considering, for example, that the 5th and the 7th order harmonics are to be eliminated and the fundamental component should be controlled at the value *V*, the following simultaneous equations can be written from (4.13)

$$\begin{cases} V_1 = \left(\frac{4}{\pi}\right) V_d \left[1 - 2\cos(\alpha_1) + 2\cos(\alpha_2) - 2\cos(\alpha_3)\right] = V \\ V_5 = \left(\frac{4}{5\pi}\right) V_d \left[1 - 2\cos(5\alpha_1) + 2\cos(5\alpha_2) - 2\cos(5\alpha_3)\right] = 0 \\ V_7 = \left(\frac{4}{7\pi}\right) V_d \left[1 - 2\cos(7\alpha_1) + 2\cos(7\alpha_2) - 2\cos(7\alpha_3)\right] = 0 \end{cases} \tag{4.14}$$

Since the equations in (4.14) are nonlinear the angles α_1, α_2, and α_3 which eliminate 5th and 7th harmonics for a desired fundamental component could be determined using, for example, the Newton-Raphson method to solve those equations. To avoid delays and the loss of performance these angles are computed off-line and stored in tables. The great advantage of the SHEPWM is that low frequency harmonics can be eliminated using the lowest switching frequency, therefore with minimum losses. However, as the calculation is done off-line its dynamic response would not be as fast as in on-line PWM. Figure 4.29 shows the angles obtained with the numerical solution of (4.14).

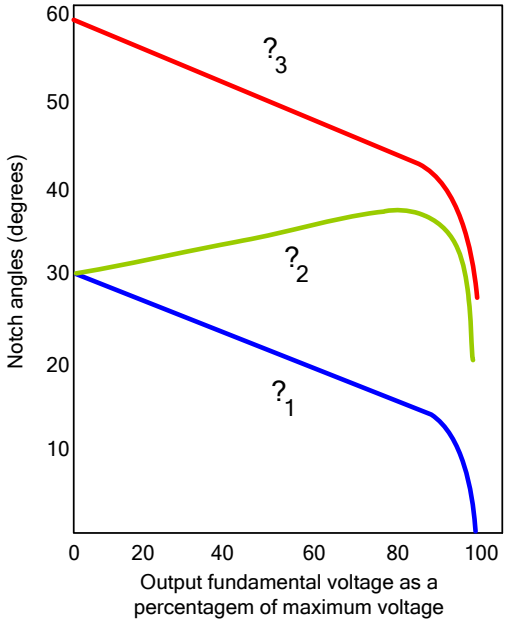


Figure 4.29 Angles to control the fundamental component and to cancel the 5th and 7th harmonics

4.5.4 Considerations about PWM SSSC synthesis

The fundamental component of the output voltages of the VSCs with a sinusoidal PWM modulation scheme is proportional to the modulation index m_a as shown in (4.6), (4.7), (4.10) and (4.12). However this characteristic is linear only for $0 \leq m_a \leq 1$. For $m_a > 1$, the VSC output voltage presents a nonlinear behavior. In fact, if the m_a index is continuously increased over the nonlinear limit, the VSC operates as a square wave converter for $m_a >> 1$.

Figure 4.30 shows the behavior of the output voltage of the 3×VSC-1ϕ as a function of the amplitude modulation factor (m_a). The output voltage is normalized by the DC capacitor voltage V_d. The value of m_a that defines the boundaries between the nonlinear and square-wave operation depends on the triangular carrier wave frequency and is given by

$$m_a \geq \frac{1}{\sin\left(\frac{3\pi}{2m_f}\right)} \tag{4.15}$$

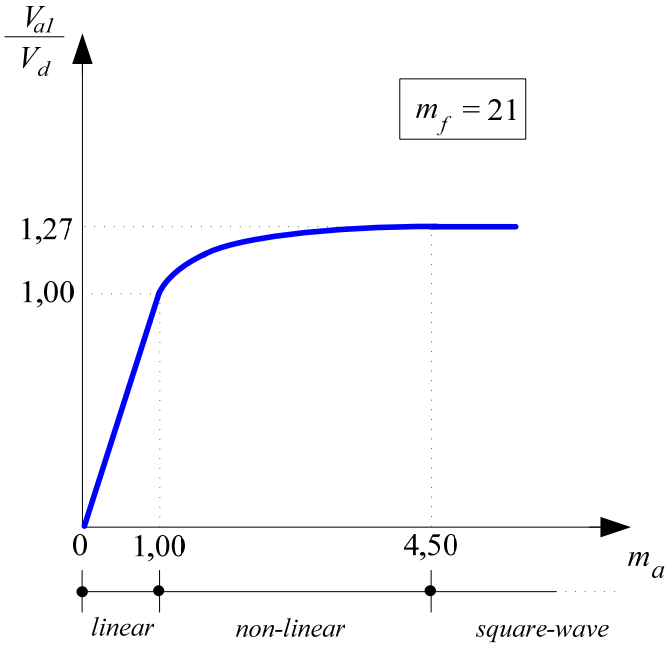


Figure 4.30 Relationship between fundamental output voltage magnitude and modulation index m_a

Another important point is that the PWM switching frequency, for high power VSC applications, cannot be high as the switching frequency used in industrial applications. Thus, the choice of the maximum frequency modulation index (m_f) depends on the voltage and current ratings of the power semiconductors devices.

The analysis of the harmonic spectra of the VSC-3ϕ (Figure 4.16) and of the 3×VSC-1ϕ with bipolar switching scheme (Figure 4.21) shows that if $(\omega_s - 2\omega) > \omega$, it is possible to keep the low-order harmonic from getting close to the fundamental component. The solution of the previous inequality results in the frequency modulation index having to comply with

$$m_f = \frac{\omega_s}{\omega} > 3. \tag{4.16}$$

This choice also avoids the superposition of the harmonics centered in ω_S and $2\omega_S$. In this case, to satisfy $(\omega_s + 2\omega) < (2\omega_s - \omega)$, m_f should be 3. This practical constraint assures that the lower order harmonics at the SSSC terminals are independent of the output fundamental frequency voltages. The choice of an *odd* value for m_f has an extra advantage because the generated voltage will have *odd* symmetry, and consequently without any *even* or non-characteristic harmonics.

The quality of the compensating voltages of the three and single-phase PWM VSCs are not sinusoidal and can be numerically evaluated by

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \times 100 \tag{4.17}$$

where *THD* is the voltage Total Harmonic Distortion index (%), V_1 is the fundamental frequency component of the output voltage, V_n is the *n-th* harmonic frequency of the output voltage and *n* is the harmonic order.

Figure 4.31 shows the total harmonic distortion as a function of the m_a factor, measured at the VSC terminals for three different configurations. Here again the 3×VSC-1ϕ with unipolar voltage waveform has a better behavior. It presents a lower harmonic distortion for $0 < m_a < 1$.

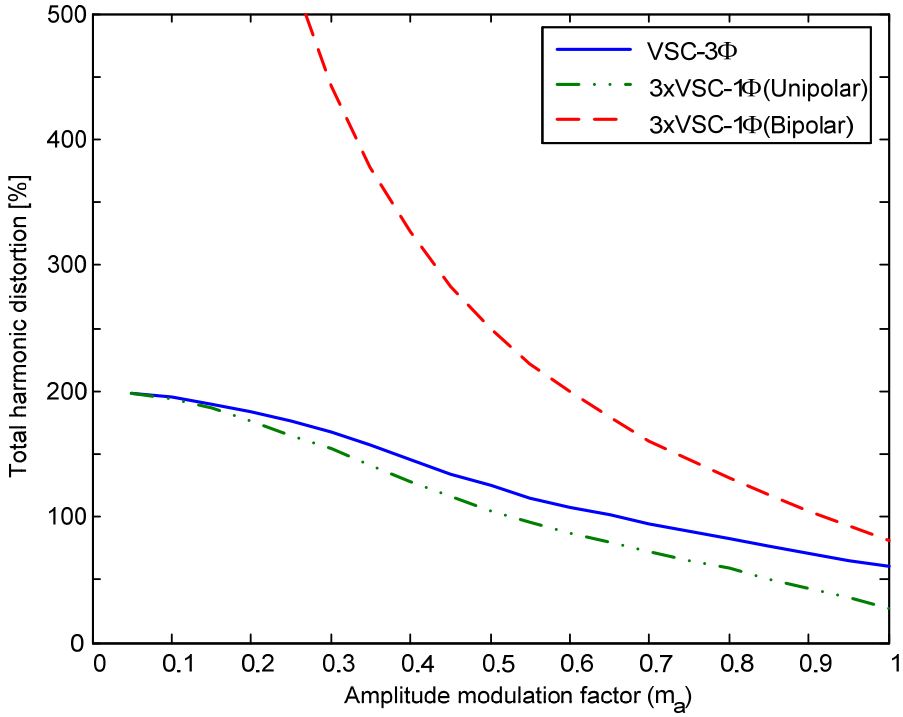


Figure 4.31 Total harmonic distortion of the output voltages of three-phase PWM VSCs

Based on the presented discussions, the 3×VSC-1ϕ with unipolar voltage wave form, shown in Figure 4.25, has a better performance because it can be viewed as a converter with twice the switching frequency and it has a high output voltage at its terminals. In this way, if the 3×VSC-1ϕ with unipolar voltage operates with $m_f = 3$ the low harmonics will appear around $m_f = 2\times3 = 6$. They have lower amplitude and they are farther from the fundamental component. This characteristic makes it easier to filter these harmonic using passive elements.

Another point is that the delta connected VSC-3ϕ can have the same output voltage of the 3×VSC-1ϕ if the compensating voltages are balanced and a third harmonic is summed to the reference signals. However, in this case the semiconductor currents are 73 % higher and the converter losses are increased by almost 200 %.

4.5.5 Square wave VSCs (6-pulse VSC)

If the objective is to have a VSC with minimum switching losses in the semiconductor devices, the switching frequency of the converters should be reduced to values near or equal to the fundamental frequency, to increase the utilization ratio of the semiconductor devices and consequently to increase to converter efficiency [4.2,4.8].

In the square-wave VSC strategy the GTOs are turned on and off only one time per cycle of the fundamental frequency voltage waveform. Figure 4.32(a), (b) and (c) shows the terminal voltages of the VSC. These voltages are normalized with respect to V_d and the symbol #n (n = 1,...,6) indicates which VSC switch (GTO + Diode) is conducting. These voltages are plotted considering the fictitious point "o" in the middle of the DC link capacitor (which is split in two) shown in Figure 4.11 as the reference. Observe that six firing pulses are sent to the converter semiconductor devices per cycle (T). This characteristic permits to call these converters as six-pulse converters or 6-pulse VSC.

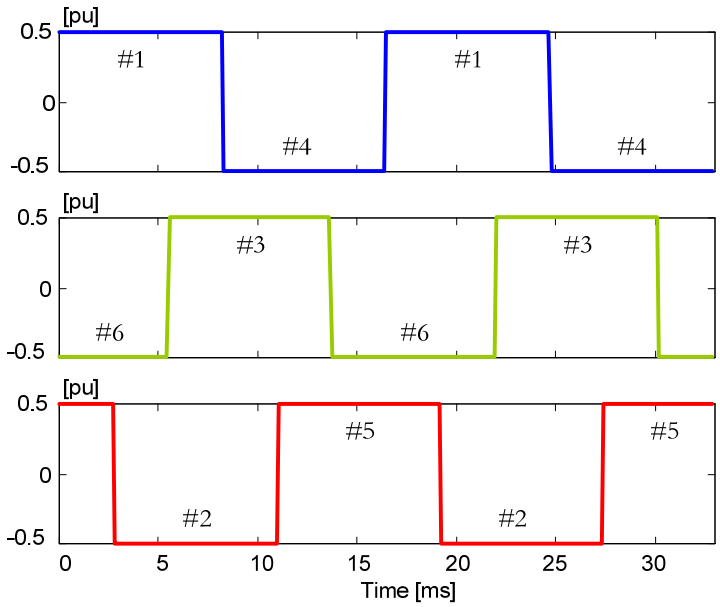


Figure 4.32 Pole voltages of the 6-pulse VSC: (a) v_{ao}, (b) v_{bo} and (c) v_{co}

From Figure 4.32, the line-to-line voltages of the 6-pulse VSC can be calculated by

$$\begin{cases} v_{ab} = v_{ao} - v_{bo} \\ v_{bc} = v_{bo} - v_{co} \\ v_{ca} = v_{co} - v_{ao} \end{cases} \tag{4.18}$$

Figure 4.33(a), (b) and (c) show the line-to-line voltages at the 6-pulse VSC terminals obtained from (4.18). Note that the line voltages are leading the VSC pole voltages by π/6 rad in Figure 4.32. The Fourier analysis of Figure 4.33 shows that the harmonics at the output voltages appear in frequencies $6k \pm 1$ for $k = 1, 2, 3, \ldots$, as shown below

$$\begin{cases} v_{ab} = \dfrac{2\sqrt{3}}{\pi} V_d \left[\cos(\omega t + \delta_i) - \dfrac{1}{5}\cos[5(\omega t + \delta_i)] + \dfrac{1}{7}\cos[7(\omega t + \delta_i)] - \right. \\ \qquad \left. - \dfrac{1}{11}\cos[11(\omega t + \delta_i)] + \ldots \right] \\ v_{bc} = \dfrac{2\sqrt{3}}{\pi} V_d \left[\cos(\omega t + \delta_i - 2\pi/3) - \dfrac{1}{5}\cos[5(\omega t + \delta_i - 2\pi/3)] + \right. \\ \qquad \left. + \dfrac{1}{7}\cos[7(\omega t + \delta_i - 2\pi/3)] - \dfrac{1}{11}\cos[11(\omega t + \delta_i - 2\pi/3)] + \ldots \right] \\ v_{ca} = \dfrac{2\sqrt{3}}{\pi} V_d \left[\cos(\omega t + \delta_i + 2\pi/3) - \dfrac{1}{5}\cos[5(\omega t + \delta_i + 2\pi/3)] + \right. \\ \qquad \left. + \dfrac{1}{7}\cos[7(\omega t + \delta_i + 2\pi/3)] - \dfrac{1}{11}\cos[11(\omega t + \delta_i + 2\pi/3)] + \ldots \right] \end{cases} \tag{4.19}$$

where ω is the output voltage angular fundamental frequency (rad/s), δ_i is a generic phase angle (rad), and V_d is the average DC voltage (V).

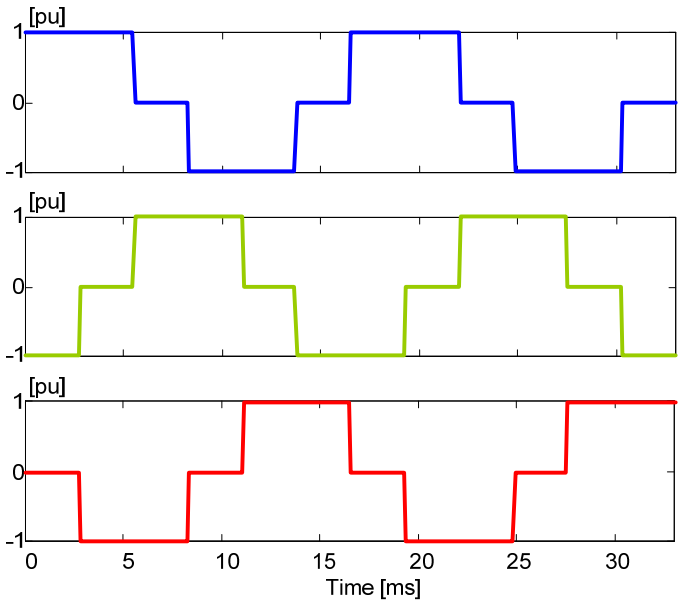


Figure 4.33 Line-to-line VSC voltage (for $\delta_i = 0^0$): (a) v_{ab}, (b) v_{bc}, and (c) v_{ca}

From (4.19), the magnitude of each harmonic is inversely proportional to its order. Figure 4.34 shows the harmonic spectrum of the output voltage of the 6-pulse VSC. This switching scheme also reduces the harmonics in the dc converter side which appears in frequencies $(6k)f$ (k = 1,2,3,…) for the DC current.

In this type of converter, the control of the magnitude of the output voltage is achieved through the charge or discharge the DC link capacitor C_d. This strategy, where the magnitudes of the ac voltages are controlled by the variation of the DC link converter voltage, is commonly called PAM (*Pulse Amplitude Modulation*).

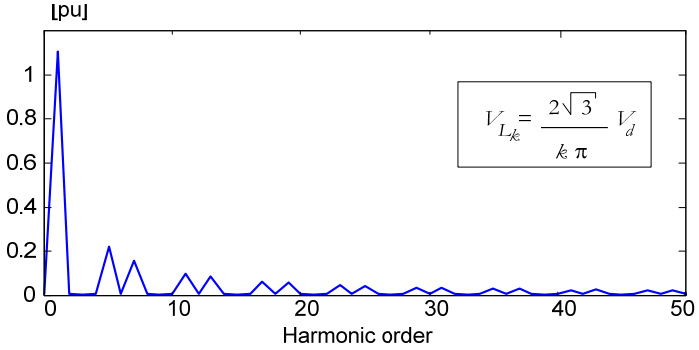


Figure 4.34 Harmonic spectrum of 6-pulse VSC line voltage

4.5.6 Square-wave operation of single-phase VSCs

Figure 4.35 shows the voltage waveforms of the 3×VSC-1ϕ topology of Figure 4.8 for the square wave operation. It has its output voltage magnitudes controlled by the modulation angle γ. In this

example γ is 2π/3 rad (= 5.56 ms for fundamental frequency of 60 Hz). Despite the square waveform shown in Figure 4.35, this scheme is also called a single-pulse PWM because the VSC output voltages can be controlled without charging or discharging the DC capacitor.

The Fourier analysis of the voltages shown in Figure 4.35 yields

$$\begin{cases} v_a = \frac{4}{\pi}V_d\left[\sin\left(\frac{\gamma}{2}\right)\cos(\omega t+\varphi)-\frac{1}{3}\sin\left(\frac{3\gamma}{2}\right)\cos[3(\omega t+\varphi)]+\right. \\ \qquad \left.+\frac{1}{5}\sin\left(\frac{5\gamma}{2}\right)\cos[5(\omega t+\varphi)]-\frac{1}{7}\sin\left(\frac{7\gamma}{2}\right)\cos[7(\omega t+\varphi)]+\cdots\right] \\ v_b = \frac{4}{\pi}V_d\left[\sin\left(\frac{\gamma}{2}\right)\cos(\omega t+\varphi-2\pi/3)-\frac{1}{3}\sin\left(\frac{3\gamma}{2}\right)\cos[3(\omega t+\varphi-2\pi/3)]+\right. \\ \qquad \left.+\frac{1}{5}\sin\left(\frac{5\gamma}{2}\right)\cos[5(\omega t+\varphi-2\pi/3)]-\frac{1}{7}\sin\left(\frac{7\gamma}{2}\right)\cos[7(\omega t+\varphi-2\pi/3)]+\cdots\right] \\ v_c = \frac{4}{\pi}V_d\left[\sin\left(\frac{\gamma}{2}\right)\cos(\omega t+\varphi+2\pi/3)-\frac{1}{3}\sin\left(\frac{3\gamma}{2}\right)\cos[3(\omega t+\varphi+2\pi/3)]+\right. \\ \qquad \left.+\frac{1}{5}\sin\left(\frac{5\gamma}{2}\right)\cos[5(\omega t+\varphi+2\pi/3)]-\frac{1}{7}\sin\left(\frac{7\gamma}{2}\right)\cos[7(\omega t+\varphi+2\pi/3)]+\cdots\right] \end{cases}, \tag{4.20}$$

where ω is the angular fundamental frequency of output voltage (rad/s), φ is a generic phase angle VSC (rad), γ is the angle equivalent to pulse width (rad), and V_d is the average DC capacitor voltage (V).

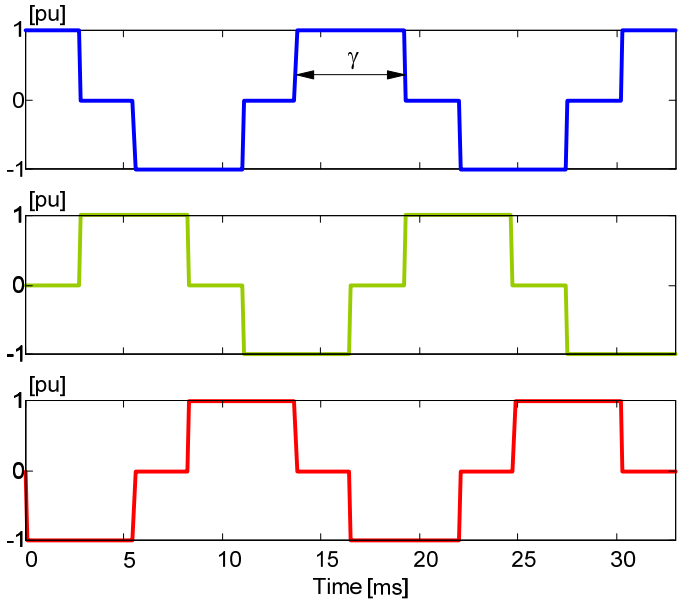


Figure 4.35 Output voltages of square wave operation of 3×VSC-1ϕ: (a) v_a, (b) v_b and (c) v_c

From (4.20), the rms value of the n-th harmonic of the VSC output voltage is given by

$$V_n = \frac{2\sqrt{2}}{\pi}V_d \sin\left[n\left(\frac{\gamma}{2}\right)\right], \tag{4.21}$$

where *n* is the odd harmonic order.

Figure 4.36 shows the rms voltage component behavior for different values of the modulation angle. These curves are normalized to the fundamental component value $V_{1,max}$. Observe that the fundamental component of the output voltage can be continuously controlled by the pulse width angle γ.

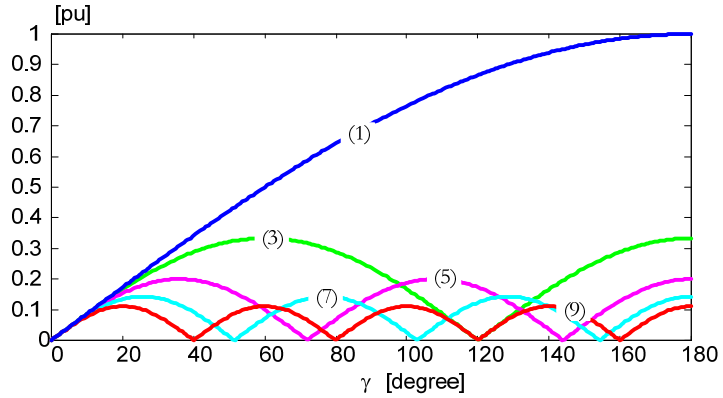


Figure 4.36 Behavior of the harmonics of the output voltages of the 3×VSC-1ϕ.

The total harmonic distortion of the 3×VSC-1ϕ varies with the angle γ and is given by

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2(\gamma)}}{V_1(\gamma)} \times 100 \qquad (4.22)$$

Figure 4.37 shows the behavior of the THD as function of the angle γ. Note that the THD value increases with the reduction of the angle γ. This behavior is due to the reduction of the fundamental component of the output voltage in (4.22) for smaller angle γ and still larger harmonic content.

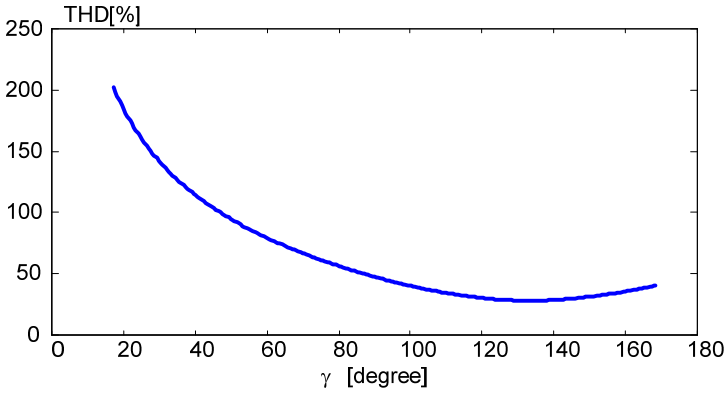


Figure 4.37 Behavior of the THD versus of the modulation angle γ.

4.5.7 Considerations about SSSC synthesis with 6-pulse VSC

Despite the square-wave VSC is more suitable for high power applications due to a lower number of commutations per cycle, this converter generates low-order harmonics that are more difficult to filter out because they are near the fundamental component of the output voltage.

A phase control of the output voltages should be designed to control the amount of real power absorbed or supplied by the converter in such a way as to control the DC link capacitor voltage. This control could be neglected if a single pulse PWM, similar to that shown in Figure 4.35, is used. However

the total harmonic distortion of this kind of converter increases drastically for low values of modulation angle γ as shown in Figure 4.37.

4.6 MULTILEVEL VSC

The advantages of the utilization of SSSC, based on VSC, to control dynamically the power flow in the transmission lines may be very important for a power system. However, the static process to generate the AC compensating voltages from a DC source is normally followed by harmonic generation as discussed in the preceding sections. These voltages and currents harmonics, with a few exceptions, should have their magnitudes minimized before the connection of the converters in the power system.

On the other hand, there are many utility agencies and technical associations in the world working to create indices to limit harmonic current injection and voltage distortion in electrical power systems. Table 4.3 reproduces the indices for voltage distortion suggested by ANSI/IEEE-519/1992 for different voltage levels. These indexes are measured at the point of common coupling (PCC) of the load or new device in the power system.

Table 4.3 Maximum voltage distortion indexes [Vh/V1 (%)]

	2.3~69 kV	69~138 kV	>138 kV
Individual harmonic amplitude	3.0	1.5	1.0
Total harmonic distortion	5.0	2.5	1.5

The comparison of the PWM-VSC and the square-wave VSC shows that the 6-pulse VSCs have low commutation losses due to the low number of commutations per cycle. They also have better utilization of the semiconductor switches because their output voltages have a high magnitude. Unfortunately 6-pulse VSCs have a high harmonic content near the fundamental component of the output voltage. In this way, to achieve the requirement suggested in Table 4.3, passive filters should be used to cut off the undesired harmonics. On the other side, these passive filters increase the size and the final cost of the VSC installation. In addition, these filters may cause resonance problems in power systems. Therefore, another way to overcome the harmonic constrains without the utilization of passive filters is the utilization of multilevel output voltage converters.

4.7 MULTIPULSE VSC

Many 6-pulse VSC can have their output voltages combined through an appropriate magnetic structure to form a multipulse VSC. This scheme requires the utilization of many transformers with their series and shunt terminals connected in such a way that the harmonics generated by one 6-pulse VSC are cancelled by the other converters. In this case the harmonics of a P-pulse VSC will be $(P\ k \pm 1)f$ for the AC output voltages and $(P\ k)f$ for the DC current of the VSC, where $P = 6m$; m is the number of 6-pulse VSCs, f is the fundamental switching frequency of the converters, and $k = 1, 2, 3, ...$

Figure 4.38 shows the block diagram of a multipulse VSC based on the connection of n six-pulse VSCs. Table 4.4 shows the characteristic harmonics of four multipulse VSC topologies. Note that the total harmonic distortion (THD) of the multipulse VSCs decrease with the increment of the number of VSC pulses. Thus, only 24 or high-pulse VSCs are indicated for high power system applications.

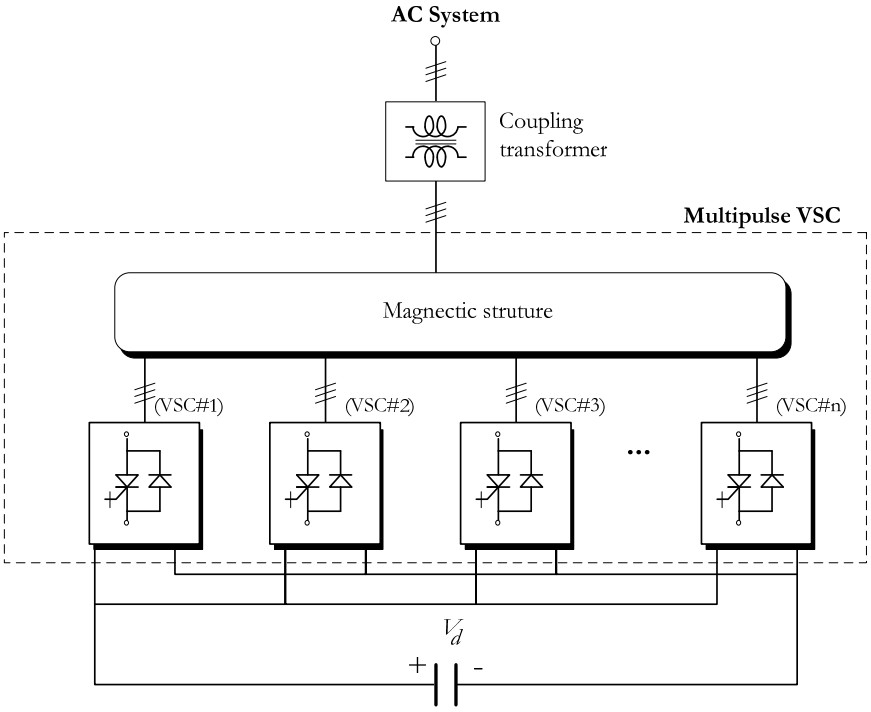


Figure 4.38 Basic arrangement of *P*-pulse VSC based on 6-pulse VSCs (*P* = 6*n*)

Table 4.4 Harmonics in multipulse VSCs

Harmonic order (n)	Harmonic component $\|V_n/V_1\|$x100%			
	6-pulse VSC	12-pulse VSC	24-pulse VSC	48-pulse VSC
5	20.000	-	-	-
7	14.286	-	-	-
11	9.091	9.091	-	-
13	7.692	7.692	-	-
17	5.882	-	-	-
19	5.263	-	-	-
23	4.348	4.348	4.348	-
25	4.000	4.000	4.000	-
29	3.448	-	-	-
31	3.226	-	-	-
35	2.857	2.857	-	-
37	2.703	2.703	-	-
41	2.439	-	-	-
43	2.326	-	-	-
47	2.127	2.1027	2.127	2.127
49	2.083	2.083	2.083	2.083
THD [%]	30.015	14.173	6.603	2.948

A multipulse VSC has the additional advantage of reducing the harmonics in the AC and DC converter terminals. This characteristic makes possible the optimized design of the DC capacitor because the VSC DC link current has a lower harmonic content.

4.7.1 24-pulse VSC

Figure 4.39 shows a 24-pulse VSC based on the series connection of four 6-pulse VSCs through four zigzag transformers. In this figure the fundamental voltage generated by each VSC is leading or lagging by an equivalent angle θ_n (rad) as

$$\theta_n = \left[\frac{(2n-1)-m}{2m}\right]\left(\frac{\pi}{3}\right), \tag{4.23}$$

where n is the number that defines the position of the 6-pulse VSC in the multipulse converter and m is the total number of converters in the multipulse configuration.

Figure 4.40 shows the voltage waveforms of each of the four 6-pulse VSCs of Figure 4.39 that form phase "a" output voltage. These voltages are normalized to V_d and they are plotted considering the fictitious midpoint between the DC capacitor as the reference. The phase delays of each converter voltage are $-\pi/8$ rad, $-\pi/24$ rad, $+\pi/24$ rad, and $+\pi/8$ rad (–22.50, –7.50, +7.50, and +22.50 degrees), respectively.

Because the primary side of the transformers is series connected, each 6-pulse VSC have to be designed to generate $1/m$ of the total output voltage and each unit power should be designed to be $1/m$ of the multipulse VSC total power.

The zigzag transformers are special purpose transformers built to lead or to lag the output voltages of the VSC. Then, the secondary windings are connected in such a way as to guarantee that the fundamental component of the voltages of each 6-pulse VSCs will be in phase in the transformer primary windings as illustrated in Figure 4.41. Therefore the transformer turns ratio are calculated considering a linear frequency response for the fundamental component and the proper relations are given by

$$N_{n1} = \frac{\sin(\pi/6)}{\sin\theta_n}, \tag{4.24}$$

and

$$N_{n2} = \frac{\sin(\pi/6)}{\sin\left(\pi/6 - \theta_n\right)}, \tag{4.25}$$

where n is the number that defines the position of the VSC in the multipulse configuration and θ_n is the lead or lag angle of the n^{th} VSC.

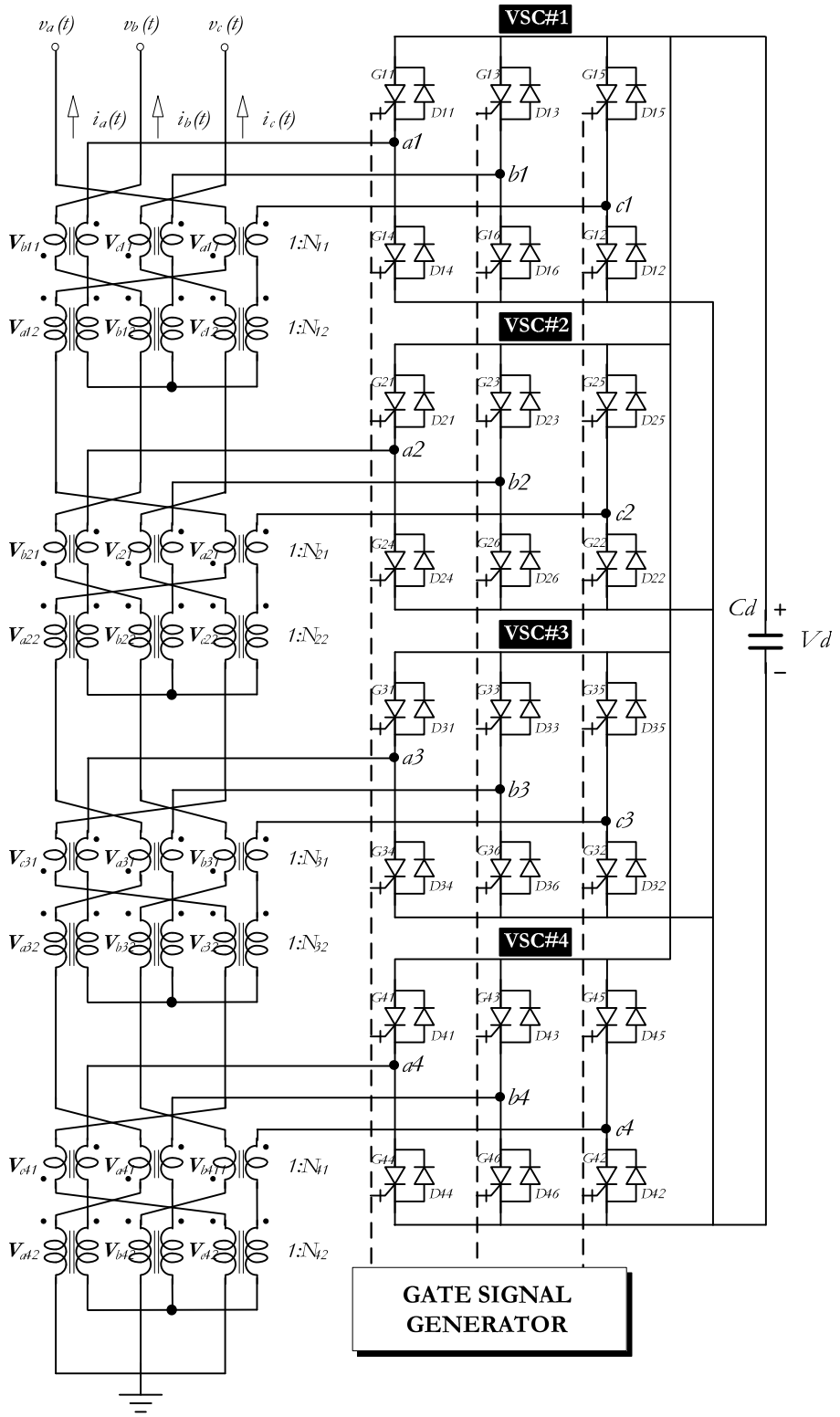


Figure 4.39 Configuration of the 24-pulse VSC based on zigzag transformers connection

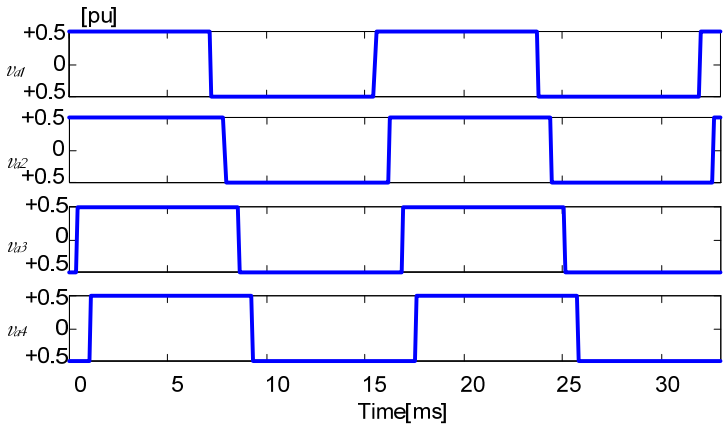


Figure 4.40 Phase "a" output voltages of each unit of 24-pulse VSC

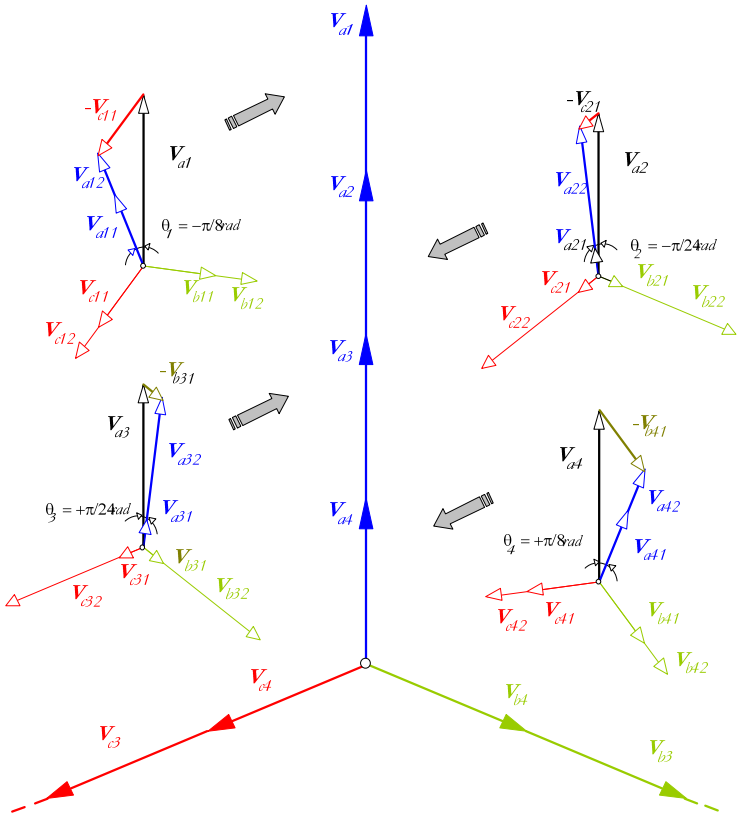


Figure 4.41 Phasor diagram for phase "a" at fundamental frequency for the output voltage construction (scale: $2V_d/\pi$ = 0.65 pu = 3 cm)

Figure 4.42 presents the voltages waveforms on the primary side of the zigzag transformers. Figure 4.43 shows the three-phase 24-pulse VSC voltages and Figure 4.44 shows the phase "a" harmonic spectrum. Observe that the 11th, 13th, 17th, and 19th harmonics and their multiples are cancelled. Figure 4.41 shows how the fundamental component of the 24-pulse VSC output voltage is composed.

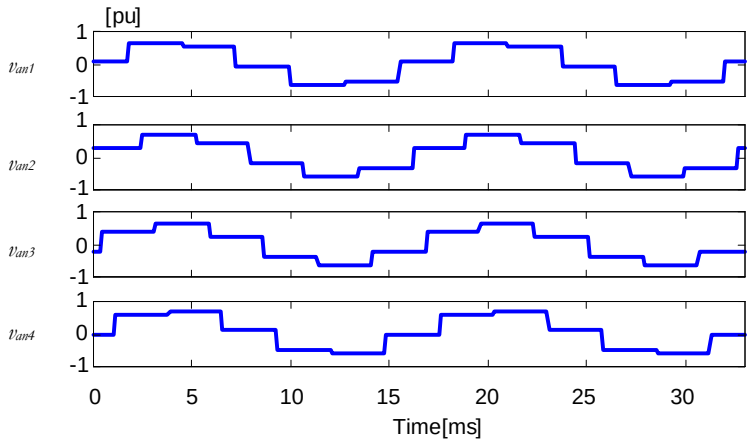


Figure 4.42 Phase "a" 24-pulse VSC output voltages on the primary side of the Zigzag transformers

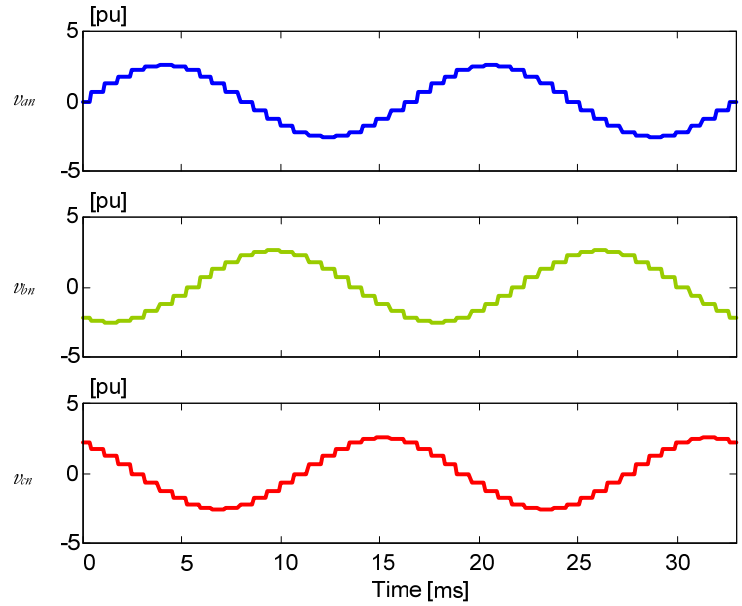


Figure 4.43 24-pulse VSC output voltages

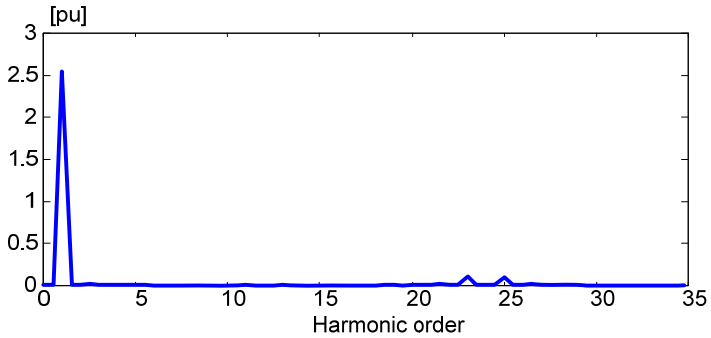


Figure 4.44 Harmonic spectrum of 24-pulse VSC Phase "a" output voltage

4.7.2 Quasi 24-pulse VSC

Inspite of the voltage waveform obtained with multipulse converter, the complexity of zigzag transformers increases with the number of pulses of the converter. That is, for a large number of pulses, VSC requires many zigzag transformers with fractional turns-ratio to adjust the phase of all fundamental voltage components. Consequently, the costs, the size, and the weight of the equipment increase. In addition, an increase of the operational problems with the transformers is observed due to voltage equalization, magnetizing currents, and core saturation.

Figure 4.45 shows a quasi-24 pulse VSC topology based on the series connection of two 12-pulse VSC. In this arrangement the firing pulses of the GTOs of VSC#1 and VSC#2 are electronically phase shifted from the pulses of the GTOs of VSC#3 and VSC#4.

The 12-pulse VSC is the simplest multipulse topology of VSC. It is built by the connection of two 6-pulse VSC with their phase voltages shifted by π/3 rad (60 degrees). To synthesize the 12 pulse output voltage two transformers with their windings connected in Y-Y and Δ-Y are used. In this scheme the 5th and the 7th harmonics are canceled.

The output voltage of each 12-pulse VSC is given respectively by

$$v_{a12(1)} = 2\left(\frac{2}{\pi}\right)\frac{V_d}{N_p}\left[\cos(\omega t+\delta_1)-\frac{1}{11}\cos[11(\omega t+\delta_1)]+\frac{1}{13}\cos[13(\omega t+\delta_1)]-\right.$$
$$\left.-\frac{1}{23}\cos[23(\omega t+\delta_1)]+\frac{1}{25}\cos[25(\omega t+\delta_1)]-\ldots\right], \quad (4.26)$$

and,

$$v_{a12(2)} = 2\left(\frac{2}{\pi}\right)\frac{V_d}{N_p}\left[\cos(\omega t+\delta_2)-\frac{1}{11}\cos[11(\omega t+\delta_2)]+\frac{1}{13}\cos[13(\omega t+\delta_2)]-\right.$$
$$\left.-\frac{1}{23}\cos[23(\omega t+\delta_2)]+\frac{1}{25}\cos[25(\omega t+\delta_2)]-\ldots\right], \quad (4.27)$$

where V_d is the average DC voltage of the VSC (V), ω is the fundamental angular frequency (rad/s), N_p is the primary to secondary normalized transformer turn ratio, and δ_1 and δ_2 are generic phase angles of the output voltages of the 12-pulse VSC #1 and #2 (rad), respectively.

Because the output voltages of the two 12-pulse VSCs are connected in series, if $(\delta_1 + \delta_2)/2 = 0$ and $(\delta_1 - \delta_2) = \pi/11$ rad in (4.26) and (4.27), the 11th voltage harmonic will be canceled. On the other hand, if $(\delta_1 - \delta_2) = \pi/13$ rad, the 13th output voltage harmonic is canceled. Observe that the behavior described above is valid for "b" and "c" phases, if lagged by $-2\pi/3$ rad and $-4\pi/3$ rad respectively for the positive sequence harmonics and by $-4\pi/3$ rad and $-2\pi/3$ rad respectively for the negative sequence harmonics.

The described mechanism cannot cancel the 11th and 13th harmonics simultaneously. However, both harmonics can have their amplitudes minimized if $(\delta_1 - \delta_2) = \pi/12$ rad and $(\delta_1 + \delta_2)/2 = 0$. In this case the amplitudes of the 11th and 13th harmonics will be 1.19% and 1.01% of the fundamental component, respectively. The rms value of the fundamental component output voltage is given by:

$$V = \frac{\sqrt{2}}{\pi}\frac{m}{N_p}V_d\cos\left(\frac{\pi}{24}\right) \quad (4.28)$$

where V_d is the average DC capacitor voltage CC (V), $m = 4$ is the number of 6-pulse VSC connected in series, and N_p is the normalized transformer turns ratio.

In Figure 4-46(a), (b), (c), and (d) it is drawn the mechanism by which the fundamental and harmonic voltage components are summed and minimized in the quasi 24-pulse VSC, respectively. In this figure the following values were assumed: $(\delta_1 - \delta_2) = \pi/12$ rad, $(\delta_1 + \delta_2)/2 = 0$, $V_d = 1$ pu, and $N_p = 1$. The first subscripts of each voltage represent the harmonic order and the second subscript defines the group of the 12-pulse VSC.

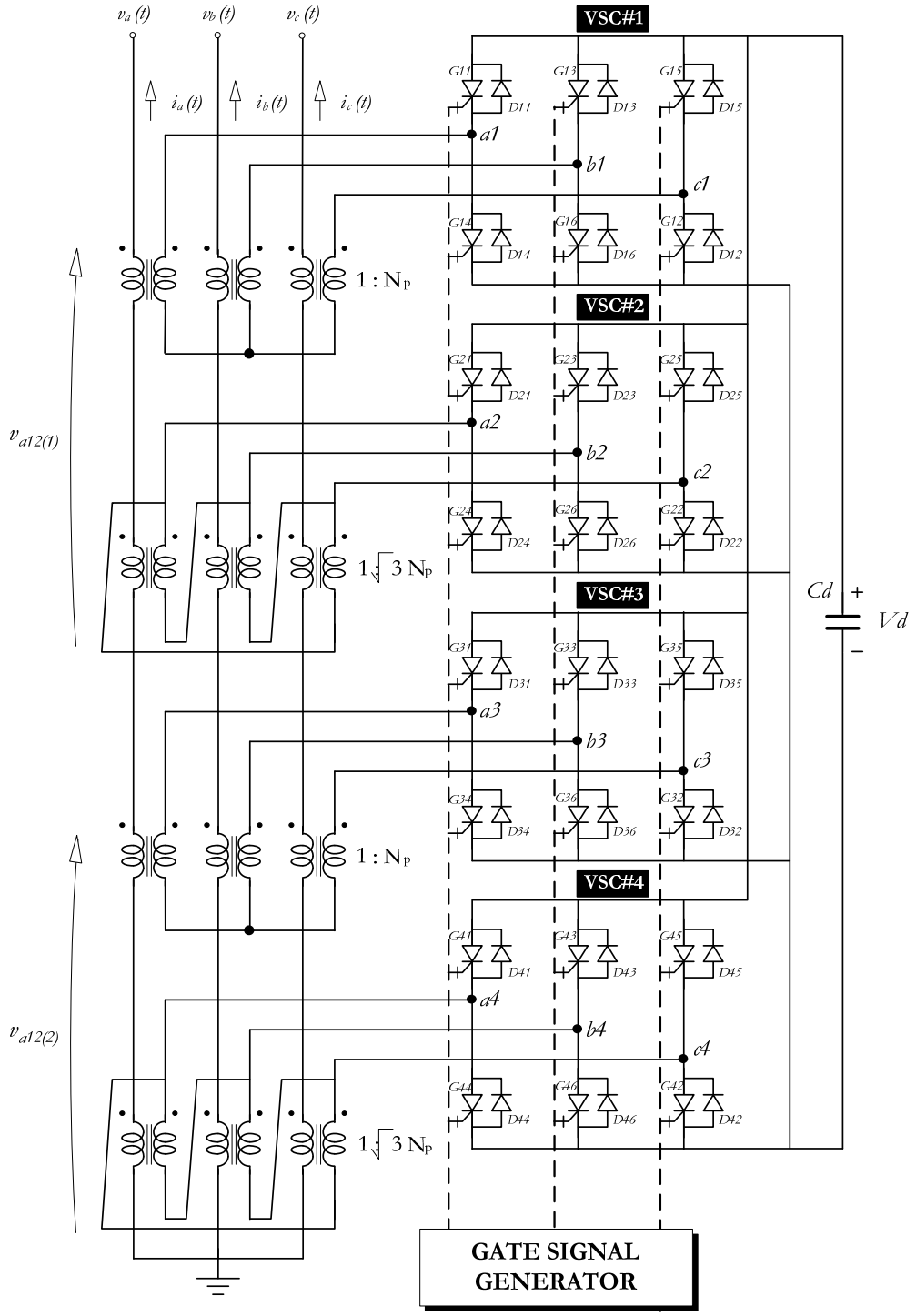


Figure 4.45 Configuration of *quasi*-24 pulse VSC based on two 12-pulse VSC

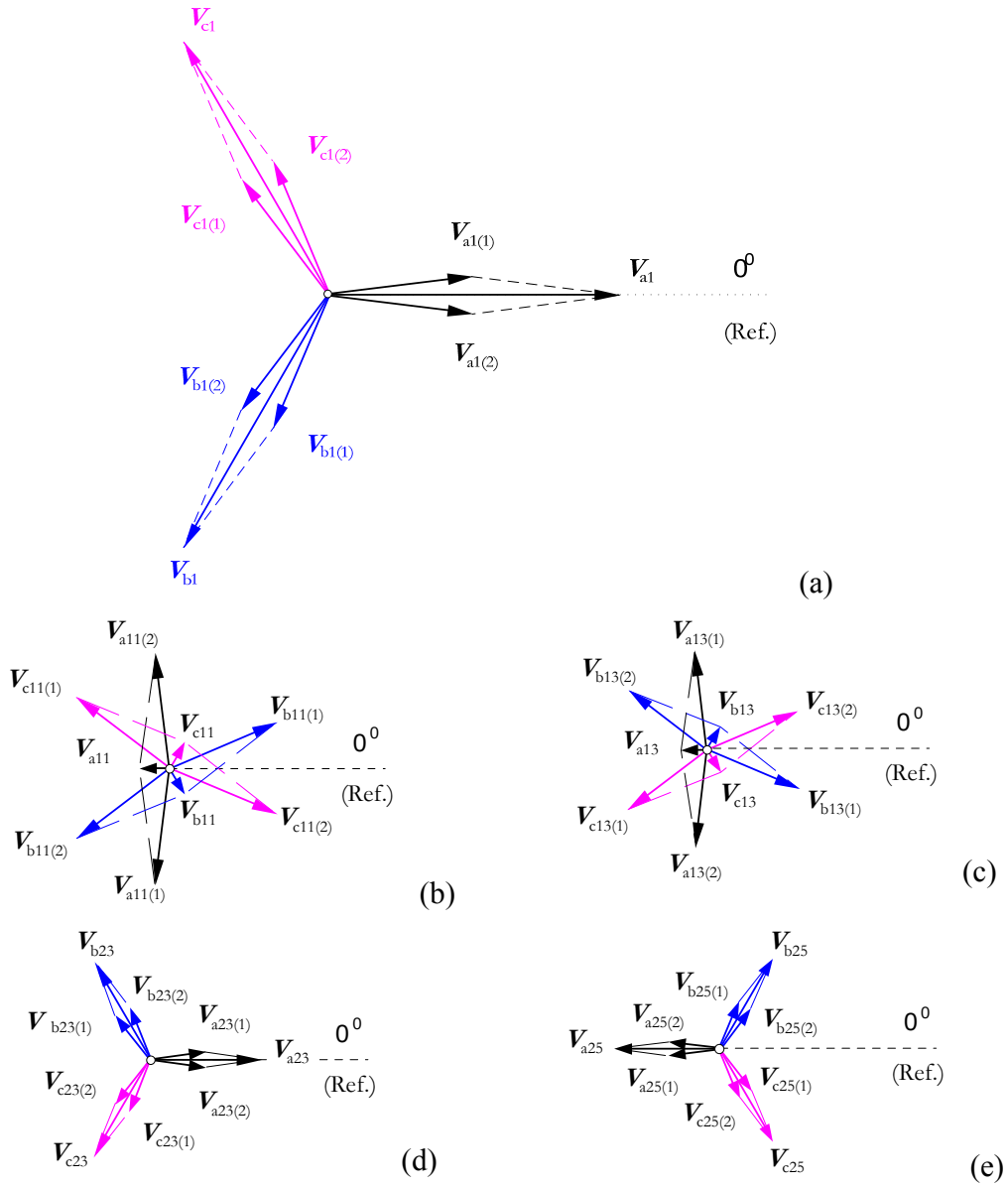


Figure 4-46 Phasor composition of three phase output voltage of *quasi* 24-pulse VSC: (a) fundamental; (b) 11th; (c) 13th; (d) 23th; (e) 25th

Figure 4.47 plots the three-phase output voltages of the quasi 24-pulse VSC and Figure 4.48 shows the phase "a" harmonic spectrum. As explained before the 11th and 13th harmonics have their magnitudes minimized.

Table 4.5 shows the theoretical values of the harmonics of the output voltages of a 24-pulse VSC and a quasi 24-pulse VSC. From the point of view of the total harmonic distortion (THD), the last row of Table 4.5, the two topologies of 24-pulse VSC have a very close behavior. However, comparing Figure 4.39 and Figure 4.45, the quasi 24-pulse VSC has the advantage of not needing complicated transformers with multiple windings per phase and with fractionary turn ratio.

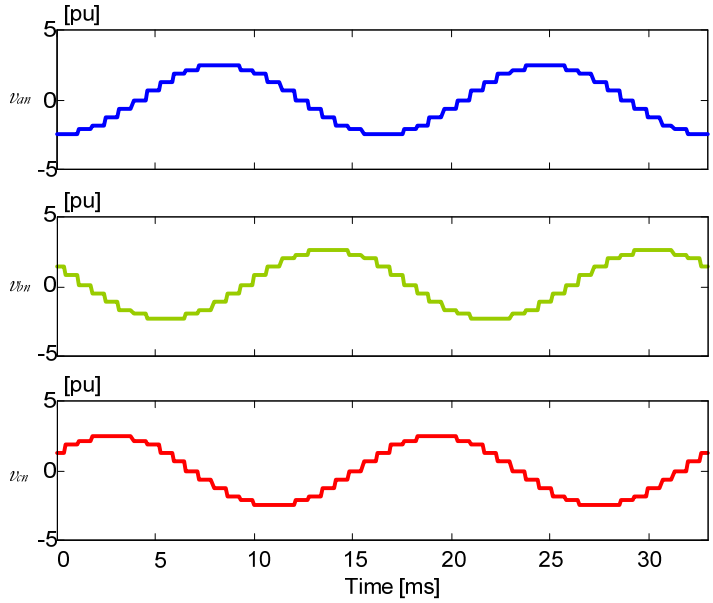


Figure 4.47 Output voltages of *quasi* 24-pulse VSC

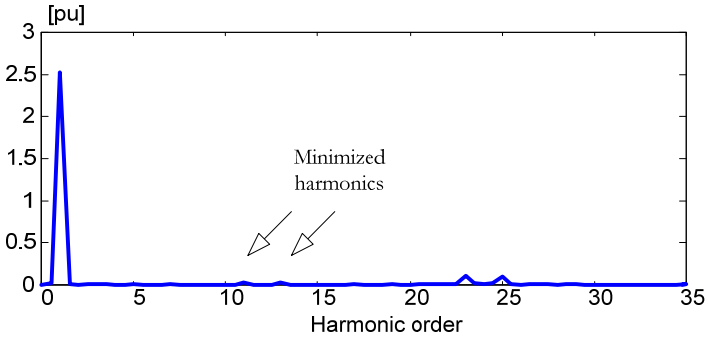


Figure 4.48 Harmonic spectrum of *quasi* 24-pulse VSC output voltage

Table 4.5: Characteristic harmonics of the output voltage of 24-pulse VSC topologies [V_h/V_1)100%]

Harmonic order (n)	Harmonic component	
	24-pulse VSC	*Quasi* 24-pulse VSC
11	-	1.197
13	-	1.013
23	4.348	4.348
25	4.000	4.000
35	-	0.376
37	-	0.356
47	2.127	2.127
49	2.083	2.041
THD [%]	6.603	6.806

4.7.3 Quasi 48-pulse VSC

Figure 4.49 shows the block diagram of a quasi 48-pulse VSC obtained with the series connection of four 12-pulse VSC or two quasi 24-pulse VSC. In this case, the two quasi 24-pulse VSCs should have their output voltages electronically phase shifted by π/24 rad between them.

In the transformer primary side windings, the output voltage of each 12-pulse VSC of Figure 4.49 can be written as

$$v_{a12(1)} = 2\left(\frac{2}{\pi}\right)\frac{V_d}{N_p}\left[\cos(\omega t+\delta_1)-\frac{1}{11}\cos[11(\omega t+\delta_1)]+\frac{1}{13}\cos[13(\omega t+\delta_1)]-\right.$$
$$\left.-\frac{1}{23}\cos[23(\omega t+\delta_1)]+\frac{1}{25}\cos[25(\omega t+\delta_1)]-\ldots\right] \quad (4.29)$$

$$v_{a12(2)} = 2\left(\frac{2}{\pi}\right)\frac{V_d}{N_p}\left[\cos(\omega t+\delta_2)-\frac{1}{11}\cos[11(\omega t+\delta_2)]+\frac{1}{13}\cos[13(\omega t+\delta_2)]-\right.$$
$$\left.-\frac{1}{23}\cos[23(\omega t+\delta_2)]+\frac{1}{25}\cos[25(\omega t+\delta_2)]-\ldots\right] \quad (4.30)$$

$$v_{a12(3)} = 2\left(\frac{2}{\pi}\right)\frac{V_d}{N_p}\left[\cos(\omega t+\delta_3)-\frac{1}{11}\cos[11(\omega t+\delta_3)]+\frac{1}{13}\cos[13(\omega t+\delta_3)]-\right.$$
$$\left.-\frac{1}{23}\cos[23(\omega t+\delta_3)]+\frac{1}{25}\cos[25(\omega t+\delta_3)]-\ldots\right] \quad (4.31)$$

$$v_{a12(4)} = 2\left(\frac{2}{\pi}\right)\frac{V_d}{N_p}\left[\cos(\omega t+\delta_4)-\frac{1}{11}\cos[11(\omega t+\delta_4)]+\frac{1}{13}\cos[13(\omega t+\delta_4)]-\right.$$
$$\left.-\frac{1}{23}\cos[23(\omega t+\delta_4)]+\frac{1}{25}\cos[25(\omega t+\delta_4)]-\ldots\right] \quad (4.32)$$

where V_d is the average DC capacitor voltage (V), ω is the fundamental angular frequency (rad/s), N_p is the normalized transformer turns ratio, δ_1, δ_2, δ_3, and δ_4 are the phase angles of output voltage of each of the 12-pulse VSCs.

Considering the converter configuration shown in Figure 4.45, if the first quasi 24-pulse VSC has its output voltage leading by π/48 rad while the second quasi 24-pulse VSC has its output voltage lagging by π/48 rad, the 11^{th}, 13^{th}, 23^{rd} , and 25^{th} harmonics will have their amplitudes minimized. The mechanism by which the harmonics are minimized is similar to that shown in Figure 4-46 for the quasi 24-pulse VSC. In this case, the rms value of the fundamental component output voltage can be calculated by

$$V = \left[\frac{\sqrt{2}}{\pi}\frac{m}{N_p}V_d\cos\left(\frac{\pi}{24}\right)\right]\cos\left(\frac{\pi}{48}\right) \quad (4.33)$$

where V_d is the DC capacitor voltage CC (V), m = 8 is the number of 6-pulse VSC connected in series.

Figure 4.50 shows the three-phase voltages waveform of the quasi 48-pulse VSC and Figure 4.51 shows the phase "a" harmonic spectrum.

Table 4.6 shows the magnitude of the harmonics for two 48-pulse VSC topologies. As for the 24-pulse VSC, the comparison between the 48-pulse VSC and the quasi 48-pulse VSC shows a very close behavior.

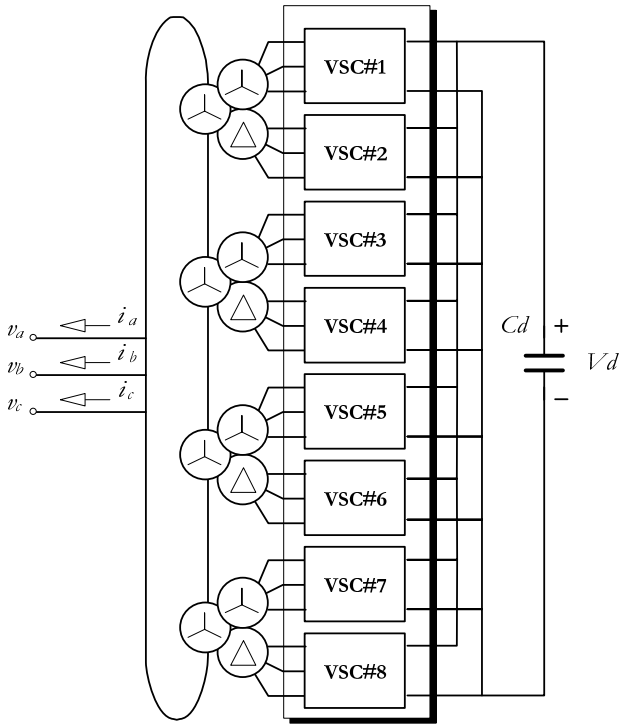


Figure 4.49 Block diagram of *quasi* 48-pulse VSC based on the series connection of two *quasi* 24-pulse VSCs

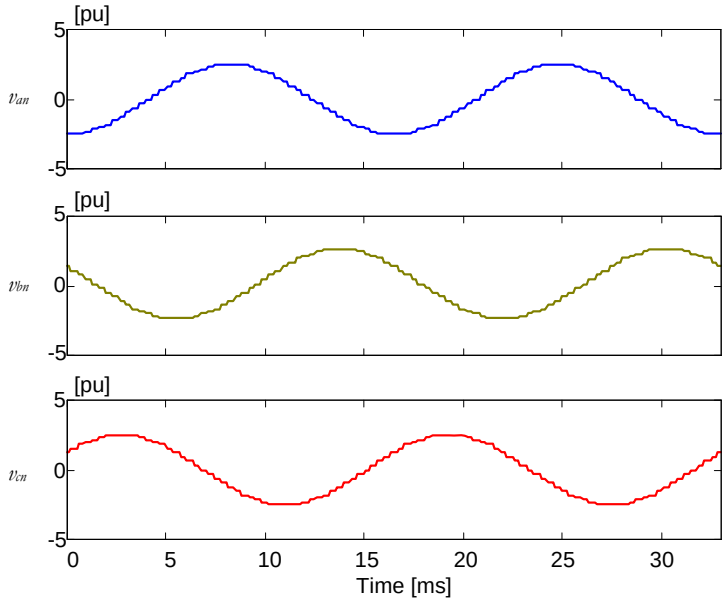


Figure 4.50 Three-phase output voltages of *quasi* 48-pulse VSC

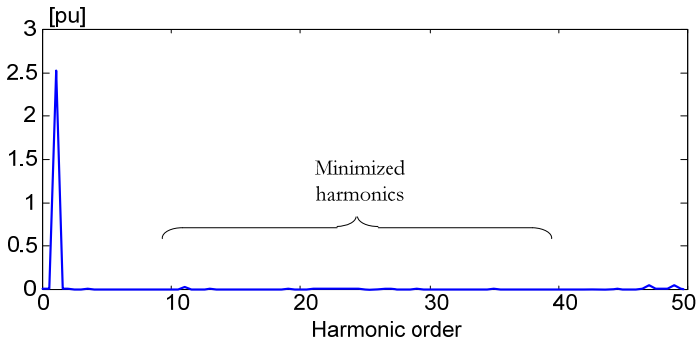


Figure 4.51 Harmonic spectrum of output voltage of *quasi* 48-pulse VSC

Table 4.6 Characteristic harmonics of the output voltage of 48-pulse VSC topologies [(V_h/V_1)100%]

Harmonic order	Harmonic component	
	48-pulse VSC	*quasi* 48-pulse VSC
11	-	0.902
13	-	0.669
23	-	0.285
25	-	0.262
35	-	0.249
37	-	0.268
47	2.127	2.127
49	2.083	2.041
THD [%]	2.948	3.199

4.8 MULTI-LEVEL SINUSOIDAL PWM VSC

Many sinusoidal PWM VSCs can have their output voltages combined to form a multi-level PWM VSC. As in the multi-pulse scheme, the multi-level PWM VSC requires the utilization of many transformers with their series terminals connected in such a way that the harmonics generated by one VSC are compensated by the others. This scheme has the advantage of reducing the total harmonic distortion of the VSC output voltages.

4.8.1 Single phase PWM-VSC with multilevel output voltage

In Section 4.5.2 (Figure 4.26) it was shown that a single-phase VSC could be viewed as a converter switching at an equivalent double frequency ($2f_S$) even when its semiconductor devices are turned on and off with a switching frequency f_S. The converter switching frequency multiplication effect is obtained by the use of triangular carrier waves phase shifted by π rad between them. This procedure can be expanded for n converters connected in series and modulated by n carrier triangular carrier waves phase-shifted by ($2\pi/n$) rad between them **Erreur ! Source du renvoi introuvable.**.

Figure 4 shows the basic configuration of the multilevel output voltage based on single-phase VSCs (VSC-1ϕ). In this multilevel converter n VSC-1ϕ has its output voltages summed through n identical single-phase transformers.

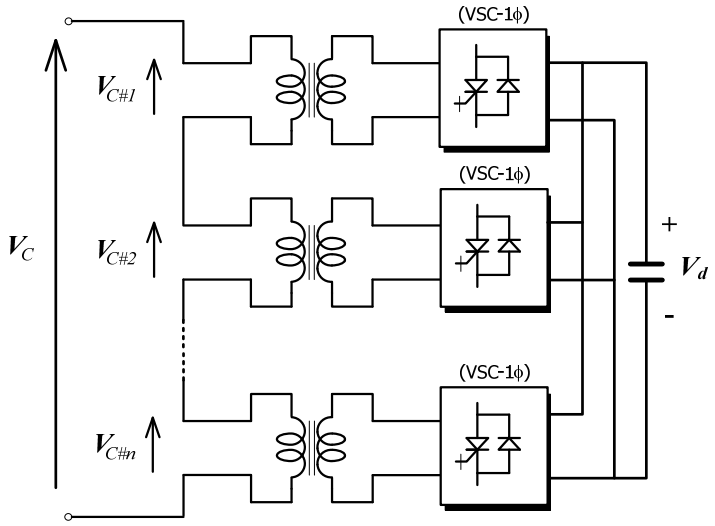


Figure 4.52 Basic configuration of multilevel VSC-1ϕ

Figure 4.53 and Figure 4.54 show the output voltage waveform and the harmonic spectrum considering the series connection of one, two, and three single-phase VSCs, respectively. In these figures, each VSC-1ϕ generates a bipolar output voltage similar to that discussed in Section 4.5.2. Each VSC-1ϕ is switched with 1 kHz. The harmonics appear around the frequency $n\omega_S$, where n is the number of PWM VSC-1ϕ. The triangular carrier waves were phase-shifted by 0 in Figure 4.53(a), by π rad in Figure 4.53(b), and 2π/3 rad in Figure 4.53(c). The use of multicarrier wave introduces intermediary levels in the VSC output voltages and increases the equivalent commutation frequency of the converter.

In Figure 4.55(a), (b), and (c), it is plotted the voltage waveforms for the multilevel VSC-1ϕ when a unipolar switching scheme is used. Figure 4.56 shows the harmonic spectra for one, two, and three unipolar VSC-1ϕ connections, respectively. The harmonics will appear around the frequency $(2n\omega_S)$, where n is the number of PWM VSC-1ϕ. In this figure each VSC-1ϕ generates a unipolar output voltage as discussed in Section 4.5.2. Now, each VSC-1ϕ uses two triangular carrier waves phase shifted by π rad. The carrier wave frequencies are equal to 1 kHz and their phase angles are 0 and π rad for Figure 4.55(a), 0, π/2, π, and 3π/2 rad for Figure 4.55(b), and 0, π/3, 2π/3, π, 4π/3, and 5π/3 rad for Figure 4.55(c). From the comparison of the simulated results, it is possible to conclude that the multilevel VSC-1ϕ, with unipolar voltage waveform (Figure 4.55), presents a better performance than the multilevel VSC-1ϕ that uses a unipolar voltage waveform (Figure 4.53).

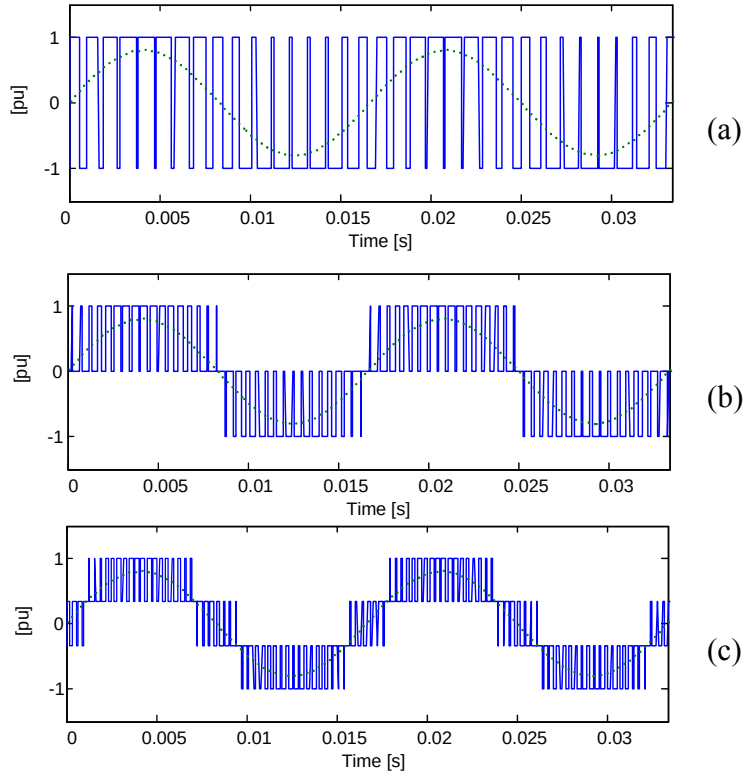


Figure 4.53 Multi-level voltages for bipolar VSC-1ϕ: (a) one, (b) two, and (c) three VSCs

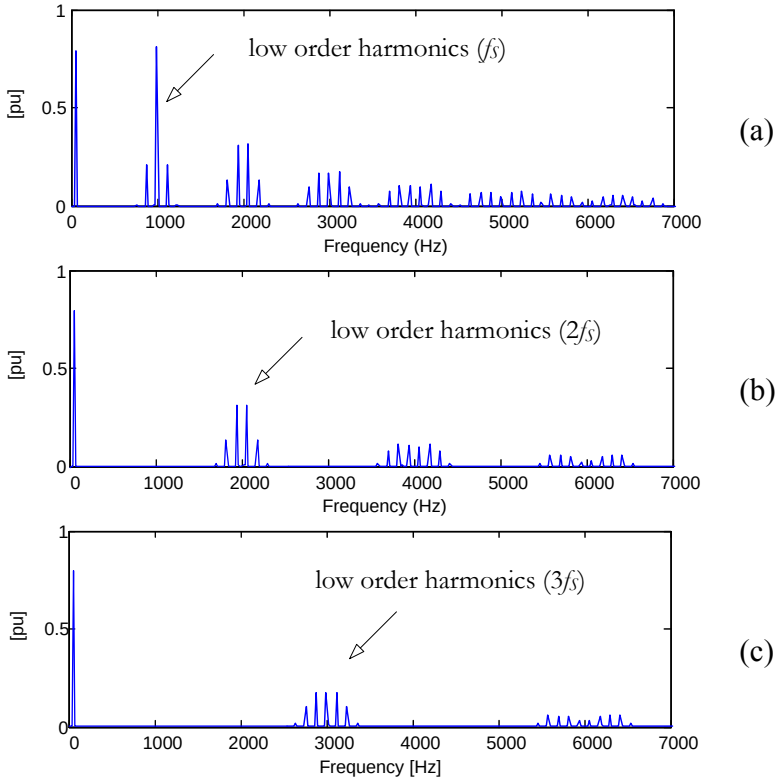


Figure 4.54 Harmonic spectra for multi-level unipolar VSC-1ϕ: (a) one, (b) two and (c) three VSCs

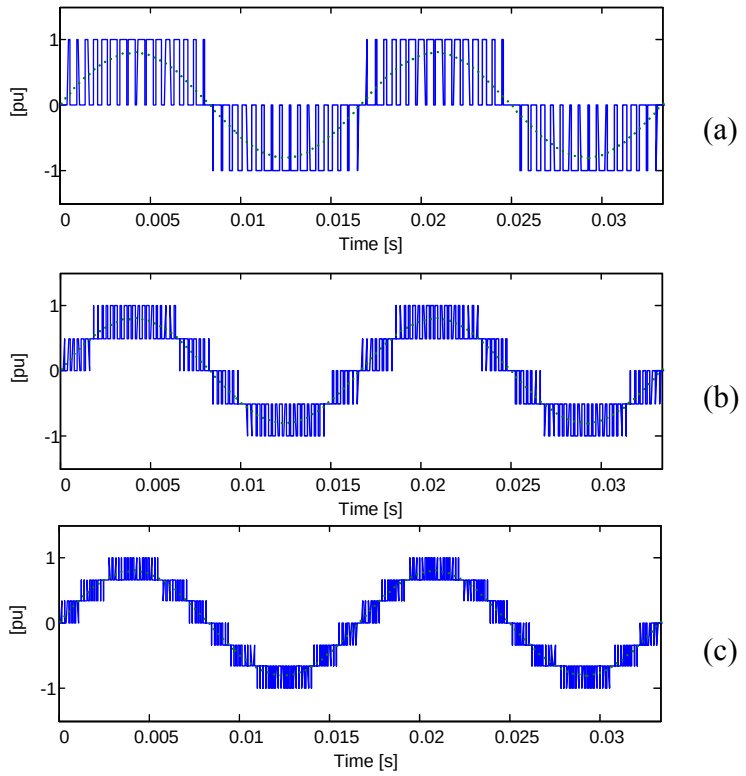


Figure 4.55 Multi-level voltages for unipolar VSC-1ϕ: (a) one, (b) two, and (c) three VSCs

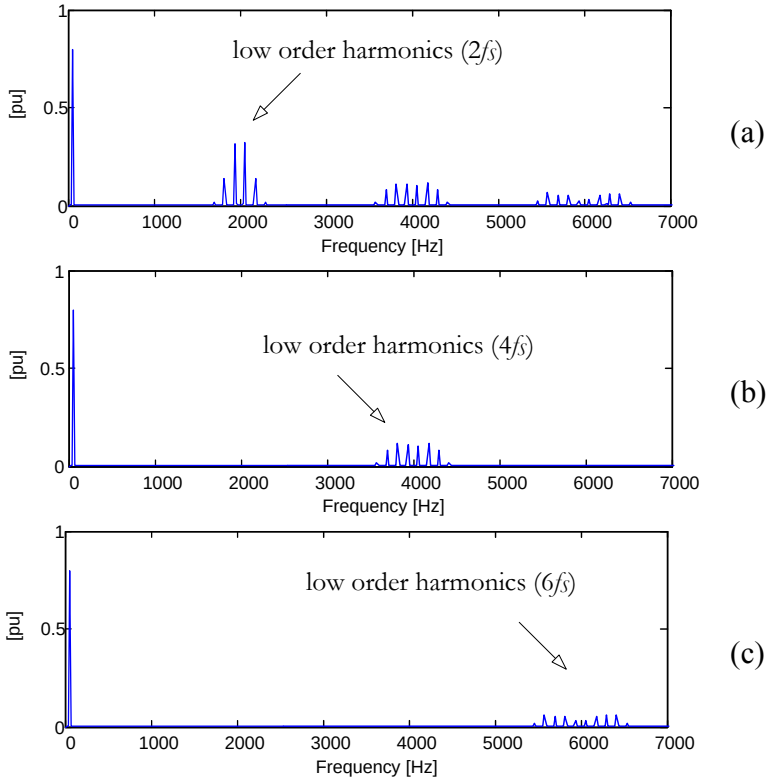


Figure 4.56 Harmonic spectra for multi-level unipolar VSC-1ϕ: (a) one, (b) two and (c) three VSCs

4.8.2 Three-phase PWM-VSC with multi-level output voltage

It is also possible to use multi-carrier waves to modulate three-phase converters. However, the transformers can have their converter side windings connected in Y or Δ. Figure 4.57(a) and (b) shows an example of the transformer connection for multi-level three-phase PWM-VSC. In this example we use four PWM-VSC-3ϕ.

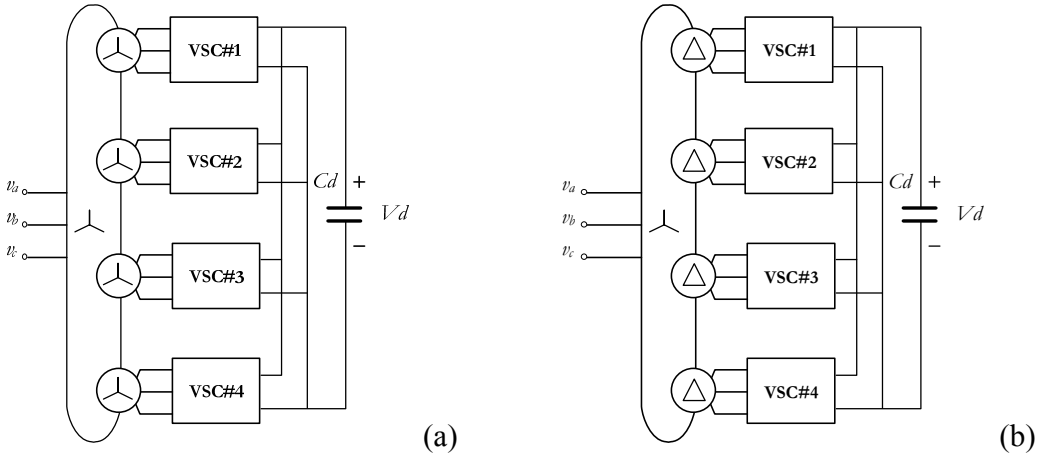


Figure 4.57 Three-phase multilevel PWM-VSC: transformers secondary connection in (a) Y and (b) Δ

Figure 4.58 and Figure 4.59 show the plots of the phase voltages and their harmonic spectra for the topologies of multi-level three-phase VSC shown in Figure 4.57. These figures are obtained for f_S = 1 kHz. It uses four triangular carrier waves phase-shifted by π/2 rad between them. Despite the better shape of the voltage in Figure 4.59(a) over the voltage in

Figure 4.58(a), the two voltages waveforms have the same harmonic content as can be viewed in Figure 4.58(b) and 4.59(b).

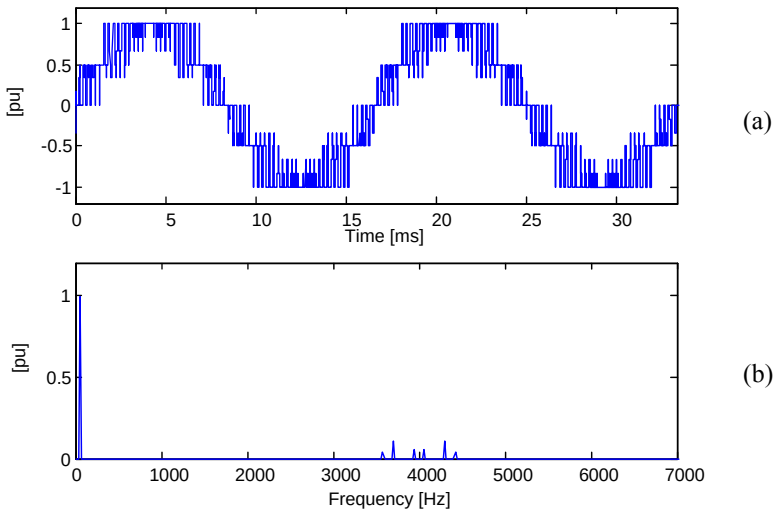


Figure 4.58 Multi-level output voltage for phase "a" of three-phase PWM VSC for Y connected transformer

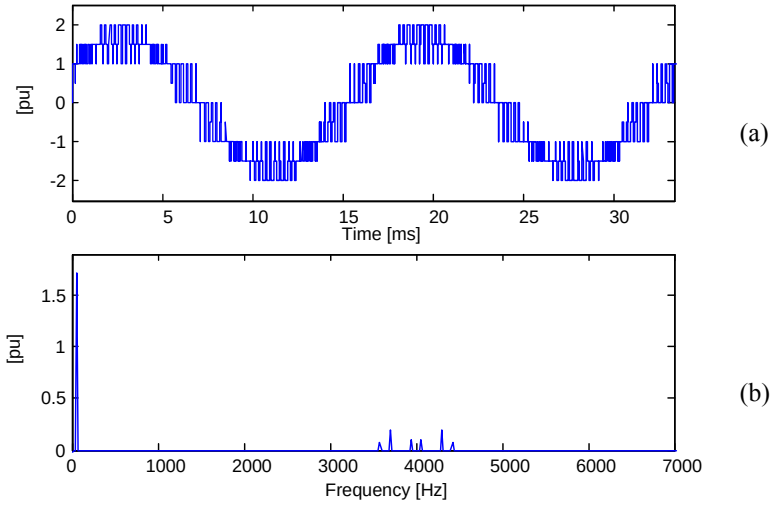


Figure 4.59 Multi-level output voltage for phase "a" of three-phase PWM VSC for Δ connected transformer

The comparison of the harmonic spectra in Figure 4.56(b) and Figure 4.59(b) shows that the single-phase PWM-VSC is equivalent to the three-phase PWM VSC. However, the three-phase PWM-VSC spectrum requires two times less semiconductor switches (4 x 3 = 12) than the 3× single-phase PWM-VSC (4 x 2 x 3 = 24). On the other hand the harmonic spectrum of the three-phase PWM-VSC deteriorates if the reference voltages of the VSC control are unbalanced. The same behavior is not observed in the converter configuration of Figure 4 because the synthesized voltages are independent from the others.

4.9 MULTIPULSE VSC WITH SELECTIVE HARMONIC ELIMINATION

This type of converter combines the multi-pulse technique, presented in Section 4.7, and the selective harmonic elimination (SHE), discussed in Section 4.5.3. Notches are introduced in the output voltage of the multipulse VSC to cancel some characteristic harmonics of the 6-pulse converters. Despite the fact that the switching frequency is increased, it is not expected to have a great change in the performance of the VSC.

Figure 4.60 shows a 12-pulse VSC controlled with a selective harmonic elimination technique. Thus, if each VSC of the multi-pulse converter has 3 notches per half cycle, it is possible to eliminate three harmonics of the 12-pulse VSC. In this case each VSC is switched with a frequency 7 times higher than the 6-pulse VSC (7 x 60 Hz = 420 Hz). Thus, making $M = 3$ and $n = 11$, 13, and 23 in (4.13), the following nonlinear system is obtained

$$\begin{cases} V_{11} = \left(\dfrac{4}{11\pi}\right) V_d \left[1 - 2\cos(11\alpha_1) + 2\cos(11\alpha_2) - 2\cos(11\alpha_3)\right] \\ V_{13} = \left(\dfrac{4}{13\pi}\right) V_d \left[1 - 2\cos(13\alpha_1) + 2\cos(13\alpha_2) - 2\cos(13\alpha_3)\right] \\ V_{23} = \left(\dfrac{4}{23\pi}\right) V_d \left[1 - 2\cos(23\alpha_1) + 2\cos(23\alpha_2) - 2\cos(23\alpha_3)\right] \end{cases} \tag{4.34}$$

Therefore, the angles α_1, α_2, and α_3 that cancel the 11^{th}, 13^{th}, and 23^{rd} harmonics are obtained solving (4.34) for $V_{11} = V_{13} = V_{23} = 0$, respectively.

Figure 4.61(a) shows the phase "a" output voltage of the 12-pulse VSC with selective harmonic elimination. In this figure the angles are $\alpha_1 = 4.14°$, $\alpha_2 = 11.95°$, and $\alpha_3 = 13.59°$. The total harmonic distortion in this case is lower than 6%. Figure 4.61(b) shows the harmonic spectrum of the phase voltage. Note that, neglecting the residues of the 25th and 47th harmonics, the 12-pulse VSC with SHE harmonic spectrum has a behavior close to the 36-pulse VSC, formed by six 6-pulse VSC connected in series.

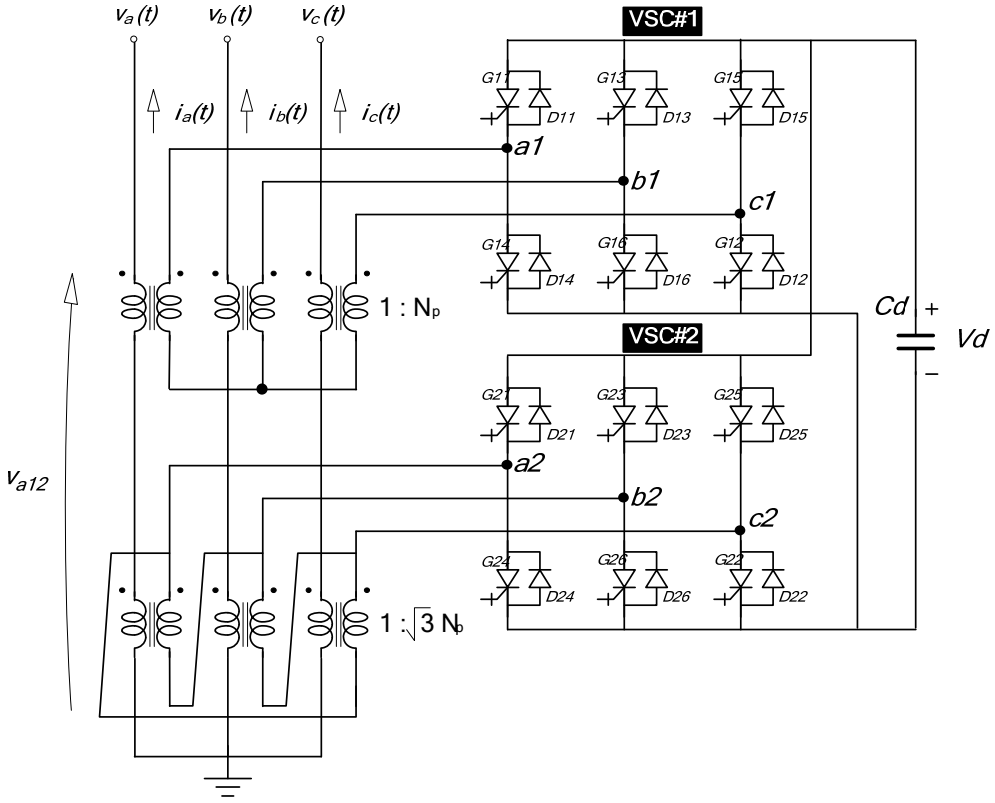


Figure 4.60 12-pulse VSC with 11th, 13th, and 23rd harmonics elimination

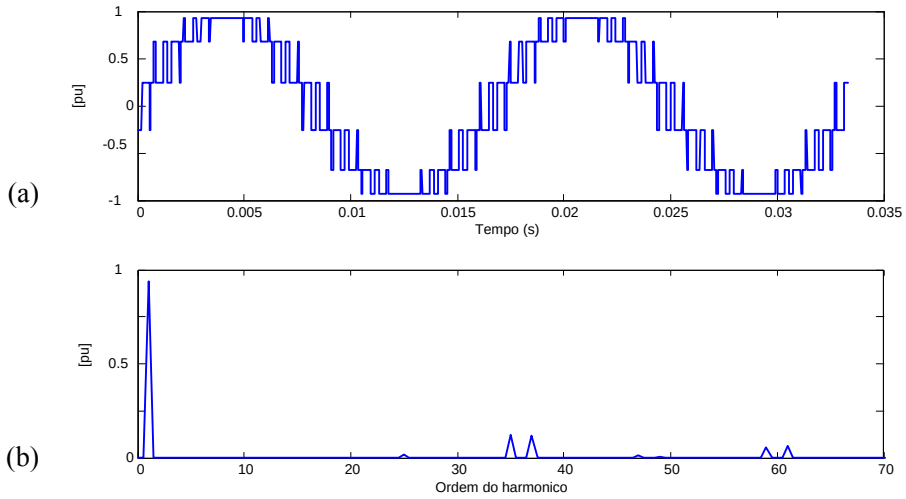


Figure 4.61 (a) Phase voltage of 12-pulse VSC with SHE; (b) harmonic spectrum

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CHAPTER 5. SSSC LOADFLOW AND DYNAMIC SIMULATION STUDIES

5.1 VSC CONTROLLER LOADFLOW MODELS

In loadflow and system stability studies, series VSC controllers introduce additional complexities, because the traditional loadflow model consists of only shunt injections and shunt voltage sources. As a result, to accommodate a series VSC controller installed on a transmission line, the decoupled FACTS controller loadflow model [5.1,5.2] uses a generator and a load to represent the series VSC controller, and the power injection model (PIM) [5.3,5.4] adds additional equivalent power injections at the from-bus and the to-bus of the series VSC controller in the conventional loadflow. However, both of these two bus injection models require additional computation effort in the regulation mode, and are not applicable to the fixed voltage injection mode or the rated capacity operation mode of the series VSCs.

On the other hand, the voltage source model (VSM) [5.5-5.7], where the VSCs are modeled directly as voltage sources, is intuitive and efficient. Directly using the voltage sources, the Newton-Raphson algorithm shows good convergence properties by simultaneously adjusting all voltage variables, without needing an outer loop for changing the equivalent injected bus power or current. Another advantage is that the line current and power are readily computed, allowing direct enforcement of device limits. The VSM is capable of modeling different operating modes of various VSC Controllers. Details of the voltage source model of the SSSC will be presented in this section.

5.2 BALANCED POSITIVE-SEQUENCE VOLTAGE SOURCE MODEL

The balanced positive-sequence steady-state operation of a SSSC can be modeled as an injected voltage source in series with the series transformer reactance, as shown in Figure 5.1. In addition to the notations used in Figure 1.2, the from-bus and to-bus of the SSSC are introduced.

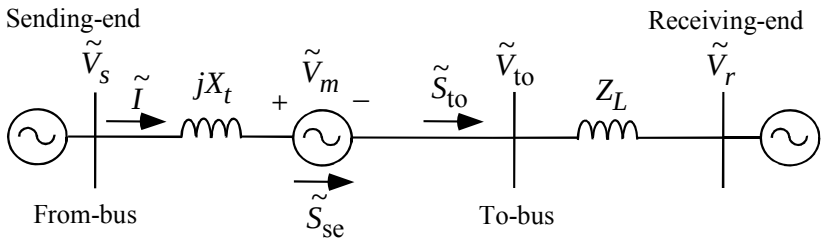


Figure 5.1 Injected voltage source model of the SSSC

The line current flowing through the series VSC is given by

$$\tilde{I} = \frac{\tilde{V}_s - (\tilde{V}_m + \tilde{V}_{to})}{jX_t} \tag{5.1}$$

such that the power injected by the series VSC is

$$\begin{aligned} S_{se} &= (\tilde{V}_s - \tilde{V}_{to})\tilde{I}^* = (\tilde{V}_s - \tilde{V}_{to})\frac{(\tilde{V}_s^* - (\tilde{V}_m^* + \tilde{V}_{to}^*))}{-jX_t} \\ &= \frac{\left|\tilde{V}_s - \tilde{V}_{to}\right|^2 - (\tilde{V}_s - \tilde{V}_{to})\tilde{V}_m^*}{-jX_t} \end{aligned} \tag{5.2}$$

and the power injected into the to-bus is

$$S_{\text{to}} = \tilde{V}_{\text{to}} \tilde{I}^{*} = \tilde{V}_{\text{to}} \frac{\tilde{V}_s^{*} - (\tilde{V}_m^{*} + \tilde{V}_{\text{to}}^{*})}{-jX_t} = \frac{\tilde{V}_{\text{to}} (\tilde{V}_s^{*} - \tilde{V}_m^{*}) - V_{\text{to}}^2}{-jX_t} \tag{5.3}$$

5.3 SSSC OPERATING MODES

As shown in Figure 1.4, the SSSC affects the active power transfer on the transmission line. It can be controlled in two different ways:

Se1. The SSSC controls the line active power flow P_{to} to a desired value P_{des},

$$P_{\text{to}} = V_{\text{to}} (V_m \sin(\theta_{\text{to}} - \alpha) - V_s \sin(\theta_{\text{to}} - \theta_s)) / X_t = P_{\text{des}} \tag{5.4}$$

where V_s, θ_s, V_{to}, and θ_{to} are the series branch from-bus and to-bus voltage magnitudes and angles, respectively, V_m and α are the series voltage injection magnitude and angle, respectively, and X_t is the equivalent series transformer winding reactance.

Se2. The injected voltage is kept at a fixed voltage magnitude, in either the quadrature leading or lagging direction with respect to the transmission line current

$$V_m = V_{m\text{des}} \tag{5.5}$$

In both control modes, the active power injected into the transmission line by the SSSC is zero

$$P_{\text{se}} = 0 \tag{5.6}$$

which can also be expressed as

$$V_s \sin(\theta_s - \alpha) - V_{\text{to}} \sin(\theta_{\text{to}} - \alpha) = 0 \tag{5.7}$$

In (5.6) the VSC losses are neglected. Active power can be injected into the transmission line if the series VSC has an energy storage system connected to the DC capacitor or it is connected to the DC bus of another VSC.

5.4 NEWTON-RAPHSON LOADFLOW SOLUTION

In an *N*-bus power network with N_g generators and without any VSCs, the loadflow equations can be formulated as *N*-1 equations for the active power bus injections/loads *P* and *N*- N_g equations of reactive power bus injections/loads *Q*

$$\begin{aligned} f_P(v) &= P \\ f_Q(v) &= Q \end{aligned} \tag{5.8}$$

where

$$v = \begin{bmatrix} V_1 & V_2 & \dots & V_N & \theta_1 & \theta_2 & \dots & \theta_N \end{bmatrix}^T \tag{5.9}$$

is a $2N$-N_g-1 vector variable of bus voltage magnitudes and angles, with N_g generator bus voltages removed and the angle of the swing bus set to 0^{o}. The Jacobian used in the Newton-Raphson solution is

$$J = \begin{bmatrix} \partial f_P / \partial V & \partial f_P / \partial \theta \\ \partial f_Q / \partial V & \partial f_Q / \partial \theta \end{bmatrix} \tag{5.10}$$

When the *N*-bus power network also includes *M* VSCs, then the loadflow equation (5.8) will expand by 2*M* equations, resulting in

$$\begin{aligned} \bar{f}_P(\bar{v}) &= P \\ \bar{f}_Q(\bar{v}) &= Q \\ \bar{f}_{\text{VSC}}(\bar{v}) &= R \end{aligned} \tag{5.11}$$

where

$$\bar{v} = [V_1 \quad \ldots \quad V_N \quad \theta_1 \quad \ldots \quad \theta_N \quad V_{m1} \quad \ldots \quad V_{mM} \quad \alpha_1 \quad \ldots \quad \alpha_M]^T \tag{5.12}$$

is a $2(N+M)-N_g-1$ vector variable of bus voltage magnitudes and angles, and the third and last equation in (5.11) is determined by the VSC operating modes, where R is a vector of the FACTS Controller setpoints or reference values. In this approach, the P and Q expressions in (5.11) will remain unchanged for all operating modes.

To apply the Newton-Raphson algorithm to the augmented system (5.11), the Jacobian matrix J (5.10) is expanded to

$$\bar{J} = \begin{bmatrix} \partial\bar{f}_P/\partial V & \partial\bar{f}_P/\partial\theta & \partial\bar{f}_P/\partial V_m & \partial\bar{f}_P/\partial\alpha \\ \partial\bar{f}_Q/\partial V & \partial\bar{f}_Q/\partial\theta & \partial\bar{f}_Q/\partial V_m & \partial\bar{f}_Q/\partial\alpha \\ \partial\bar{f}_{\text{VSC}}/\partial V & \partial\bar{f}_{\text{VSC}}/\partial\theta & \partial\bar{f}_{\text{VSC}}/\partial V_m & \partial\bar{f}_{\text{VSC}}/\partial\alpha \end{bmatrix} \tag{5.13}$$

Note that the first 2x2 blocks of $\bar{J}$ (namely, the (1,1), (1,2), (2,1), and (2,2) entries) are identical to the Jacobian J in (5.10), except for the additional terms due to the shunt and series VSC transformer reactances and injection terms. Thus an attractive feature of this Newton-Raphson algorithm for solving loadflow is that the formulation (5.11) to (5.13) can be readily built into a conventional Newton-Raphson algorithm. For large data sets, sparse factorization techniques can be used to achieve an efficient solution.

5.5 Operating Limits

The operating limits are imposed on the loadflow computation to ensure that the VSCs are not overloaded, and that the voltages of the adjacent buses are within an acceptable range. For the SSSC, the operating limits include:

- the maximum series injected voltage,
- the maximum series line current,
- the series VSC MVA rating,
- the maximum and minimum voltage magnitudes at adjacent buses, and
- the maximum power transfer between the converter and the energy storage system, if the series VSC is coupled with an energy storage system.

If any of these limits are violated, the voltage or flow setpoints of the SSSC can no longer be enforced.

5.6 Coupling Series VSC to Energy Storage Devices and Other VSCs

An important feature of a VSC is its ability to exchange active power with other controllers such as energy storage devices and VSCs by linking its DC bus to these controllers. For example, if the DC bus of the SSSC is linked to an energy storage system, such as a battery park, then the active power injected into the line, instead of (5.6), will become

$$P_{\text{se}} = P_{\text{ES}} \tag{5.14}$$

A similar effect can be achieved by coupling the series VSC to a shunt VSC. When the DC capacitors of the series and shunt VSCs are connected, forming a Unified Power Flow Controller (UPFC), active power can be absorbed by the shunt VSC and circulate to the series VSC as

$$P_{\text{sh}} + P_{\text{se}} = 0 \tag{5.15}$$

With this additional dispatch flexibility, the line active and reactive power flow can be independently controlled by the series VSC. Furthermore, the power circulation can be a useful parameter in maximum power transfer dispatch. As in the series VSC, equations (5.14)-(5.15) can be readily incorporated into the Newton-Raphson loadflow solution algorithm.

5.7 SSSC DISPATCH EXAMPLE

Consider the four-bus radial system in Figure 5.2, where a 100 MVA series VSC is located between Buses 2 and 4 to enhance the power transfer capability from the generator on Bus 1 to the load on Bus 3. The maximum series line current and injected voltage of the series VSC are 10 pu and 0.1 pu on the system base, respectively. The maximum and minimum voltage magnitudes at adjacent buses are 1.5 pu and 0.5 pu, respectively. The maximum power transfer between the converter and the energy storage system is 10 MW. All the other system parameters are included in Table 5.2 in the Appendix 5.1.

Note that by closing Switch B the SSSC is bypassed, which is referred to as the uncompensated system (base case). The SSSC is in service if Switch B is open. By also closing Switches S1 and S2, the SSSC is coupled with an energy storage system.

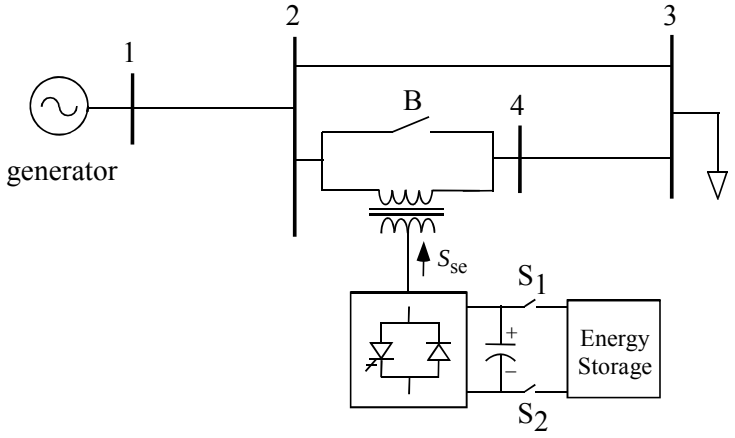


Figure 5.2 Four-bus system with a series VSC

Because the VSC is a reactive power source, the objective is to show the impact of the VSC on the system voltage stability as the power transfer on the transmission lines is increased. As a base case, Switch B is closed so that the VSC is not deplored. Figure 5.3 shows the variation of the voltage V_3 at Bus 3 when the load L_3 on Bus 3 is increased from the base value of 400 MW. In particular, V_3 drops to 0.95 pu when L_3 reaches about 565 MW.

Next, Switch B is opened with Switches S1 and S2 open and the SSSC is inserted to carry 62% of L_3. As shown in Figure 5.3, V_3 drops to 0.95 pu when L_3 reaches about 615 MW, showing a 50 MW increase in the power transfer. Figure 5.4 shows the magnitude of the injected voltage as a function of the power dispatch. Note that the injected voltage V_m reaches the maximum value of 0.1 pu (on the system base) at 510 MW and remains at the maximum value for higher values of power transfer.

Then Swtiches S1 and S2 are closed to form a SSSC with energy storage system. The load L_3 on Bus 3 is again increased from the base load of 400 MW, with 62% carried on the series VSC. The dispatch results are shown in Figures 5.3. Without any power circulation, that is, the active power flowing out of the energy storage system into the series VSC is zero, the dispatching is exactly the same as the SSSC without energy storage system, showing a 50 MW increase in power transfer when V_3 drops to 0.95 pu compared with the base case. Furthermore, by circulating 10 MW from the energy storage system to the series VSC, the power transfer is improved by another 30 MW. On the other hand, if active power circulates from the series VSC to recharge the energy storage system, the power transfer is decreased. The magnitude of the injected series voltage source for the three cases of power circulation is shown in Figure 5.4, depicting the saturation of the inserted voltage magnitude.

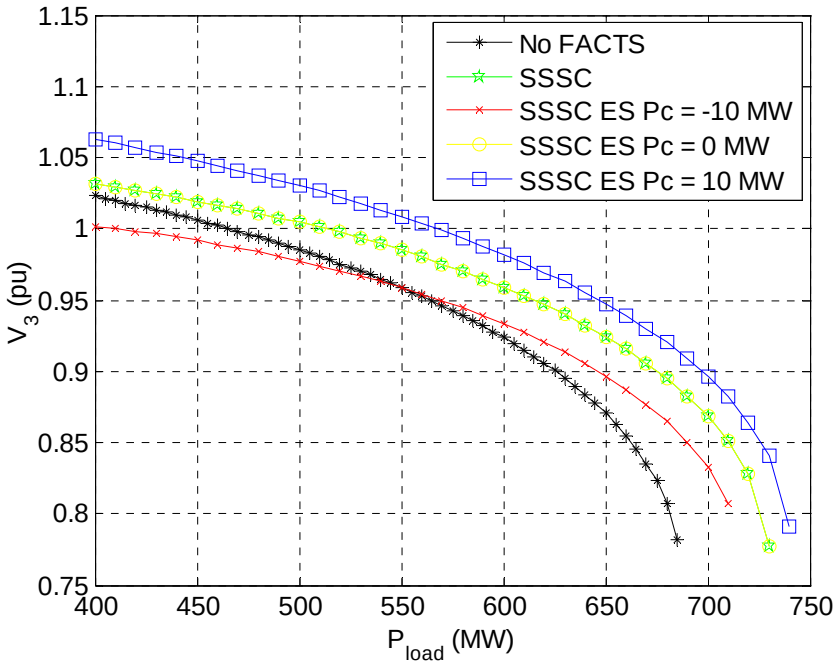


Figure 5.3 PV characteristic of the SSSC without and with energy storage

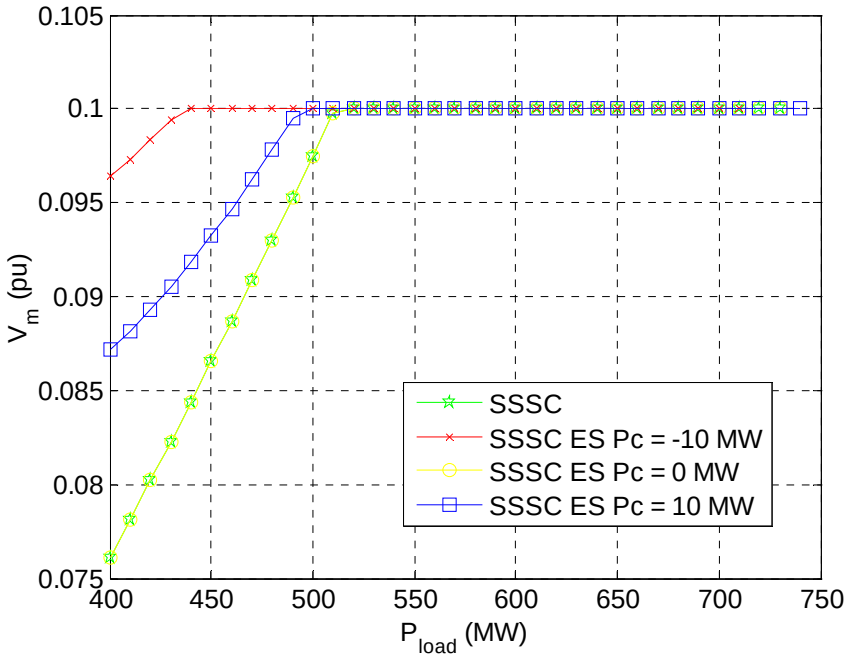


Figure 5.4 Series VSC injected voltage magnitude

5.8 SSSC DYNAMIC MODEL

Figure 5.5 shows the schematic diagram of the SSSC, where γ_{se} is the conversion ratio signal to control the series converter voltage magnitude, and α_{se} is the phase angle of the series VSC. Note that α_{se} is measured with respect to the angle of the from-bus voltage phasor $\tilde{V}_1$.

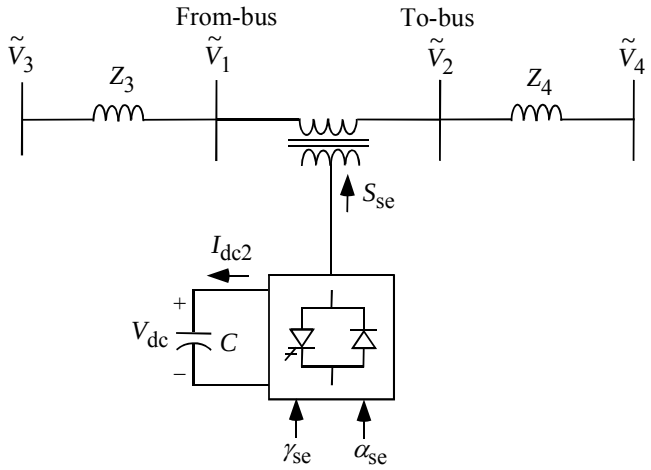


Figure 5.5 Series voltage-sourced converters showing DC capacitor

In the time scale of transient stability analysis, in which the VSC switching dynamics are neglected, the voltage insertion model of the series VSC can be represented as

$$\tilde{V}_m = kV_{dc}e^{j(\alpha_{se}+\theta_1)} = V_m e^{j\alpha} \tag{5.16}$$

where k is a factor which relates the inverter DC-side voltage to its AC-side terminal voltage, and θ_1 is the angle of $\tilde{V}_1$. Note that k is dependent on the ratio γ_{se}.

The dynamic balanced positive-sequence model of the SSSC is shown in Figure 5.6.

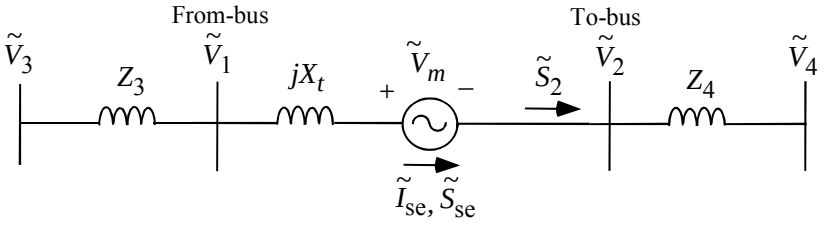


Figure 5.6 SSSC balanced positive-sequence model

The series VSC is modeled as a controllable injected voltage source $\tilde{V}_m$ behind an equivalent transformer reactance X_t. The line current $\tilde{I}$, the power $\tilde{S}_{se}$ injected by the series VSC, and the power $\tilde{S}_2$ injected into the to-bus (Bus 2) are the same as given in (5.1-5.3) for the steady-state series VSC model, respectively.

During transient stability studies, the DC link capacitor of the SSSC will exchange energy with the AC system and consequently its voltage varies. The variation of the DC capacitor voltage is dependent on its current inflow, which can be modeled as

$$C\frac{dV_{\mathrm{dc}}}{dt} = I_{\mathrm{dc}} \tag{5.17}$$

where I_{dc} is the current flowing into the DC capacitor from the VSC and C is the capacitance of the DC capacitor. In steady-state operation the power transfer is balanced, and hence, $I_{\mathrm{dc}} = 0$ and $dV_{\mathrm{dc}} / dt = 0$.

The SSSC dynamic model will be interfaced with the other dynamic components in a power system, such as synchronous machines and excitation systems, through the power network. In using injected voltage source for the VSC in the loadflow formulation, this transition to dynamic model will be seamless, because $\tilde{V}_m$ is a variable in the loadflow model.

The AC instantaneous active power injected into the power system for the SSSC is given by (5.6) and (5.14) for a SSSC and a SSSC linked with an energy storage system, respectively. Assuming that the VSC model is ideal, the AC instantaneous active power in the AC-side is equal to the DC-side active power, that is

$$P_{\mathrm{se}} = V_{\mathrm{dc}} I_{\mathrm{dc}} \tag{5.18}$$

From (5.17) and (5.18), we have

$$\frac{dV_{\mathrm{dc}}}{dt} = \frac{1}{CV_{\mathrm{dc}} P_{\mathrm{se}}} \tag{5.19}$$

Equation (5.19) is in general not per-unitized.

The block diagram of the DC link dynamics is shown in Figure 5.7.

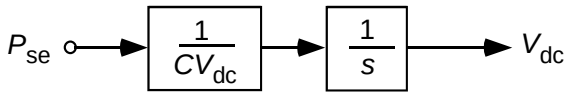
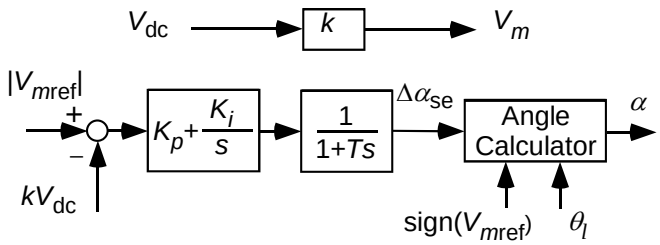
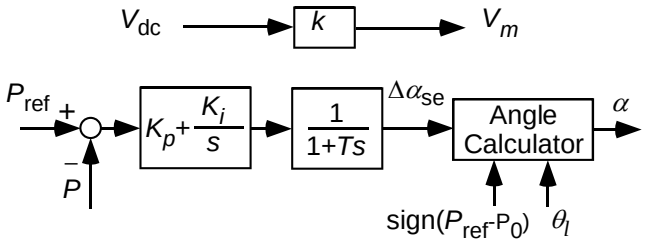


Figure 5.7 DC link dynamics

The SSSC can be either in the line active power control mode or the inverter voltage magnitude control mode. The block diagrams for these two modes are shown in Figures 5.8 (a) and (b), respectively. The magnitude V_m and the angle α of the inverter voltage are generated by the control systems.



(a) Inverter voltage magnitude control mode



(b) Line *P* control mode
Figure 5.8 SSSC setpoint control diagrams

The SSSC is operated with a constant conversion factor k between its AC-side voltage V_m and DC-side voltage V_{dc}, and hence the changes in the magnitude of the inverter output voltage are achieved by charging or discharging the DC bus capacitor to a different voltage.

A PI controller $K_p + K_i / s$ and a LP filter $1/(1+T \cdot s)$ are applied in the angle control loop of the SSSC. The input signal for the line active power control mode is the difference of the line active power setpoint P_{ref} and its measured value P, while the input signal for the inverter voltage magnitude control mode is the difference of the inverter voltage magnitude setpoint $|V_{mref}|$ and kV_{dc}. In each operating mode, the output signal from the LP filter is the angle deviation $\Delta\alpha_{se}$. In steady state, $\Delta\alpha_{se}$ is zero, implying that the inverter output voltage is kept essentially in quadrature with the current of the compensated line. Small transient positive or negative deviations in the phase angle of the inverter voltage will cause nonzero active power to go through the DC capacitor and thus result in changing the DC bus voltage.

5.9 SSSC DYNAMIC SIMULATION

The dynamic model of the SSSC is simulated in a 22-bus test system as shown in Figure 5.9, which has 6 equivalent generators and 3 equivalent loads. The loads of the test system are concentrated in the Southeast part of the system, while the generations are mainly in the Northwest area. The arrows indicate the directions of the active power flow. A 100 MVA SSSC can be inserted into Line 4-11, which is a major path between the generators and the loads. Note that the system base is 100 MVA. In the dynamic simulation, the generators are modeled as the voltage behind sub-transient reactance model with a simple voltage regulator control. The loads are modeled as constant impedance.

In order to evaluate the maximum power transfer capability of the critical paths in the 22-bus system, we stress the system by increasing the active power consumption of Load L2 on Bus 17, to be supplied by Generators G1, G2, and G3. The initial value of Load L2 is 2500 MW. Line 3-13, which is a line paralleled with Line 4-11, is tripped at time *t*=0.1 s. The maximum load on Bus 17 that the system can withstand for this disturbance and the corresponding power transfers on Line 4-11 and Line 4-12 for the system configurations without and with the SSSC are displayed in Table 5.1. The setpoint for the SSSC is simply specified based on its rated capacity.

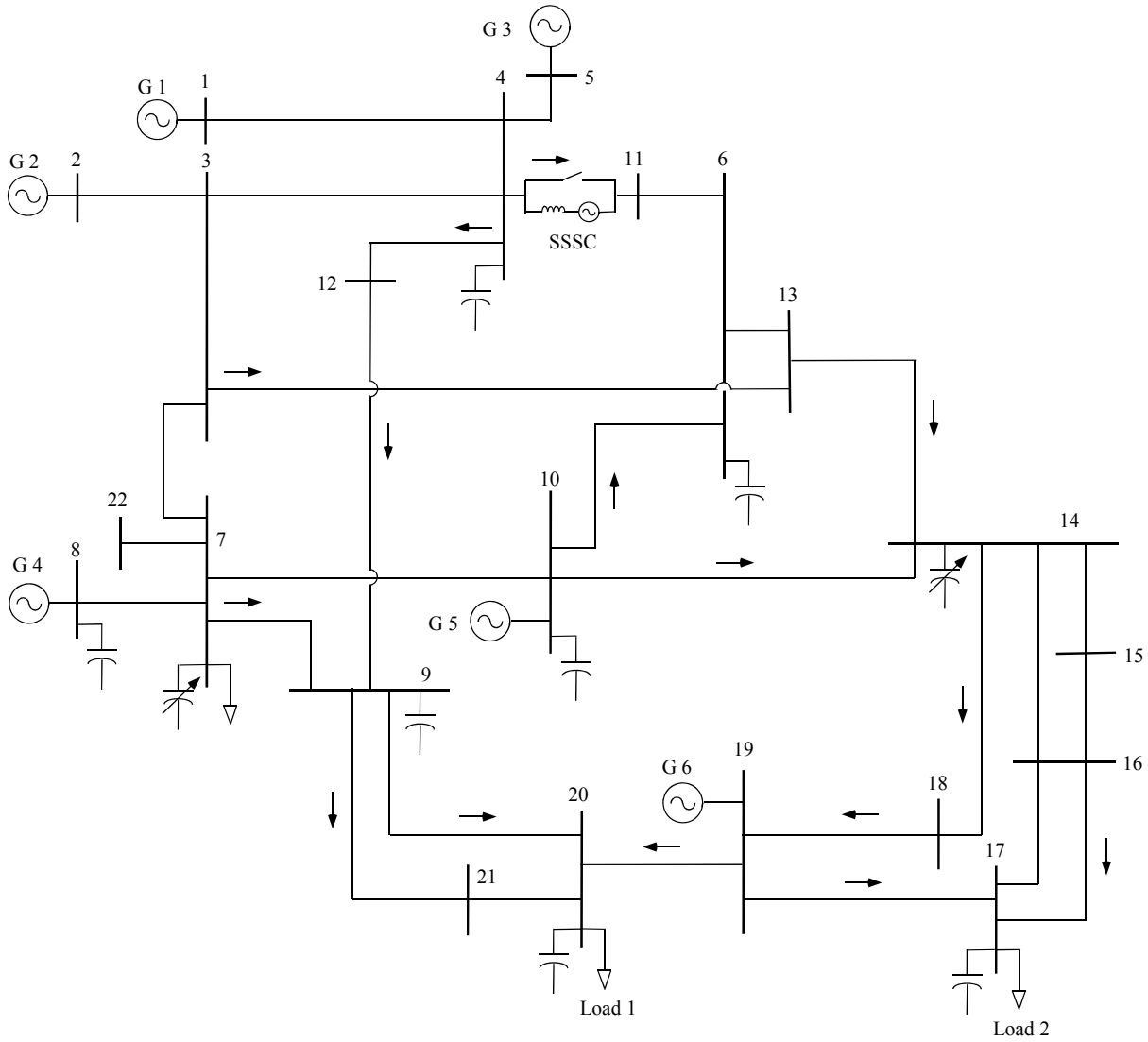


Figure 5.9 22-bus test system

Table 5.1
Comparison of transient transfer capability with and without a SSSC

Configuration	Setpoint	Maximum Load on Bus 17 (MW)	Line Power Transfer (MW)	
			Line 4-11	Line 4-12
No SSSC	-	3236.5	1383.8	903.2
SSSC 100 MVA, L4-11 Inverter V_m Control	V_{mref} = -0.055 pu	3278.5	1454.3	896.6

As shown in Table 5.1, a SSSC with 100 MVA rating can support over 40 MW more load on Bus 17 than the configuration without the SSSC. The corresponding power flow on Line 4-11 increases about 70 MW while that on Line 4-12 decreases about 7 MW.

If the SSSC is operated in the line active power control mode, when the load on Bus 17 is sufficiently high, the dynamic simulation will terminate due to the non-convergence of the network solutions, because of the lack of reactive power support. So the SSSC should be operated in the inverter V_m control mode.

Figure 5.10 shows the dynamic simulations of configurations without and with the SSSC in the same loading conditions where the active power of Load L2 on Bus 17 is 3236.5 MW. The SSSC is operated in the inverter V_m control mode and its setpoint is given in Table 5.1. The SSSC reduces transient oscillations in the voltages on Bus 3 and Bus 4 and the power flows on the critical paths Line 4-11 and Line 4-12 during the tripping Line 3-13, which allows it to increase the transfer capability of the system.

To summarize, a SSSC can substantially improve the transient power transfer capability of a transmission system during a system change.

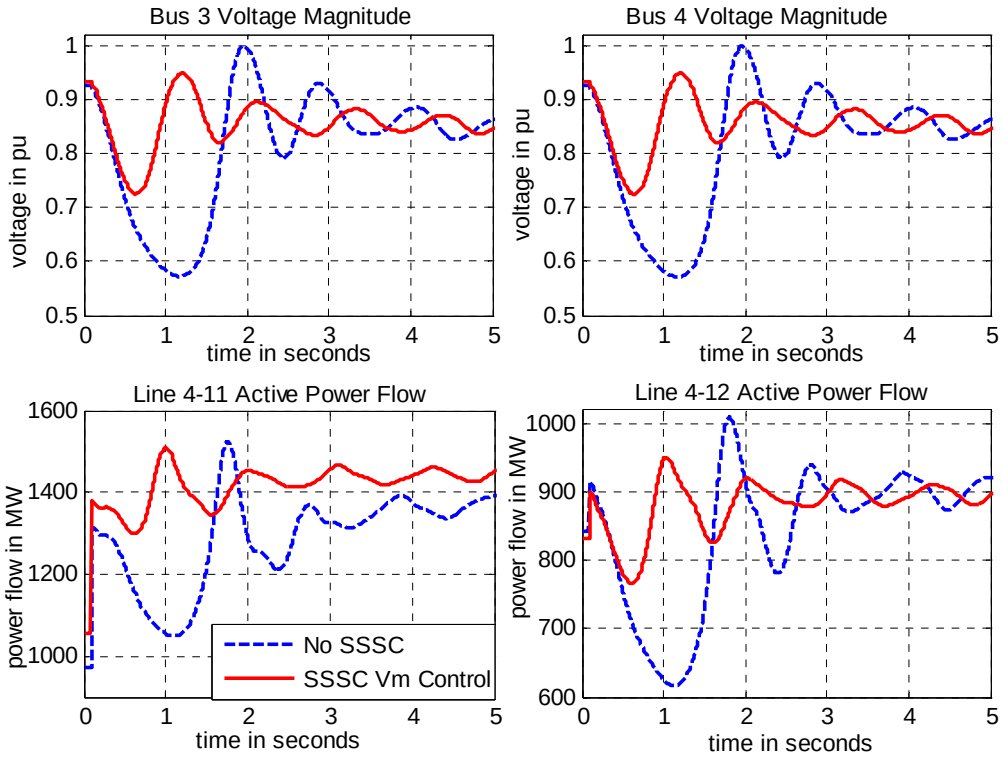


Figure 5.10 Comparison of time responses without and with a SSSC in the V_m control mode when P_{L2}=3236.5 MW

APPENDIX 5.1 4-BUS RADIAL SYSTEM PARAMETERS

All network parameters in Table 5.2 are given on a base of 100 MVA.

TABLE 5.2
Transmission line data

Line	Resistance (pu)	Reactance (pu)	Charging (pu)
1-2	0.00163	0.03877	0.78800
2-3	0	0.08154	0.39400
3-4	0	0.07954	0.39400

The SSSC transformer leakage reactance is X_t = 0.002 pu.

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CHAPTER 6. EMTP SIMULATIONS OF SSSC

6.1 INTRODUCTION

In the past, electromagnetic transient studies in power system were traditionally performed using transient network analyzers (TNA). Nowadays, due to the development of high-capacity, high-speed digital computers, these studies are normally carried out using digital simulation packages. The applications of electromagnetic transient methods have being frequently reported in many international journals and conference proceedings. They are normally classified as frequency-domain and time-domain based techniques [6.1].

At the present time there are a large variety of commercial and academic simulation packages to solve electromagnetic transient problems in power system. Electromagnetic Transients Program (EMTP), Electromagnetic Transients Program for DC (PSCAD/EMTDC), MicroTran, Alternative Transients Program (ATP) among others are examples of these programs. Most of them have graphical interfaces to simplify the simulation task [6.2].

The aim of this chapter is to present some results of a time-domain model of a multi-level PWM Static Synchronous Series Compensator (PWM-SSSC) obtained in ATP (Alternative Transients Program). ATP is a variant of the EMTP package and its choice was based on the fact that it is a royalty-free program.

There are a number of available built-in circuits in the ATP such as sources, linear and non-linear elements, transformers, transmission lines, and electric machines, etc. Devices such as diodes and forced-commutated semiconductor devices like GTOs (Gate Turn-off Thyristors) and IGBTs (Insulated Gate Bipolar Transistors) can only be represented by their idealized characteristics. However, this model limitation cannot be viewed as a problem at the system level. The control systems can be easily represented in terms of their transfer functions and FORTRAN-like statements in the TACS (Transients Analysis of Control Systems) environment. The control algorithms can be also represented in MODELS environment where the instructions are written as a computer program.

The ATP uses the "trapezoidal rule" as its numerical integration method and as a consequence it is susceptible to numerical oscillations. Thus, a user should be aware of these potential oscillations when simulating power electronics circuits and systems such as SSSC and other FACTS devices. One option to eliminate these oscillations is to use of numerical snubbers connected in parallel with the switching elements. These snubbers remove or reduce numerical oscillations because they provide an alternate current path for the inductive current, resulting in a damped RLC circuit.

Recently the ATP had incorporated a graphic interface named ATPDraw. In the graphical environment the components are dragged and dropped to the work area and they can be easily connected to each other to build the system. The ATPDraw produces the source code of a circuit for ATP simulation. Figure 6.1 shows some of the components available in the ATPDraw.

6.2 MULTILEVEL PWM-SSSC

Figure 6.2 shows the single-line diagram of the double-line circuit modeled in the ATP/ATPDRAW simulation package [6.3]-[6.5]. A multilevel PWM-SSSC is connected to the sending-end side of a 200 km AC transmission line whose parameters are given in Table 5.1. The PWM-SSSC can be controlled to inject or absorb reactive power (Q_C), to synthesize a positive or negative controllable magnitude and phase voltage ($\boldsymbol{V}_C$), or to emulate a positive or negative reactance (jX_C) in series with the AC line. In this figure the source and the load are modeled by two ideal three-phase voltage sources in series with a series reactance and phase-shifted by $\pi/3$ rad.

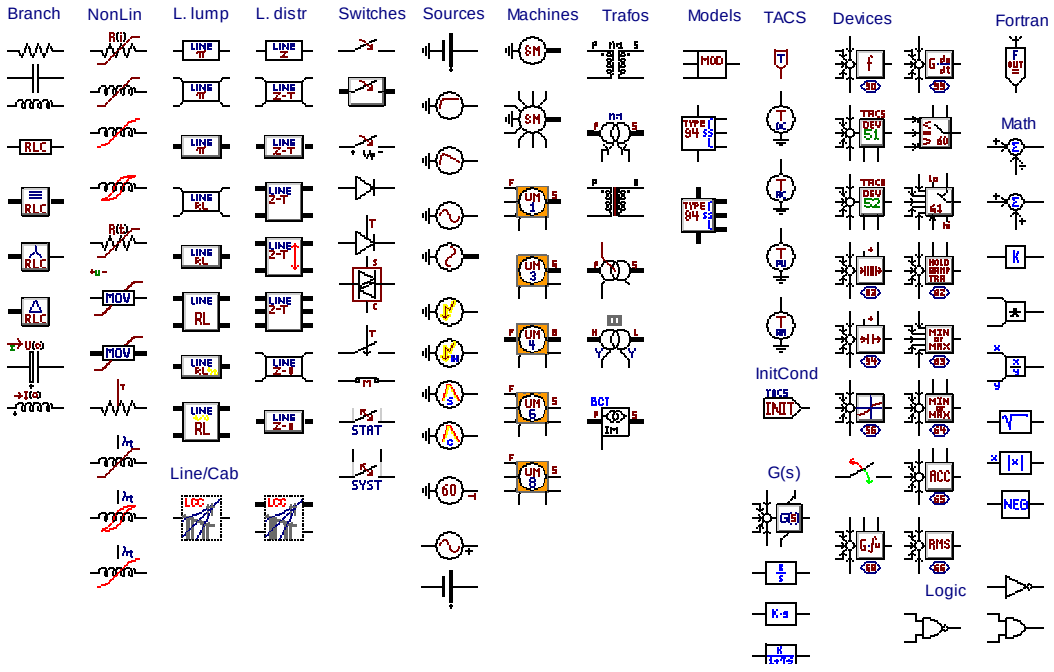

Figure 6.1 Some components available in ATPDraw environment

Table 6.1 Transmission line parameters

Component	R (Ω/km)	L (mH/km)	C (μF/km)
Zero sequence	0.03167	3.2220	0.00787
Positive sequence	0.01430	0.9238	0.01260

The multilevel PWM-SSSC of Figure 6.2 is composed of four single-phase VSC per phase, with unipolar voltage outputs. The GTOs were modeled by TACS controlled switches with anti-parallel diodes and numerical snubbers. All transformers have a unitary turns-ratio. Four triangular carrier waves are used to obtain the frequency multiplication effect explained in the multilevel PWM section. These triangular carrier waves are phase-shifted by π/2 rad between them.

6.3 PWM SSSC CONTROL ALGORITHM

The active power flowing through the compensated transmission line of Figure 6.2, considering $\boldsymbol{V}_C = 0$, $\boldsymbol{V}_S = |V|e^{+j(\delta/2)}$, and $\boldsymbol{V}_R = |V|e^{-j(\delta/2)}$ and neglecting the harmonics generated by the multi-level PWM-SSSC and the losses of transmission line, is given by

$$P = \frac{V^2}{X_L}\sin(\delta) \qquad (6.1)$$

Because the SSSC can be continuously controlled to inject an AC voltage (V_C) leading or lagging by π/2 rad with respect to the line current, the transmitted active power P_q through the compensated line can be rewritten as

$$P_q = \frac{V^2}{X_L}\sin\delta - \frac{V}{X_L}V_C\cos(\delta/2) \qquad (6.2)$$

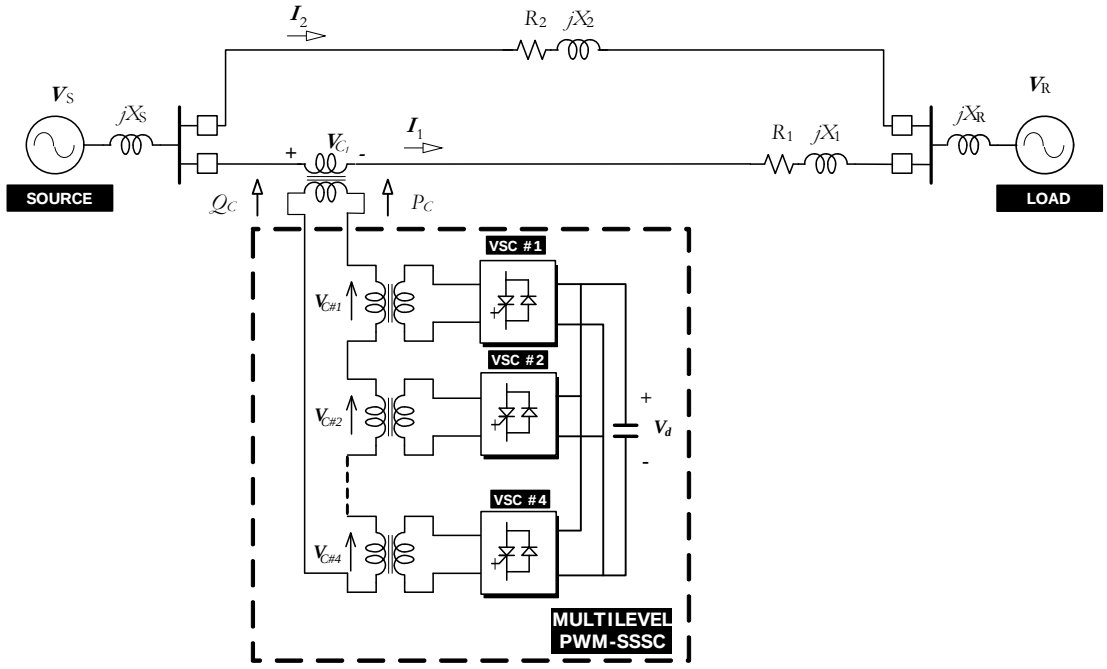

Figure 6.2 Single line diagram of the modeled system with the multilevel PWM-SSSC

Normalizing (6.2) with respect to the active power flowing through the AC line for $\boldsymbol{V}_C = 0$ results in

$$\frac{P_q}{P} = 1 - \frac{V_C}{V_C + V_L} \tag{6.3}$$

where V_L is the voltage drop across the line reactance. Multiplying both sides of (6.3) by the line current yields

$$\frac{P_q}{P} = \frac{Q_L}{Q_C + Q_L}, \tag{6.4}$$

where Q_L is the reactive power absorbed or generated by the AC line (var) and Q_C is the reactive power (var) injected in series by the SSSC. Thus, if $Q_L > 0$, the active power flowing through the compensated AC line increases if $Q_C < 0$. Otherwise, if $Q_C > 0$, the active power P_q flowing over the ac line decreases.

Figure 6.3 shows the block diagram of the controller of the PWM-SSSC. The control algorithm is implemented in the TACS (*Transient Analysis of Control System*) environment. A transformation is applied to the three-phase line currents before they, and the reference active (p*) and reactive (q*) powers, feed the SSSC Reference Voltages block. The generated reference voltages are transformed to three-phase quantities and they are sent to the PWM controller and Gate Signal Generator block. The PWM Controller is also fed by four triangular waves displaced by π/2 rad between them.

The DC Voltage Regulator adds an extra control signal to the reference active power signal (p*) to assure that the SSSC will absorb or supply some active power from the power system in such a way as to control the DC voltage of the multi-level VSC.

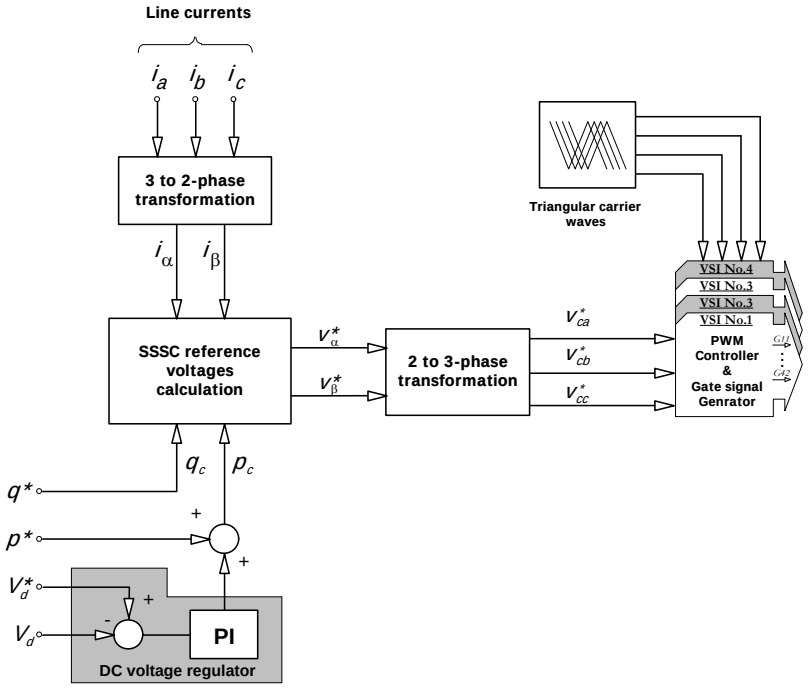

Figure 6.3 Block diagram of the multilevel PWM-SSSC

The PWM Controller and Gate Signal Generator are implemented for one branch of the PWM-SSSC as shown in Figure 6.4. The Sample-and-Hold block is used to decouple the gate signals of the semiconductor switches. Because each single-phase VSC uses two PWM Controllers, twenty-four (4x3x2 = 24) blocks, similar to that shown in Figure 6.4, are used to control the multi-level PWM-SSSC.

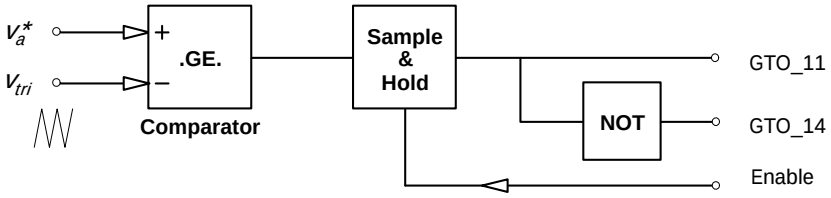

Figure 6.4 PWM Controller and Gate Signal Generator

6.4 DIGITAL SIMULATION RESULTS

Each branch of single-phase VSC of the multi-level PWM-SSSC is switched with 1 kHz. The VSC DC link capacitance was chosen equal to 2000 μF. The average DC voltage of the multi-level PWM-VSC is set to 9.4 *kV*. Despite the better voltage waveform of the multi-level SSSC, passive filters, similar to that shown in Figure 6.5, are connected between the multi-level VSC output terminals and each series transformer to cut off high-order harmonics due to the switching of the converters. These filters were designed with a 3162 rad/s of cut-off frequency.

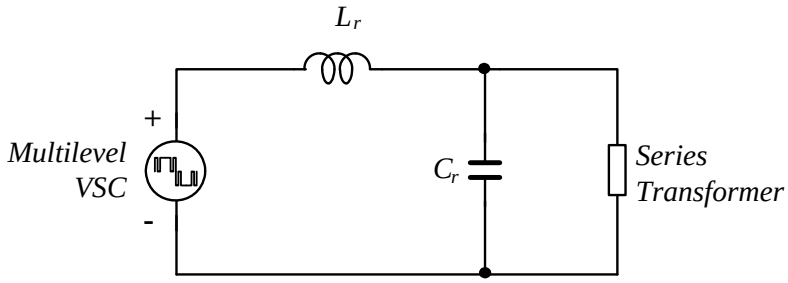

Figure 6.5 Second order passive filter

Figure 6.6(a) and (b) shows the active and reactive powers at the PWM-SSSC terminals. Initially the PWM-SSSC has a null compensation characteristic. At t = 100 ms the reference reactive power signal is step-changed from 0 to –50 Mvar (capacitive characteristic). At t = 200 ms the reference reactive power is changed from –50 Mvar to +50 Mvar. Then the SSSC operates with an inductive characteristic. Finally, at t = 300 ms the reactive reference power is reduced to zero again and the compensator return to null compensation characteristic. All curves are normalized to 100 MVA and 1000 A.

Figure 6.7(a), (b), and (c) present the line currents through the compensated ac line, where it is possible to see that these currents increase for 100 ms < t < 200 ms during capacitive compensation. For 200 ms < t < 300 ms the line currents decrease due to the inductive compensation and for t > 300 ms they return to the uncompensated level. Figure 6.8(a), (b), and (c) show the compensating voltages of the PWM-SSSC. The ripples on these voltages are due to the switching for the PWM modulation. Figure 6.9(a) and (b) show the active and reactive power flowing in the compensated transmission line. Because no feedback control is used there is a small oscillation in these responses due to the transmission line characteristics when step-like capacitive or inductive compensation is introduced. Figure 6.10 shows the reference voltage, compensating voltage, and line current for a capacitive compensation. The difference between the reference voltage and the synthesized voltage is basically the switching ripple. It is clear from this figure that the line current is leading the compensation voltage by 90°. Figure 6.11 presents the total harmonic distortion (THD) at the SSSC terminals voltage considering its fundamental voltage as reference. This fact makes this THD reach almost 3.5% which is not too high, but, generally, cannot be neglected. However, if the transmission line voltage is considered, this THD falls to a very small value and, from the point of view of the transmission system it can be neglected without problem. Finally, Figure 6.12 shows the behavior of the SSSC DC link voltage. During the time the SSSC is operating, its control system is able to keep the DC voltage controlled, although a small amount of ripples appears on it.

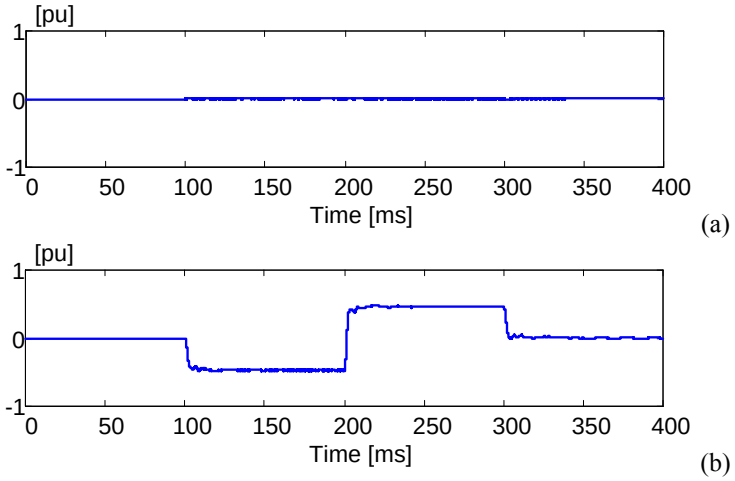

Figure 6.6 (a) Active power (W); (b) reactive power (var) at the PWM-SSSC terminals

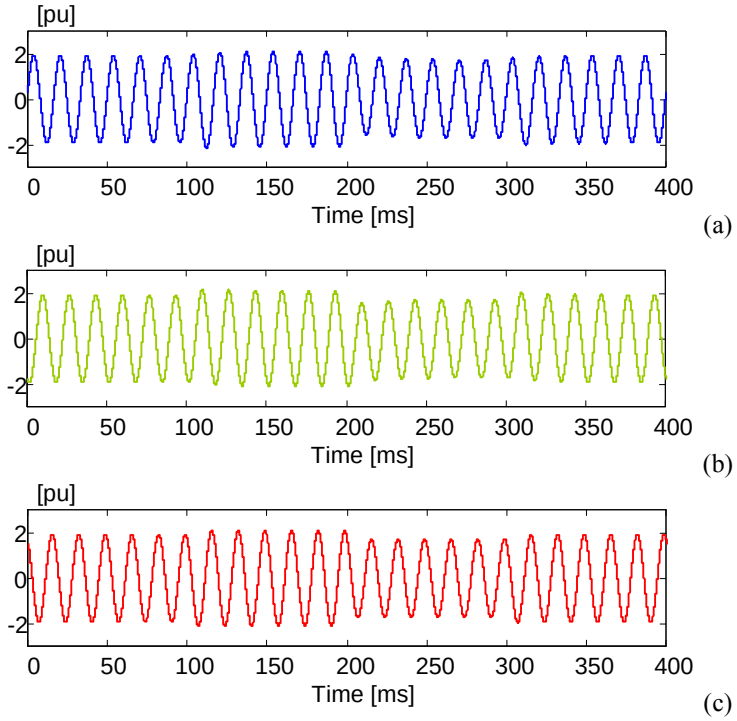

Figure 6.7 Three-phase line currents: (a) i_a, (b) i_b, and (c) i_c

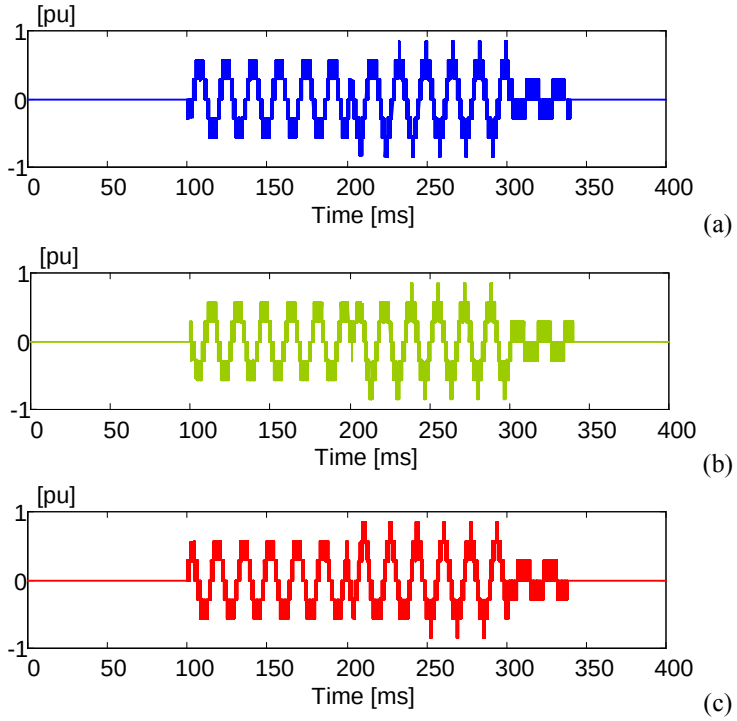

Figure 6.8 Series voltage of multi-level PWM-SSSC: (a) v_{ca}, (b) v_{cb}, and (c) v_{cc}

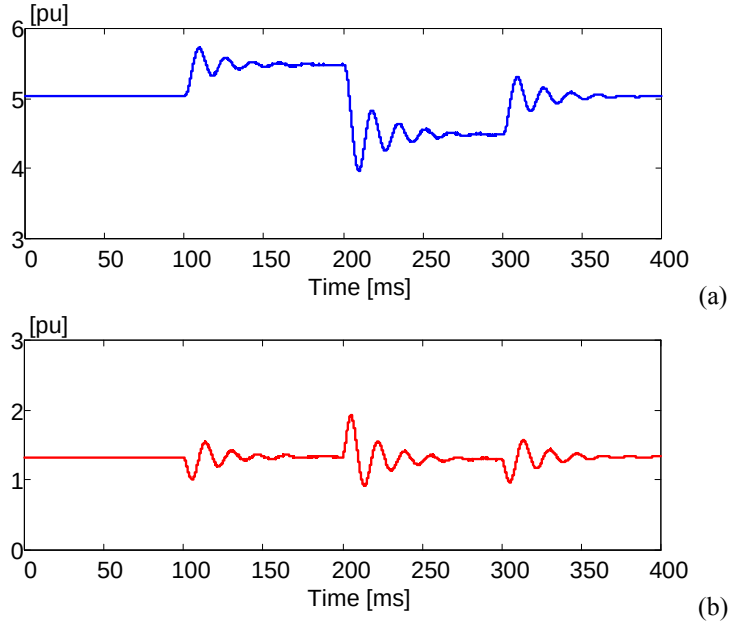

Figure 6.9 (a) Active power (*W*); (b) reactive power (var) flowing into the compensated AC line

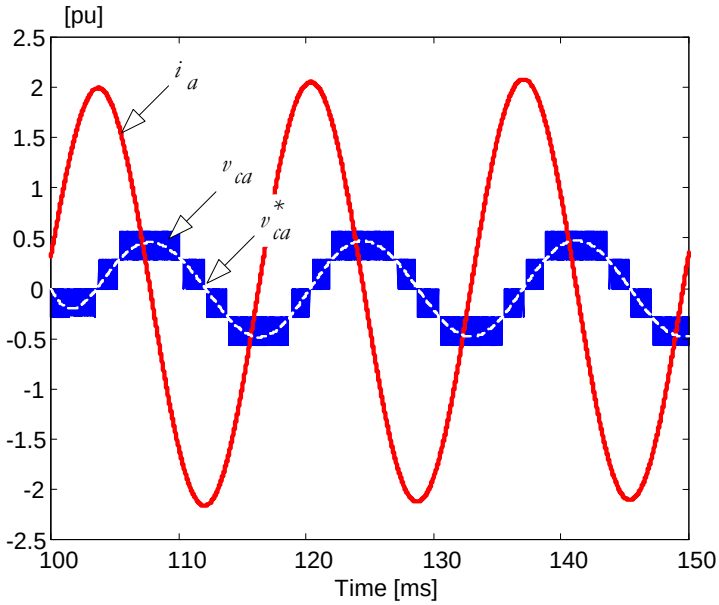

Figure 6.10 Details of the phase "a" of the line current, reference voltage, and multi-level PWM-SSSC voltage

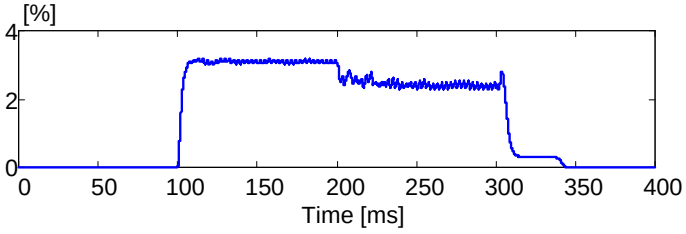

Figure 6.11 Total harmonic distortion due to the PWM-SSSC operation

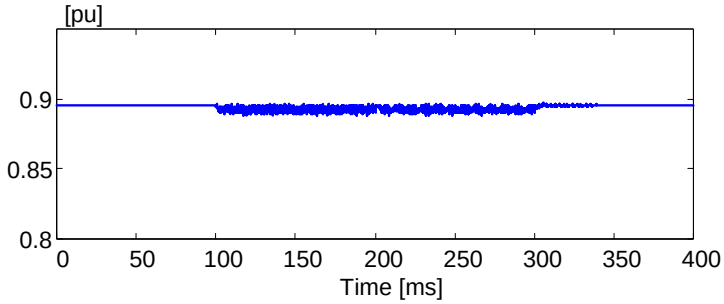

Figure 6.12 DC voltage of the PWM-SSSC

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CHAPTER 7. SUBSYNCHRONOUS RESONANCE

7.1 SUBSYNCHRONOUS RESONANCE (SSR) PHENOMENON

Any transient in the electric network, like a switching operation or a fault, will affect all generators connected to the system by causing a disturbance in the electrical torque in the machine. The generator is linked with several turbines stages through its shaft arrangement and the torque disturbance creates a vibration in the generator-turbine shaft system due to the resonances that exist in the mechanical system.

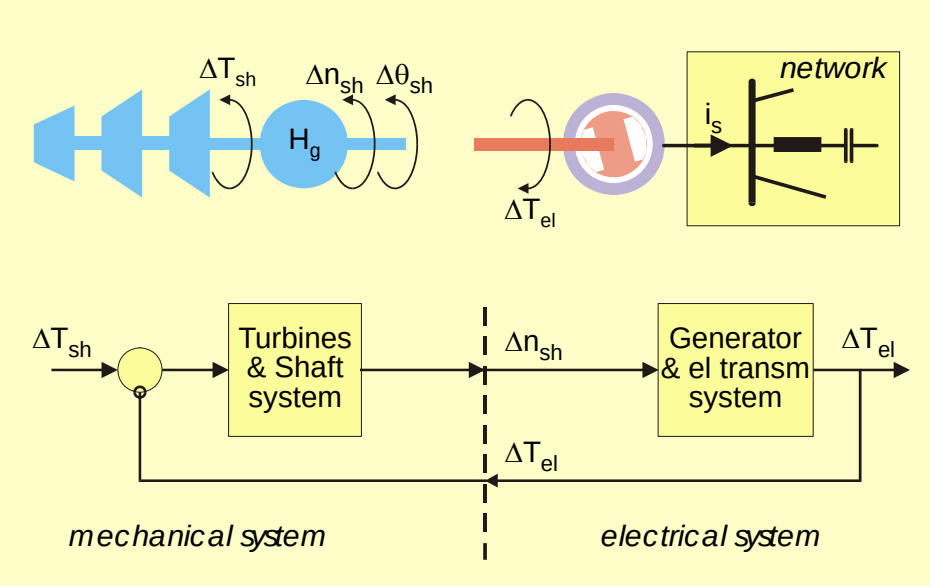

Figure 7.1 Interaction between electrical and mechanical systems

Figure 7.1 illustrates the interaction between the mechanical and electrical systems as described above. For those mechanical oscillation modes where the generator participates considerably, the vibration will modulate the speed of the generator shaft. The phase of the generator voltage then becomes modulated relative to the rest of the electrical network and accordingly the active power output, i.e., the electrical torque (ΔT_{el} in Figure 7.1), also will be modulated. As the electrical torque also impacts on the generator rotor speed a closed loop will be established as shown in the Figure 7.1.

The mechanical resonance frequencies in a turbo-generator shaft system typically occur in the subsynchronous frequency range between 10 Hz and 40/50 Hz at network frequencies of 50/60 Hz. The interaction in the closed-loop system illustrated in Figure 7.1 occurs mainly between mechanical frequency f_{mech} in the mechanical system and frequency f_{el} in the electrical system with the following relation

$$f_{mech} + f_{el} = f_N \tag{7.1}$$

where f_N is the network frequency (50 or 60 Hz). Thus, as an example, a mechanical frequency 12 Hz corresponds to the electrical frequency 38 Hz in a 50 Hz network.

7.2 DAMPING CONTRIBUTIONS

Both electrical and mechanical damping effects act on the vibrations in the shaft system. It is well known amongst the turbine manufacturers and sufficient margins are included in the design. These

margins are based on experience, measurements, and statistics, and it is assumed that a certain amount of damping is provided.

The mechanical damping is always positive but quite small. It depends strongly on the loading of the turbine. Normally it is difficult to calculate the damping at the design stage and often definitive values can only be obtained by measurements after commissioning. However, estimates of the minimum mechanical damping are known from experience.

The electrical damping depends on the characteristics of the network to which the generator is connected. For an uncompensated network the electrical damping in the subsynchronous frequency range is very small. Any system, passive or electronically controlled, connected to the network may impact on the electrical damping causing more or less damping of the mechanical resonance vibrations in the shaft system.

7.3 FIXED SERIES CAPACITORS (SC)

A passive fixed series capacitor (SC) is an extremly powerful and cost effective means to increase the transfer capability of electrical power through a power line. The inserted capacitive reactance compensates a portion of the natural inductive reactance of the line. The SC virtually shortens the length of the transmission line and thereby improves both angular and voltage stability. The transfer capability often is increased by 50-100 %. This becomes obvious from the well-known power transfer formula

$$P = \frac{U_1 U_2 \sin\delta}{X_L - X_C} \tag{7.2}$$

where U_1 and U_2 are the voltages in the line terminals, δ is the phase deviation between the line terminal voltages, X_L is the line inductive reactance, and X_C is the SC capacitive reactance.

Typically the degree of compensation, defined as X_C / X_L, is kept in the range 30-70%. In system configurations where large turbogenerators are connected directly into a series compensated line with a degree of compensation exceeding approximately 30%, the electrical damping needs to be examined in the frequency range where the resonance frequencies of the machine are located. Any possible interaction should be identified and assessed. Such a study is referred to as a SSR study and it is performed either before the project is executed or during the project execution stage.

In principle a SSR study aims for calculating the change in electrical torque, ΔT_{el} in Figure 7.1, which is caused by a small sinusoidal speed variation of the generator shaft, Δn_{sh} in Figure 7.1. The frequency of the speed variation is varied and for each such frequency one evaluates the ratio between the amplitude of the torque variation and the amplitude of the exciting shaft speed variation. The resulting quotient is the **electrical damping**, D_{el},

$$D_{el}(f_{mech}) = \frac{\Delta\hat{T}_{el}(f_{mech})}{\Delta\hat{n}_{sh}(f_{mech})} \tag{7.3}$$

often expressed in (per unit torque)/(per unit speed). A typical result from such a calculation for a generator connected to a strong power system through a radial transmission corridor which comprises lines with fixed series capacitors is depicted in Figure 7.2.

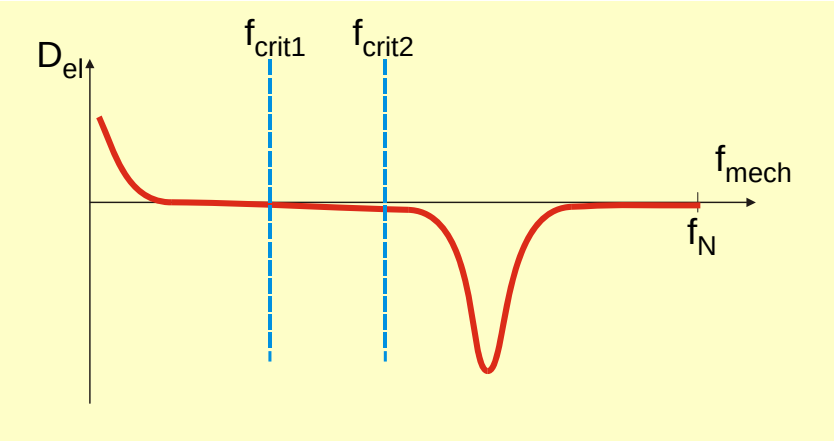

Figure 7.2 Typical electrical damping curve versus mechanical frequency

Two critical mechanical resonance frequencies for the turbine-generator shaft system also have been indicated in Figure 7.2. In order to avoid a SSR condition to occur, the negative peak of the electrical damping curve must not coincide with any of these critical frequencies. Preferably the negative peak of the electrical damping should be located to the right of all mechanical resonance frequencies in the shaft system, because then any further weakening of the power system will push the negative peak towards the right thereby moving it even farther away from the critical mechanical frequencies.

It is an interesting exercise to see what impact on the conditions described above that are caused by the insertion of any additional impedance in series with the compensated line. Figure 7.3 depicts the general effect of adding an additional series reactance or resistance.

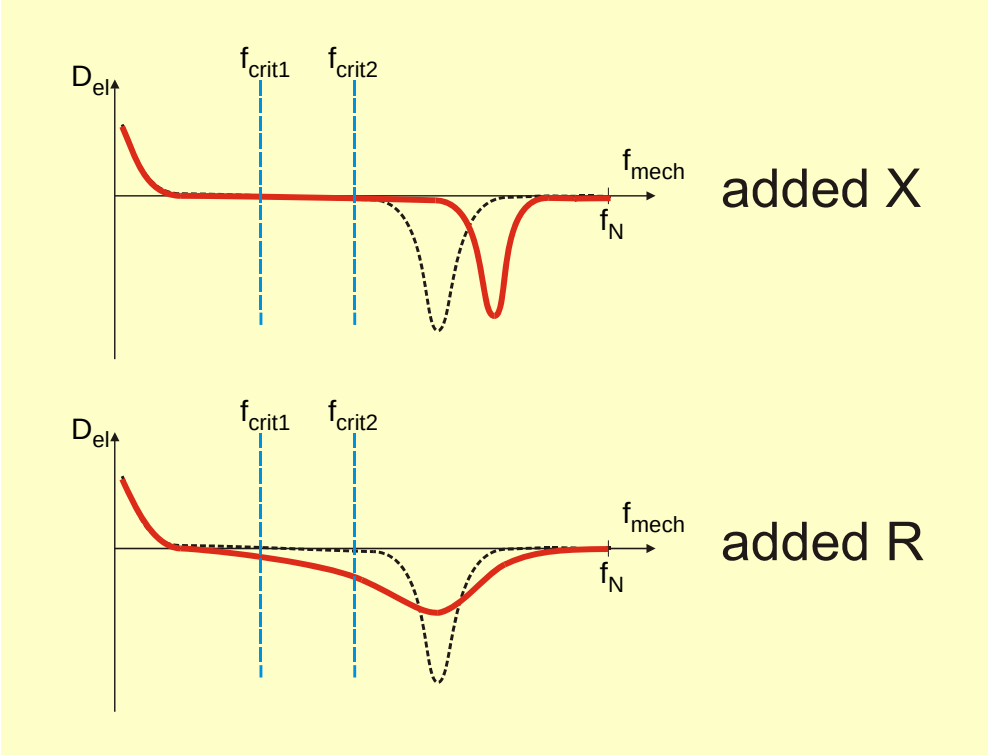

Figure 7.3 Effect of inserting additional impedance in series with the line

In the upper diagram in Figure 7.3, the effect of adding inductive reactance in series with the line is shown. The negative peak of the electrical damping then is moved towards the right towards a lower electrical frequency or equivalently towards a higher mechanical frequency. In general this will lessen the risk of SSR.

The lower diagram in Figure 7.3 shows the result of inserting additional resistance in the line. The magnitude of the negative peak in the electrical damping curve is decreased but at the same time its width is expanded. As shown this may worsen the risk of SSR for some critical mechanical frequencies.

7.4 THYRISTOR CONTROLLED SERIES CAPACITORS (TCSC)

The Thyristor Controlled Series Capacitor (TCSC) is a further development of the fixed series capacitor, which incorporates a thyristor controlled inductive path in parallel with the series capacitor bank. The main circuit and the generic waveforms are shown in Figure 7.4.

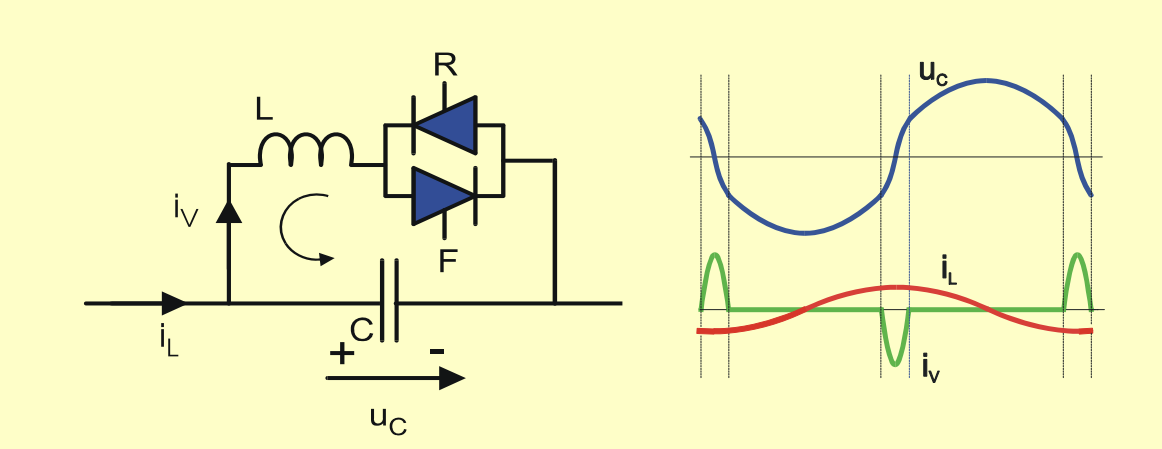

Figure 7.4 TCSC main circuit and generic waveforms

Each thyristor is fired when it is forward biased and at a certain angle before the capacitor voltage reaches zero. This causes a circulating current pulse through the series capacitor bank and the parallel inductor. The current through the capacitor thereby is increased and the fundamental frequency component of the capacitor voltage is "boosted" to a higher level than what would be obtained by the line current only. The controllable inserted voltage typically is used to provide damping to electromechanical power oscillations (0.1-2 Hz).

The topology of the TCSC radically changes the response of the series capacitor to small current components with frequencies in the subsynchronous range, i.e., in the range from 10 Hz to 40/50 Hz in a 50/60 Hz system system. When a subsynchronous current component with frequency f_{el}, $\Delta i_L(f_{el})$, is injected into the TCSC an additional voltage component with the same frequency, $\Delta u_C(f_{el})$, will appear across the TCSC. The quotient between these components constitutes the "virtual" or "apparent" impedance of the TCSC.

At high boost levels, where the apparent reactance of the TCSC at fundamental frequency is at least two times the physical reactance of the capacitor bank, the virtual impedance of the TCSC approaches an inductive reactance in the subsynchronous range. Accordingly the electrical damping curve changes as in the upper diagram ("added X") in Figure 7.3, when part of a certain fixed series capacitor is converted into a TCSC.

At low boost levels, where the capacitor voltage is increased by thyristor control only with a portion of the voltage caused by the line current, the apparent impedance of the TCSC depends strongly on the control system. It is possible to make a control system that preserves the inductive character of the

virtual impedance even at low boost levels. This means that series compensation can be provided at a higher degree of compensation than what would otherwise have been possible due to risk of SSR.

If only TCSC with adequately designed controls is utilized, no electrical resonance that could adversely affect turbo generators will be created and such a series compensator is "SSR free".

7.5 STATIC SYNCHRONOUS SERIES COMPENSATOR (SSSC)

The SSSC based on a power electronic Voltage-Sourced Converter (VSC) connected through a series power transformer already has been implemented in some test installations as part of a Unified Power Flow Controller (UPFC). The main circuit arrangement is depicted in Figure 7.5. The transformer provides the insulation between the converter and the high-voltage line and the converter can be composed of a number of three-phase units working on a common DC capacitor. The converters utilize fundamental frequency switching and several three-phase modules are combined through a magnetic interface in order to obtain a multi-pulse voltage waveform that satisfies the requirements on harmonic voltage generation. The converters may be of two-level or three-level type. The amplitude of the injected compensating voltage mainly is determined by the DC voltage, but, at least in the three-level converters, the amplitude can also be modified by controlling the converter voltage waveform. The leakage inductance of the series transformer and the magnetic interface will be added to the line inductance.

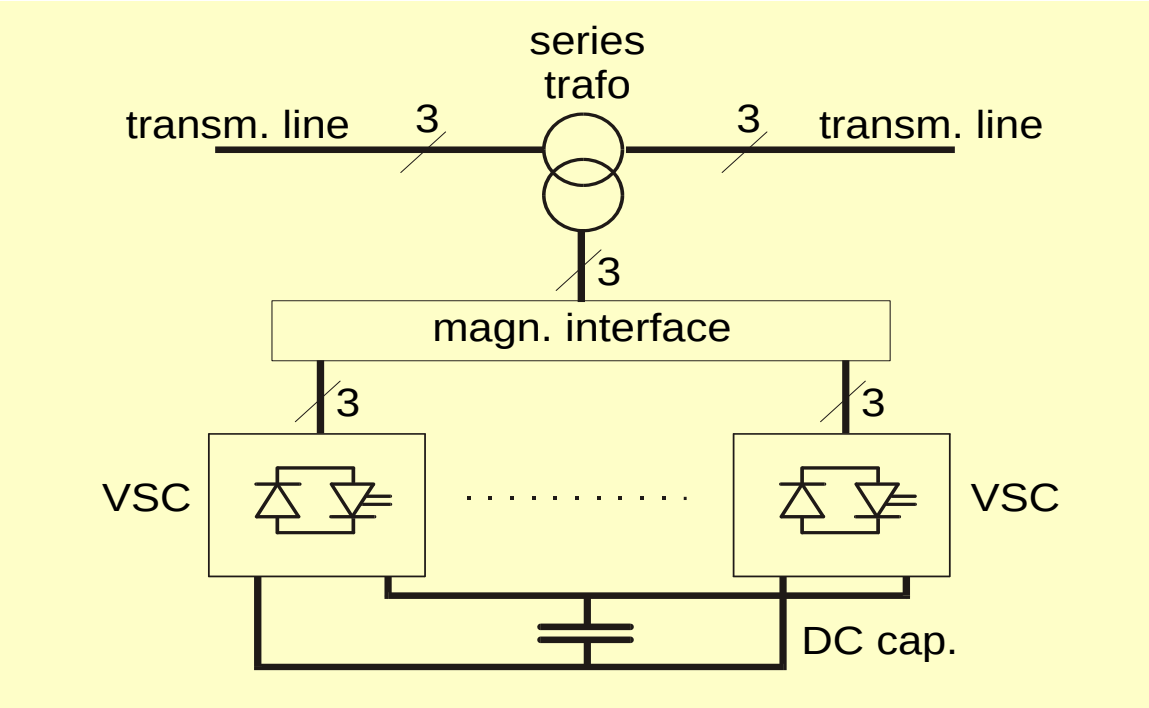

Figure 7.5 Outline of a multi-pulse SSSC using series transformer

The voltage that is inserted by the SSSC is strictly determined by the waveform command and the instantaneous DC voltage. Thus the inserted voltage at subsynchronous frequencies is independent of the line current, if the DC capacitor is sufficiently large and the bandwidth of the VSC control system is limited. Therefore, the SSSC ideally has zero virtual impedance in the subsynchronous frequency range and the SSSC can, in principle, be used to provide series compensation without causing SSR. The situation when a high degree of fixed series compensation is replaced by a lower degree of fixed series compensation plus an SSSC generating the remaining compensation voltage would appear as in the upper diagram ("added X") in Figure 7.3.

However, in reality the size of the DC link capacitor will be limited and the control system is not totally insensitive to subsynchronous components in the line current. The characteristic virtual impedance of the SSSC due to these effects must be studied in detail in order to determine the behaviour of the SSSC with respect to SSR in any specific case. It seems reasonable to believe that it is possible to design a control system, where the generation of resonance conditions in the subsynchronous frequency range can be avoided. Some results have been published already and it is expected that further results from calculations and simulator testing will be presented in the future at technical conferences.

In another type of SSSC a power electronic converter using high frequency switching is used. Figure 7.6 outlines such a converter. The switching is controlled by Pulse Width Modulation (PWM). An AC filter is inserted in series with the VSC terminals in order to suppress the high-frequency frequency harmonics caused by the switching.

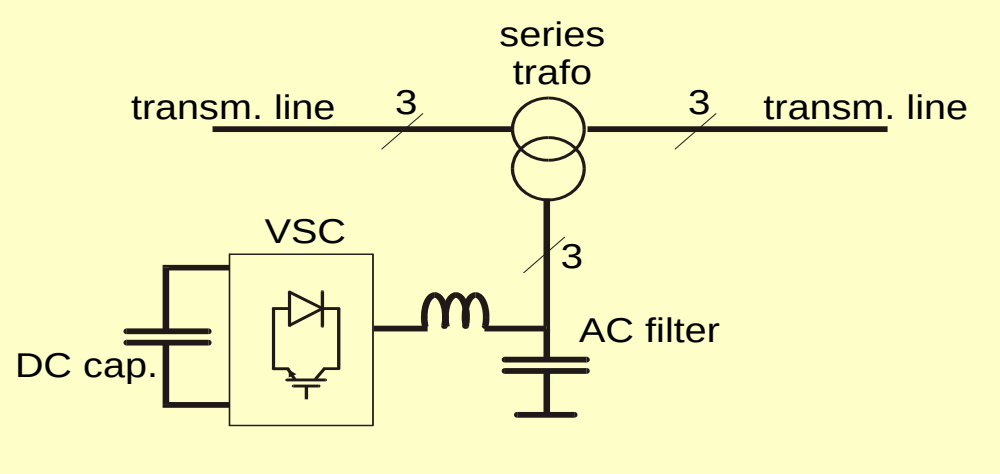

Figure 7.6 Outline of a SSSC using PWM modulation and series transformer

The bandwidth of the controlled inserted voltage can be quite high if the switching frequency is kept sufficiently high and this makes it probable that the control system can be designed to mitigate resonances in the subsynchronous frequency range. Analysis of the behaviour with respect to SSR can only be made if details about the control system and the filter arrangement are available.

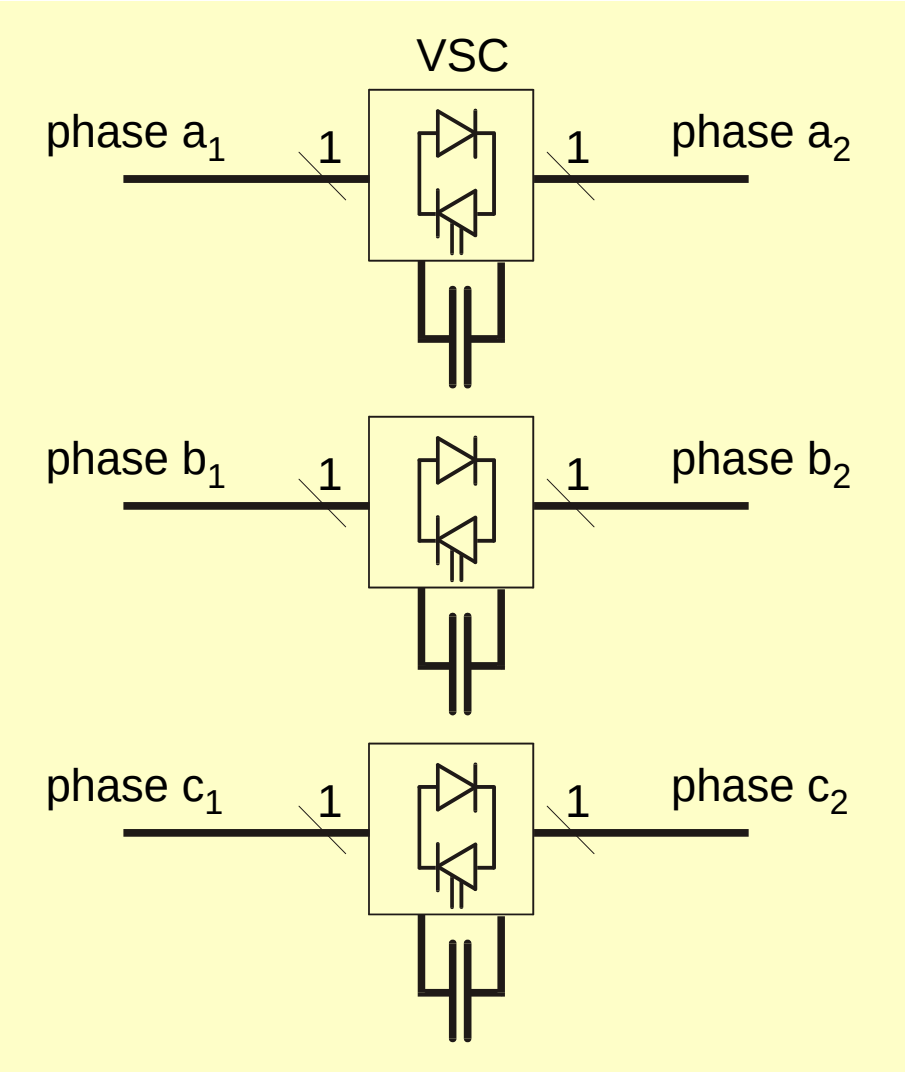

Figure 7.7 Outline of SSSC using VSC modules in each phase

Alternatively a concept using power electronic converters connected directly in series with the transmission line according to Figure 7.7 can be envisaged. In principle one single-phase converter is inserted in each line phase. It is assumed that only fundamental frequency switching can be utilized in this case due to the need for harmonic voltage suppression. Each converter should be located on a separate platform, which should provide the insulation with respect to ground and the mutual insulation between the different phases. Therefore each converter needs its on DC link capacitor. The same considerations with respect to its SSR behavior as in the multi-pulse SSSC apply.

It is interesting to discuss this type of SSSC from the cost and from the footprint point of view. However, a converter of this kind needs to be extremely robust since it must conduct the full short-circuit current through the semiconductors. This restricts the types of components for this application. In the author's opinion the available semiconductor devices of today are not suitable for this application. Some materials developed in long-term research and development, like silicon carbide (SiC), seem to be interesting candidates for such converters located "in the power line". Unless a breakthrough is achieved in the research and unless a strong market pull for such SSSC installations is noticed, this development will take a considerable time.

Finally it should be mentioned that some studies have been performed on a concept that utilizes the PWM modulated SSSC as a means to mitigate SSR caused by, for example, fixed series

compensation. In this case the SSSC, inserted close to the generator that shall be protected, is used exclusively to produce voltage at the subsynchronous electrical frequencies that are relevant for the protected generator. The rating of the SSSC becomes very small (< 5% of the generator rating) because it does not produce any voltage at the network fundamental frequency.

7.6 ASSESSING SSR CONDITIONS USING THE FREQUENCY SCANNING METHOD

In order to assess the risk of SSR for a certain power system one must know the contingencies under which the power system is supposed to operate, which generators that are at risk, the resonance frequencies of the generator-turbine shaft system and the electrical damping curve for these generators. A first evaluation can be made using "frequency scanning". This concept means that an approximative electrical damping curve is being calculated for each generator in every contingency case. The result is then compared with the resonance frequencies for the critical generators. Typically the most severe conditions occur in contingency cases that leave one generator or a group of generators radially connected via a series compensated line to the power system.

The approximative electrical damping traditionally is calculated by evaluating the impedance seen from the generator rotor in the frequency range from 0 to $2\times f_N$, where f_N is the network frequency. The network should be configured in the contingency case under study. Other generators in the system can be represented by their subtransient reactances. Under the assumption that the rotor flux is constant the following formula for the electrical damping coefficient ($D_{el} = \frac{\Delta \hat{T}_{el}[pu]}{\Delta \hat{n}_{sh}[pu]}$) can be derived as

$$D_{el}\left(f_{mech,k}\right) = \frac{1}{2}\left\{\left(\frac{f_N}{f_{mech,k}} + 1\right)\mathrm{Re}\left(\frac{1}{Z\left(f_N + f_{mech,k}\right)}\right) - \left(\frac{f_N}{f_{mech,k}} - 1\right)\mathrm{Re}\left(\frac{1}{Z\left(f_N - f_{mech,k}\right)}\right)\right\} \tag{7.4}$$

where

$f_{mech,k}$ is the frequency of mechanical resonance at mode k
f_N is the network frequency
$Z(f)$ is the impedance seen from the generator at electrical frequency f

The formula shows that the conductance at supersynchronous frequencies provides a positive contribution to damping while the conductance at subsynchronous frequencies provides a negative contribution. The corresponding change of the exponential damping coefficient (constant σ_k in the exponential expression for the oscillation amplitude $e^{-\sigma_k t}$ for mode k) is given by

$$\Delta\sigma_k\left(f_{mech,k}\right) = \frac{D_{el}\left(f_{mech,k}\right)}{4H_k} \tag{7.5}$$

where H_k is the modal inertia constant for mechanical resonance at mode k.

The critical frequencies for the generator-turbine shaft system are then compared with the calculated electrical damping in order to evaluate the risk of SSR. If the electrical damping in the vicinity (some Hz) of the critical frequencies is negative with a magnitude that exceeds the mechanical damping in the shaft system SSR is a problem. An example of a result obtained in such investigation is shown in Figure 7.8. In the example the system is operated in an entirely radial configuration, which causes

substantial electrical undamping in a large part of the subsynchronous frequency range. Figure 7.8 shows that the electrical damping at the critical frequency 2 is negative with high magnitude and that some modification must be made in order to make the system operable.

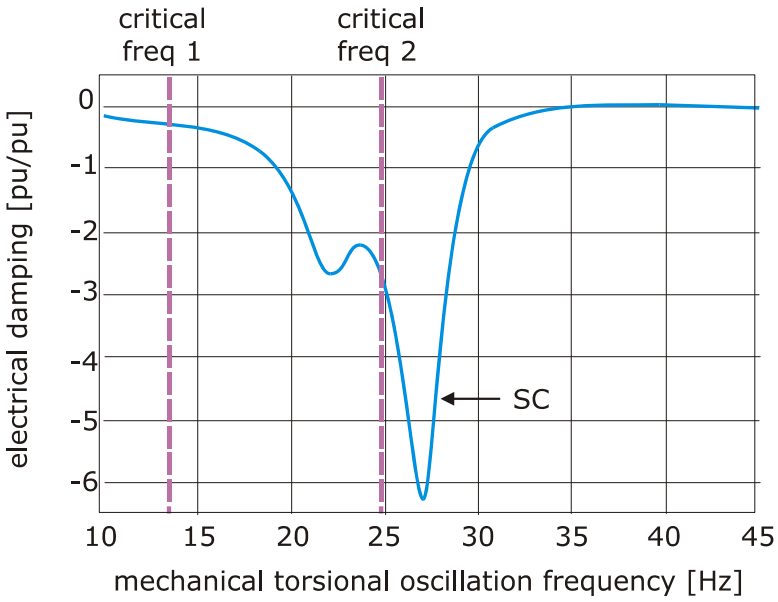

Figure 7.8 Example of Frequency Scanning Result

A problem arises in the method described above when power electronic devices are involved in the SSR study. They might be suspected to cause SSR problems or they are supposed to mitigate SSR conditions produced by other equipment. The problem is that it may be difficult or impossible to describe the response to an injected subsynchronous current component as a simple frequency-dependent impedance. In this case a time-domain digital simulation program may be used to extract the electrical damping curve.

To this end the generators and the electrical system with the contingencies that are applicable to the studied case are modelled in the simuation program. At least the network surrounding the critical generator and the series-compensated transmission lines should be carefully represented. A forced sinusoidal speed variation with a subsynchronous frequency is applied on the generator shaft in the model. The program calculates the responding electrical torque, which also is sinusoidal and has the same frequency as the exciting speed modulation signal. The electrical torque signal is resolved into its components in phase with and in quadrature with the speed variation. The quotient between the amplitude of the oscillation component in phase with the speed variation and the amplitude of the speed variation itself is the desired electrical damping. The frequency of the shaft speed modulation signal can be slowly swept through the interesting subsynchronous frequency range with, for example, frequency slope 0.25 Hz/s. The electrical damping curve can then be extracted from the result of the time-domain simulation. Figure 7.9 depicts the principle for this method to extract the electrical damping curve.

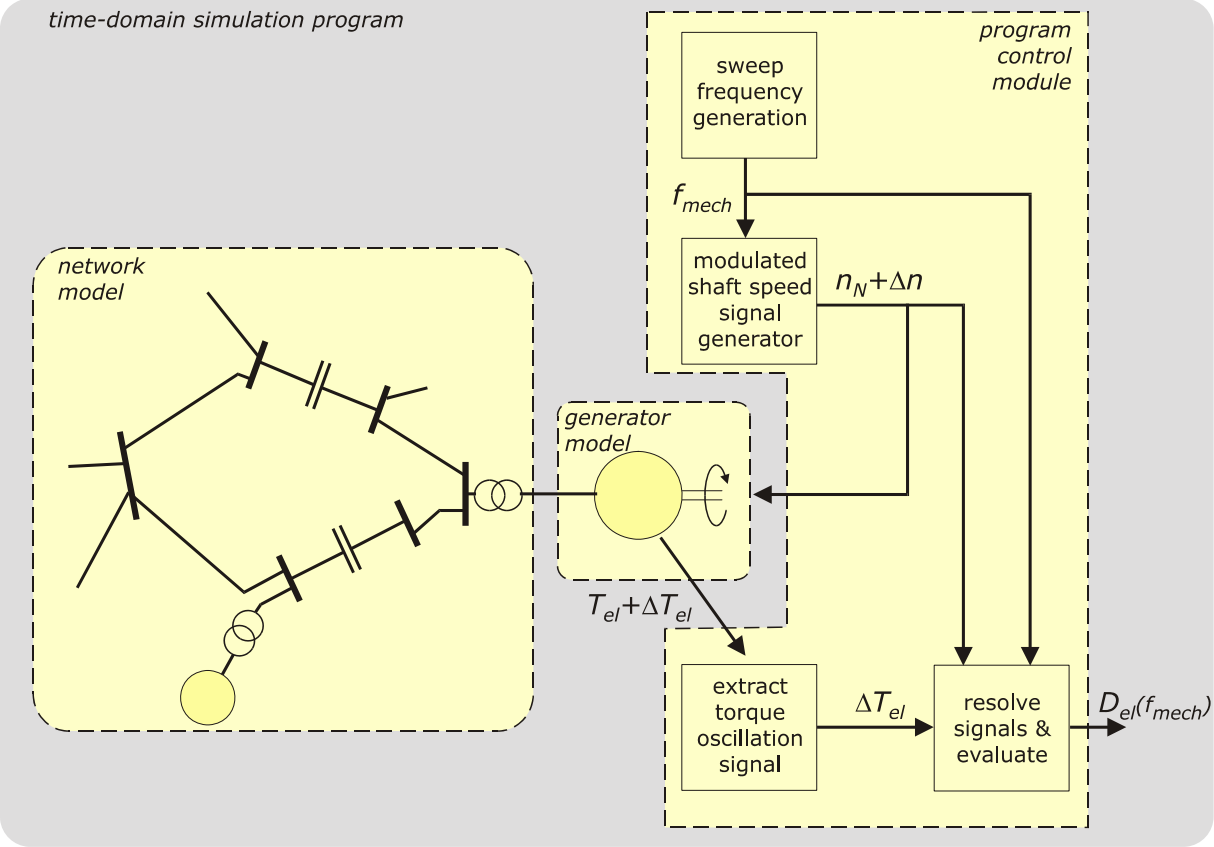

Figure 7.9 Program structure using time-domains simulation to extract electrical damping

An example of an electrical damping curve where this method has been applied is depicted in Figure 7.10. In this study the same system as in Figure 7.8 has been studied. TCSC has been included for the purpose of SSR mitigation and active damping.

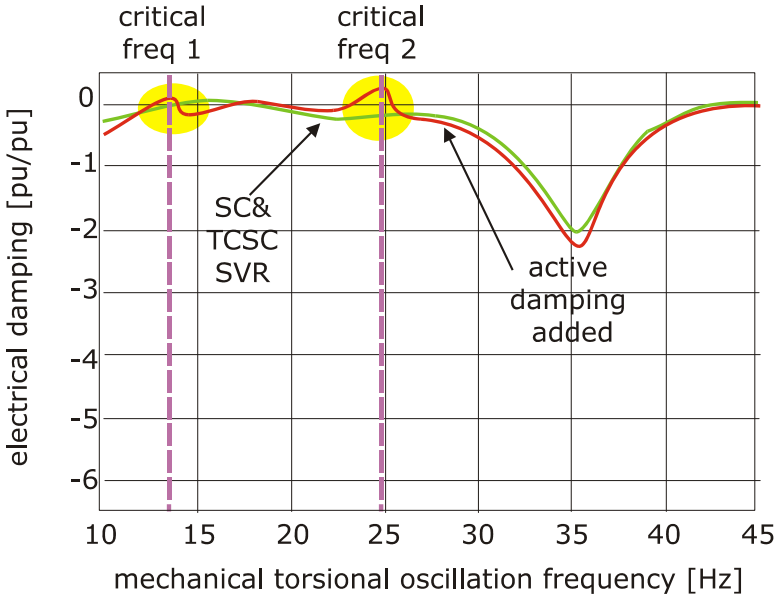

Figure 7.10 Electrical damping extracted from a time domain simulation program

An important advantage of the method based on time-domain simulation is that it may easily be adapted to study the torques in the shaft system at transient events, for example, caused by short-circuits in the transmission system. In this case the program control module in Figure 7.9 should be replaced by a simulation model of the generator-turbine shaft system as shown in Figure 7.11.

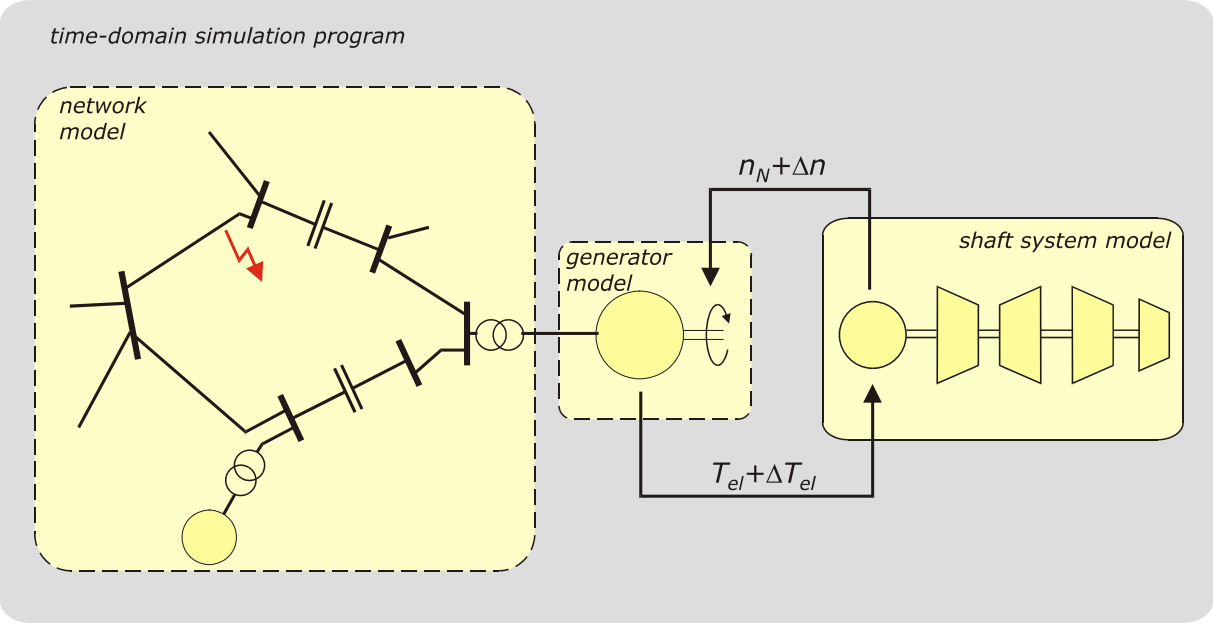

Figure 7.10 Transient torque study program structure

If the generator shaft system has critical resonance frequencies close to frequencies where the electrical damping is negative such studies should be performed for possible short-circuit scenarios. The reason is that very high stresses may occur in the shafts in the interconnecteing shafts between the generator and turbine stages due to "torque amplification". This phenomenon may cause an untolerable loss of life expectancy of the shafts if it is not being alleviated.

References

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[7.4] F. R. A. Jowder and B.-T. Ooi, "Series Compensation of Radial Power Systems by a Combination of SSSC and Dielectric Capacitors," *IEEE Trans. Power Delivery,* vol. 20, no. 1, pp. 458-465, Jan. 2005

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PART III
SSSC INSTALLATIONS

CHAPTER 8. EXISTING INSTALLATIONS

The first section of this chapter gives a brief overview about the components which are used in a SSSC. It is followed by a description of existing high power electronic plants where an SSSC part is included. Finally commissioning tests and field test results for the described installations are reported.

8.1 COMPONENTS OF AN SSSC

Figure 8.1 gives an overview of the SSSC main components, which are hightlighted in boxes. These components will be explained below in alphabetical order.

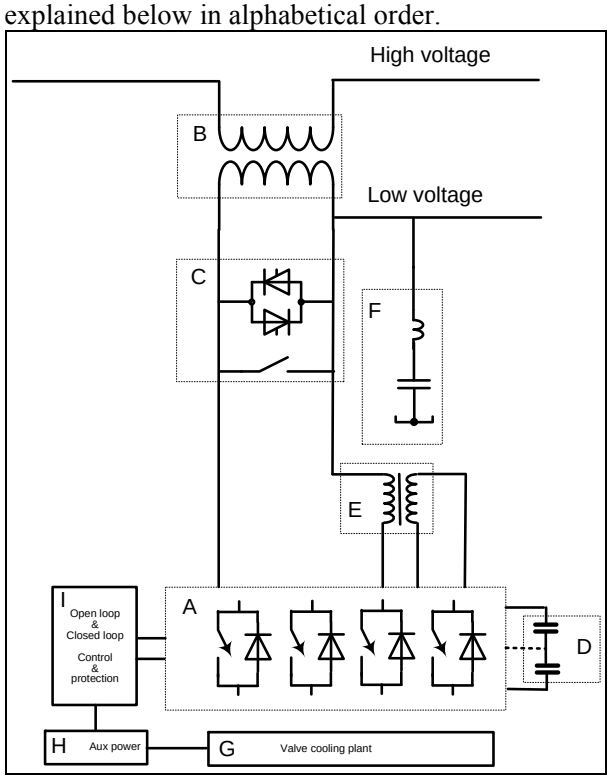


Figure 8.1 Overview of an SSSC single-line diagram

A Converters

The converters of the existing stations are made up by GTO devices and are based on 3 level arrangements. Generally converters can be made up by thyristors (forced commutated configurations), GTOs, IGCTs and IGBTs. The principal arrangement can vary from 2-level configurations using PWM modulation up to multilevel configurations using fundamental switching technology. Details are described in the VSC Topologies chapter.

B Series Transformer

SSSC is connected in series with the line. To couple the voltages which are generated in the converter circuits at lower voltage levels towards the system a transformer is connected in series with the line at high voltage side.

C Electronic By-Pass Switch

In case of system short circuits where the system short-circuit current can also flow through the SSSC system-side transformer winding, the respective current will also arise on the low-voltage side transformed by the transformer ratio. This current will also flow through the converter power electronic

devices. Therefore electronic by-pass switches which can react immediately are typically installed in parallel to the converter terminals. They are designed to take over the short circuit for a short time and are released from these stresses by the operation of a primary conventional by-pass breaker.

D DC Capacitor

At the "DC" terminals of the converters the DC capacitor is connected. This DC capacitor is the energy storage component of the VSC. The size of the DC capacitors is determined from the allowable DC ripple contents and how fast voltage changes are required on the DC side. The DC capacitors can be connected directly at the common DC terminals or to various levels of the converter (refer to the VSC Topologies chapter).

E Harmonic intermediate transformer/Series Reactor

Harmonic intermediate transformers are used in existing SSSC installations based on GTO semiconductors. The topology is built up such that the suppression of harmonics is achieved by specific interconnections of separate converters by magnetic circuits. The converters are controlled by fundamental switching technology to combine several converters such that the harmonics in the output voltage are magnetically suppressed.

If several VSCs are operating in parallel they have to be decoupled by reactors. Each of the parallel VSC is equipped with its own series reactor. The series reactor is designed to limit the di/dt stresses of the converter components. Paralleling is used in newer installations based on IGBT devices.

F Harmonic Elimination Requirements

Future installations based on IGBT technology have several converters operating in parallel using PWM control resulting in suppression of major harmonics. Typically they will use common filtering of higher frequency harmonics at the bus where they are connected in parallel (refer to the chapter on Basic VSC Structure and Harmonic Generation).

G Valve cooling plant

A cooling system for the semiconductor devices is necessary to limit the thermal stresses of the individual devices. The size of the cooling system depends on the continuous and transient operation of the SSSC and must also consider internal and system fault conditions. Typically ionized water cooling technology can be used, configured as a single-circuit or double-circuit cooling system depending on the environmental conditions. The cooling system purification is located inside the building with the pump skids. Water to air heat exchangers are located outside. The cooling system is the major load for the auxiliary power supply.

H Auxiliary Power

The major auxiliary load for the operation of a SSSC is the cooling system. DC power is provided also to the converter poles for GTO/IGBT gating power and local pole control power. Station service power is typically backed up by battery equipment (lead acid batteries and charging equipment).

I Control and Protection Equipment

The control includes the open-loop (sequence control) and closed-loop control (CLC). The sequence control acts on start-up and shutdown, and communicates with all major components collecting status information of the equipment. The CLC controls the SSSC according to its requirements from the system. Depending on the converter configuration a different kind of control is used (refer to the chapter on Basic VSC Switching Strategies). Each converter pole is typically made up by submodules which include associated gate drive controls for each semiconductor level. Each pole has additional electronics which are associated with the particular switching of the pole. The control signals from the CLC are sent to the converter pole controls where the device firing and blocking are coordinated with the other series connected devices. Communication is provided by fibre-optic cables. The control is connected by serial

communication to all relevant parts of the SSSC including the cooling system. The control monitors continuously the operation of all subsystems, collecting and analyzing the relevant status information.

Because of the importance of the SSSC controllability the features of the SSSC control is described in more detail below.

8.1.1 Control

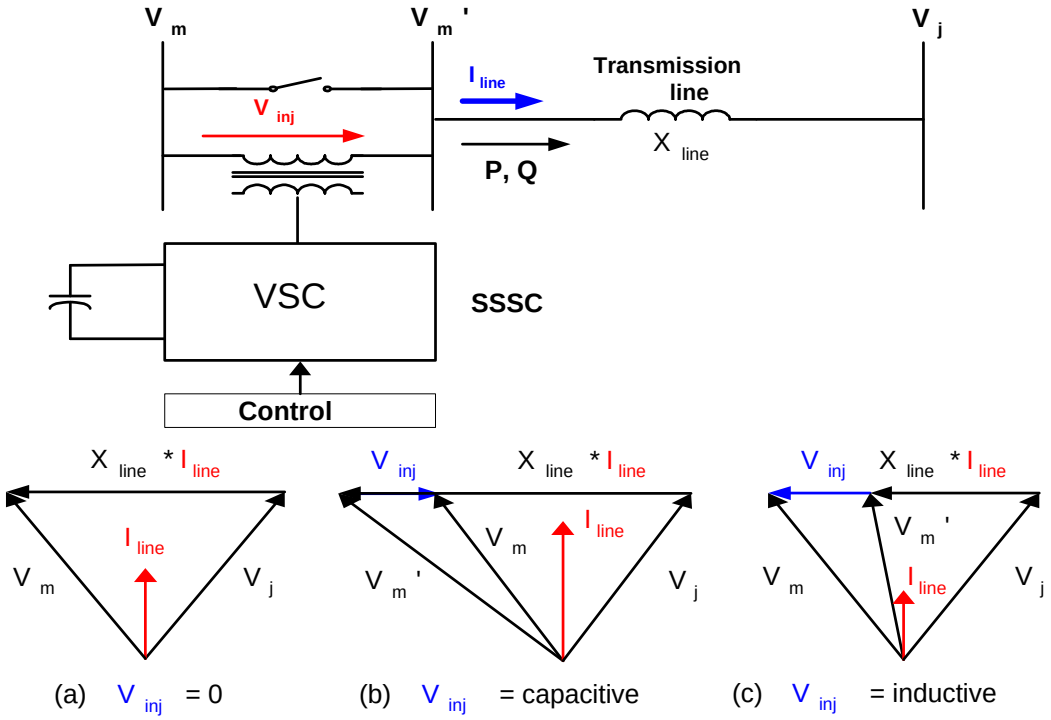


Figure 8.2 SSSC inserted voltage with respect to the line current (a) neutral, (b) capacitive, (c) inductive

The SSSC controller injects the voltage V_{inj} in quadrature (i.e., at ±90 degrees) with respect to the transmission line current as illustrated in Figure 8.2. Therefore, the SSSC exchanges only reactive power with the transmission line. The SSSC has the effect of changing the equivalent line impedance and therefore, only the magnitude of the line current. As shown in Figure 8.2 (a), with $V_{inj} = 0$, the magnitude of the line current is unchanged; with capacitive V_{inj} the line current magnitude is increased (as shown in Figure 8.2 (b)); and with inductive V_{inj} the line current magnitude is decreased (as shown in Figure 8.2 (c)). The control of the magnitude of the line current enables control of real power flow P (MW) in the transmission line. The real power flow can be increased or decreased from the nominal (uncompensated) line power flow. In fact, the real power flow in the line can be reversed based on the change in the line current magnitude (or the rating of the SSSC) and the nominal (uncompensated) line power flow value.

As mentioned in previous chapters, the SSSC is implemented with a Voltage-Source Converter (VSC) connected in series with the transmission line. The basic operation of the Voltage-Source Converter (VSC) is essentially to convert the dc voltage at their dc terminals into an ac voltage output, in accordance with a vector reference that determines:

- the ratio between the DC-side and AC-side fundamental voltage, and
- the phase angle of the AC output voltage.

The basic controller structure for the SSSC is shown in Figure 8.3. For SSSC control, as for STATCOM, the VSC or the inverter can be operated with a constant ratio between the DC voltage and the AC output voltage, as one control option. In this control method, the phase angle of the inverter output voltage is thus the only control input. Changes in the magnitude of the output (series injected) voltage are made by linearly charging and discharging the DC bus capacitors or changing V_{dc} voltage. The inverter voltage V_{inj} is kept substantially in quadrature with the line current Iline. This can be done with leading or lagging polarity so that the injected voltage V_{inj} appears in the line as inductive or capacitive respectively. Charging of the DC bus capacitors (or V_{dc} voltage) is controlled by allowing the injected voltage to deviate slightly from a quadrature relationship with the line current, thereby exchanging real power between the inverter (i.e., the DC capacitors) and the line. Clearly this mechanism will only work when there is a sufficient level of line current to allow power exchange – typically 0.05-0.1 pu line current. The control scheme thus has a singular region around zero line current which must be avoided. In addition, the DC voltage control loop gain varies with the DC voltage and line current. Adaptively changing the loop gains can compensate for this problem as shown in Figure 8.3.

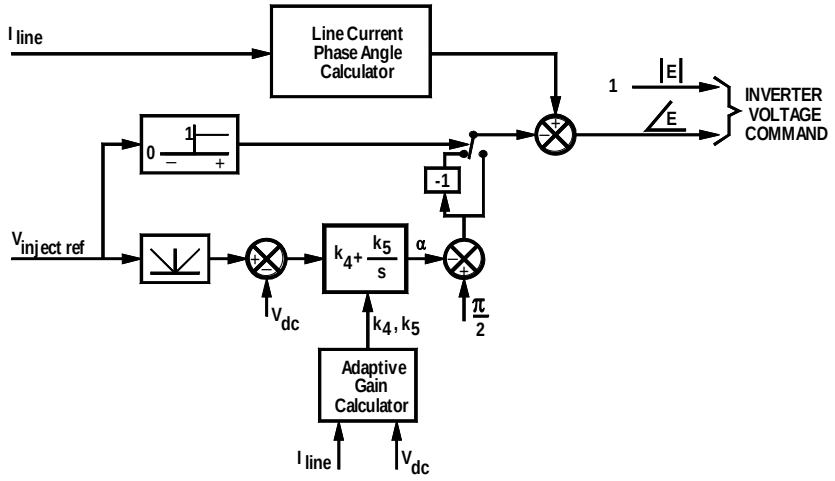


Figure 8.3 SSSC controller structure

As a second control option, the VSC can also be vector-controlled where the magnitude and phase angle of the inverter output voltage are both independently controlled. In this case, the DC bus voltage V_{dc} is regulated to a constant value, as compared to the SSSC controller in Figure 8.3, where the DC bus voltage is linearly proportional to the magnitude of the output voltage.

The SSSC injected voltage (V_{inj}) control method shown in Figure 8.3 is an open-loop control – that is, the operator "dials" in an injected voltage reference (as a percentage of the system bus voltage) and depending on the line impedance, the magnitude of the line current changes. As it will shown by commissioning results, because the injected voltage range is small (typically 5% to maximum of 10% of the line/bus voltage), the line current magnitude change is linear. This is an important result because the operator can apriori predict the voltage injection required for a given line current magnitude change. This even allows the calibration of the real power changes to required voltage injection V_{inj} for a given transmission line in p.u. This "linear" control aspect of SSSC is attractive to the operator for real power dispatch, even with open-loop voltage injection V_{inj}.

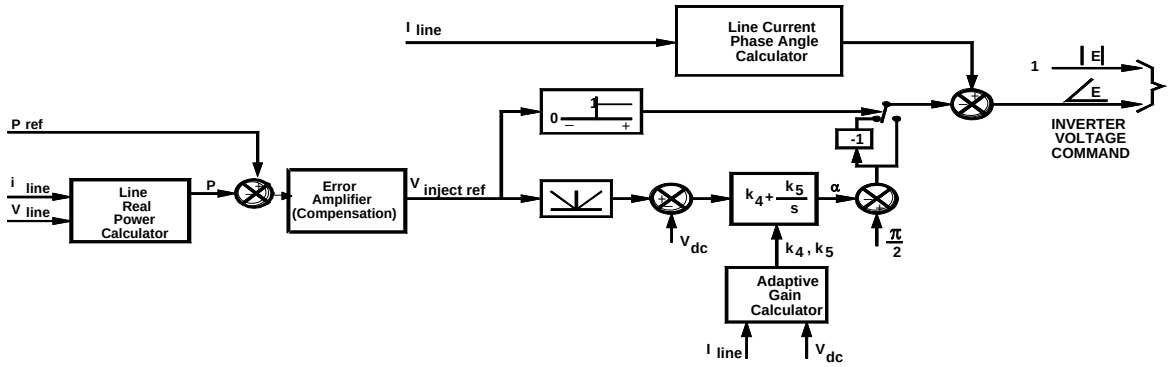


Figure 8.4 SSSC control structure for vector control and closed loop power flow

Figure 8.4 shows the SSSC control structure for vector control and closed-loop power flow controller – in this case, the line real power P_{line} (MW) can be regulated to a desired P_{ref}. The real power on the line is calculated based on the line/bus voltage and current at the point of SSSC voltage injection bus. The power error is used to generate an injected voltage reference V_{inject_ref}, which is required to increase or decrease the line current magnitude. Note that in this case, the line real power flow can be increased or decreased from the nominal or uncompensated line power flow value, and can even be reversed.

For the SSSC, the reactive voltage injection is chosen to influence the power flow on the line. Capacitive injection tends to increase the magnitude of the line current and inductive insertion tends to decrease it. With the SSSC, real and reactive power on the line cannot be independently influenced. In principle, the choice of the reactive voltage reference for a particular change in line power can be made automatically by a control loop. This automatic power flow control mode is as shown in Figure 8.4.

It is important to note that the reactive power flow Q_{line} (MVAR) on the transmission line with the SSSC operation is uncontrolled – i.e., the reactive power flow on the line can increase or decrease depending on the line impedance and voltage injection. This will be validated by field test results in Section 8.2.2.2.

8.1.2 Protection

The protection includes conventional protection devices for the conventional equipment and fast action protection functions in the control for the electronic devices of the VSC. The protection must ensure that all components are operated within their design limits. Conventional over-current and over-voltage protection is used for the conventional equipment. Special control-embedded over-current and over-voltage protections limit the voltage and current stresses of the semiconductors.

The protective action for the SSSC is to bypass the series insertion transformer as shown in Figure 8.5. This can be done mechanically by means of the bypass breaker, and/or electronically by means of the secondary side fast-acting thyristor bypass switches (TBS). Protective bypass can be initiated at any time and will also be initiated by the SSSC under irrecoverable internal failures and line fault conditions. Because the SSSC inverter carries the line current but does not dictate its value, the principal reason for bypass is inverter overcurrent protection. The method by which the SSSC comes out of bypass after an overcurrent needs to be defined. Also the possibility of initiating only an electronic bypass and not closing the mechanical bypass breaker can also be investigated. Several options exist – including re-insertion of the SSSC after the system line fault condition. Consider the case of a 6-cycle line fault. Due to the line fault, the overcurrent limit of the VSC is reached and the VSC is bypassed by the fast acting thyristor bypass circuit. The low-voltage breaker (LVB) and the high-side breaker (HSB) are both not closed and after the fault, the SSSC is re-inserted into the line with the same voltage injection as the pre-fault condition. If the system line fault recurs within a certain pre-determined period or

persists, both the TBS and the LVB can be closed to isolate the SSSC from the line, forcing a re-start of the SSSC after the fault condition.

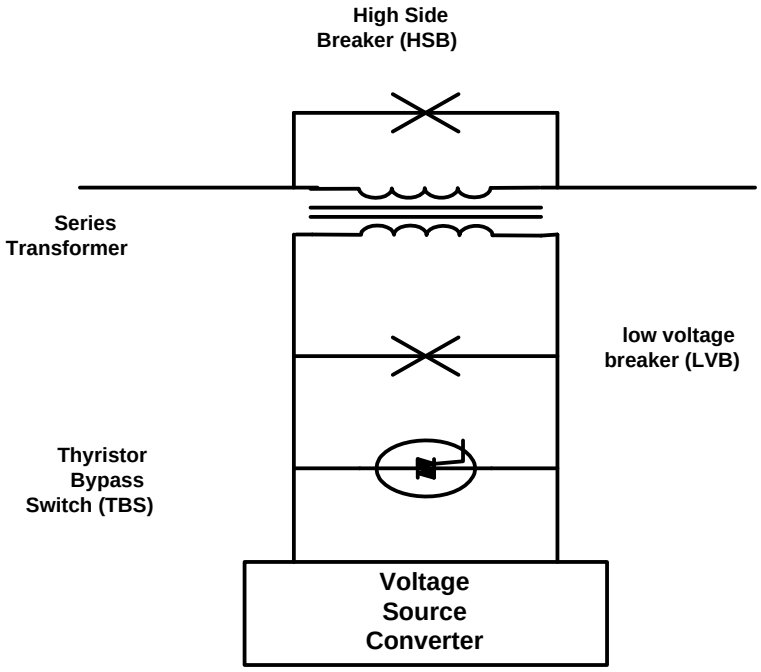


Figure 8.5 Thyristor Bypass System (TBS) for protection of series connected VSC based SSSC

8.2 DESCRIPTION OF EXISTING INSTALLATIONS

There are three SSSC installed on transmission grids, SSSC portions included in the Convertible Static Compensator (CSC) installed on NYPA transmission system, SSSC included in the UPFCs installed at at Inez, substation of AEP transmission system and the UPFC installed on the Korean transmission system at Kanglin. The following sections describe the background of these installations, summarize the technical data, and give an overview about the commissioning of the plants.

8.2.1 UPFC Inez, AEP, USA

8.2.1.1 Overview

Purpose

This installation developed from a collaboration between AEP, EPRI, and Westinghouse Electric Corporation in 1996. The Inez area was selected due to requirements for an increase in power transfer capability and for voltage support. The UPFC installation was part of a reinforcement project which also included building of a high capacity line, a system transformer, and additional series reactors to limit loads on existing lines.

Modes of operation

The UPFC Inez can be used as 2 x STATCOM, 1 UPFC, or 1 SSSC.

Single line - layout

The single line of the UPFC Ines is shown in Figure 8.6 below. Figure 8.7 shows the arrangement of the UPFC components in the Inez station.

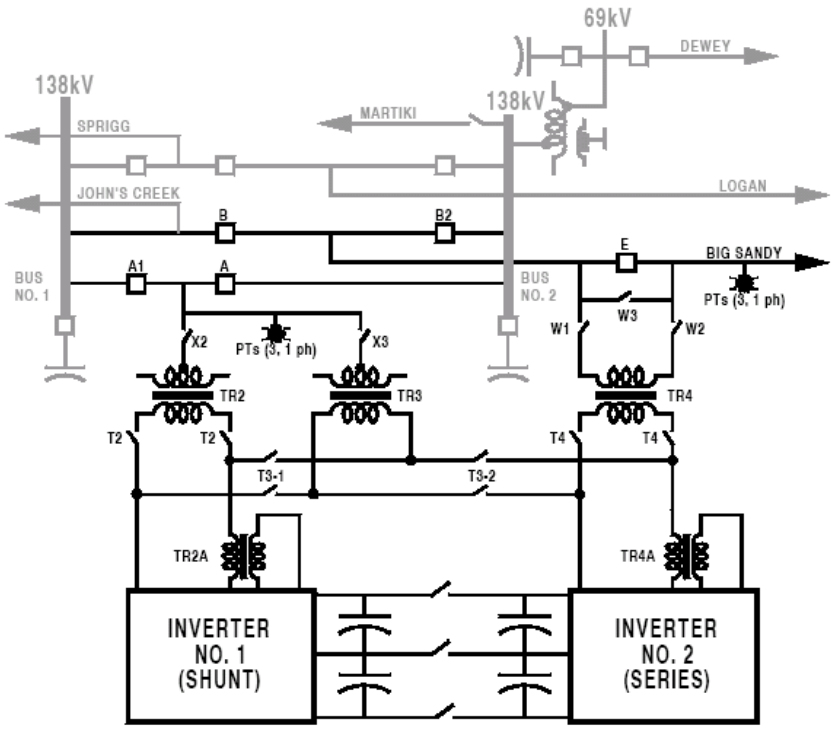


Figure 8.6 Single line of the UPFC Inez and connection to the 138 kV system

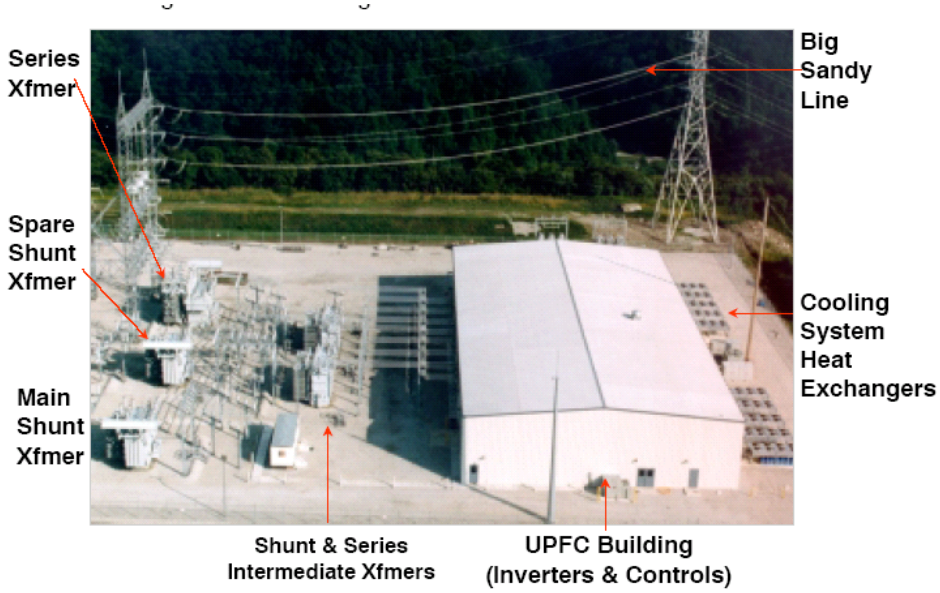


Figure 8.7 Aerial view of the UPFC installation

Basic data

HV system voltage	138 kV
LV system voltage	8.317 kV
DC bus voltage	± 10.46 kV
Converter rating	2 x ± 160 MVA
Type of semiconductor	GTO 4.5 kV / 4 kA
Type of converter	3 level
Number of converter sections	4
Pulse number	48
Number of series connected GTOs	6/7
Cooling	50/50% EG/Water
Ambient temperature	-37 / 40 ˚C

Commissioning schedule

The project was started in 1996. The commissioning started in1997. The dedication ceremony for the full UPFC installation was on June 26, 1998.

The commissioning was carried out in various steps to cover the five main operating conditions:

UPFC changing real power (P)
UPFC changing reactive power (Q)
UPFC changing local bus voltage
UPFC keeping unity power factor
Series converter operating in SSSC mode

8.2.1.2 Commissioning and test results

Inverter #2 Test Plan for Operation in Series with Big Sandy Transmission Line

I. Background

The Inez UPFC installation comprises two ±160 MVA voltage-sourced GTO-based inverters arranged in a versatile power circuit configuration. The two inverters can be connected through the DC bus or operated separately with no DC bus interconnection. Inverter #1 is dedicated as a shunt-connected STATCOM, using either TR2 or the spare TR3 as the main coupling transformer. Inverter #2 can be operated as a second shunt-connected STATCOM using TR3, or else connected in series with the Big Sandy transmission line through the TR4 insertion transformer. When Inverter #2 is connected in series with the line and joined to inverter #1 through the DC bus, then the two inverters constitute a full UPFC. Alternatively Inverter #2 can be disconnected from Inverter #1 and connected in series with the line to operate as an SSSC.

II. Introduction

Inverter #1 has been commissioned previously. Inverter #2 has already been commissioned to operate as a second shunt-connected STATCOM in conjunction with the spare shunt transformer, TR3. All of the preliminary checkout that would normally be specified for a newly installed inverter has thus already been completed. This includes visual and functional checkout of the pole structures and all auxiliary equipment such as cooling system and auxiliary power supplies.

This test plan specifies a sequence of tests to verify the capability of Inverter #2 to operate in series with the line. In particular the tests are directed at the case where Inverter #2 is part of a UPFC, although the functions checked also cover the requirements for SSSC operation and it should not be

necessary to do further testing before proceeding to SSSC commissioning. The test sequence leads up to and includes insertion of Inverter #2 into the line and basic checkout of operating modes, but does not include a more formal array of commissioning tests that will be specified by AEP to verify the performance of the equipment. Through all of the following tests it is assumed that the Big Sandy line will be available for service. However, as a precaution, the Big Sandy line will be switched out during the early steps of the tests to insure that the no disturbances introduced to the AEP system when the UPFC equipment is switched in. It is also assumed that Inverter #1 will not be in service continuously, and that it will be possible to start or stop it as needed for the various tests.

III. Commissioning Test Results for Series Converter Operating in SSSC mode

For this test, the shunt inverter is disconnected from the DC terminals of the series inverter and is completely out of service. Consequently the Inez bus voltage is not regulated. The series inverter injects voltage into the line essentially in quadrature with the prevailing line current. The injection angle deviates from true quadrature to draw real power from the line for inverter losses and to charge and discharge the DC bus capacitor banks. By means of the quadrature voltage injection, the SSSC is able to raise or lower the line current, but cannot independently alter P and Q. In principle, the SSSC can reverse the direction of power flow on a line, but the control becomes difficult as the line current is reduced through zero, at which point real power cannot be drawn from the line. SSSC operation is an important subset of full UPFC operation, because it can be used when the shunt inverter is not available. A single series-connected inverter installation may be the most cost effective solution for applications where a simpler form of power flow control is sufficient.

The objective of the test is simply to show the SSSC raising and lowering the power on the Big Sandy line. The SSSC is operated to control the magnitude and the polarity of the injected voltage (i.e., the line power is not automatically controlled). Voltage injections are selected to give a sequence of approximately 100 MW, 180 MW, 250 MW, and finally 200 MW on the line (Figure 8.8). Note the corresponding changes in Q. From the phasor diagrams (Figure 8.9) it can be clearly seen how I_{line} maintains a constant phase relationship to V_1 and is always in quadrature with V_{21} . The natural flow on the line is between 100 MW and 180 MW. Consequently the polarity of V_{21} is reversed from lagging I_{line} to leading in this transition. The polarity reversal is accomplished by taking the DC bus voltage first to zero, then raising it again with 180 degree phase shift in the inverter output voltage.

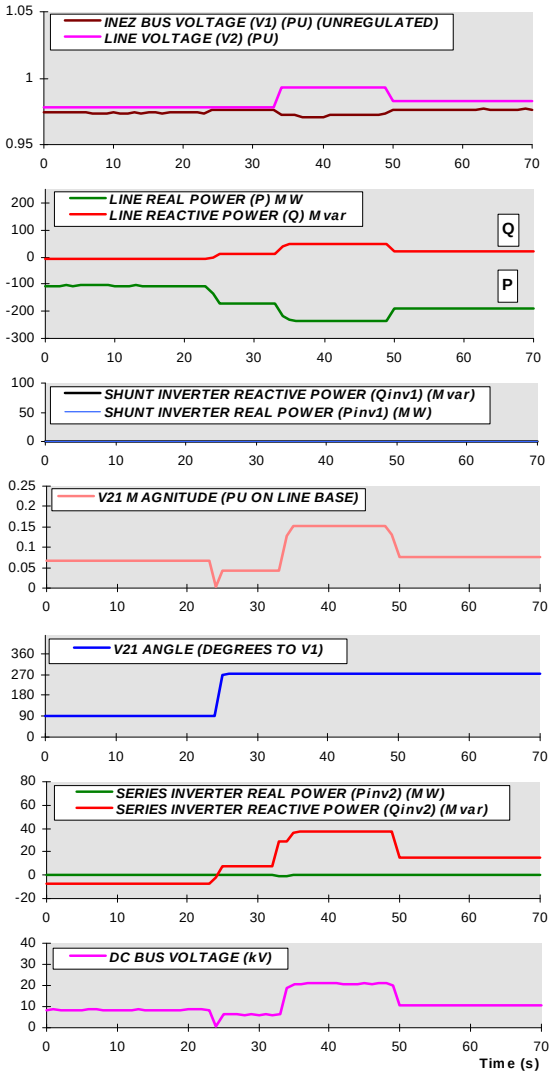


Figure. 8.8 Case 5: Series inverter operating in SSSC mode

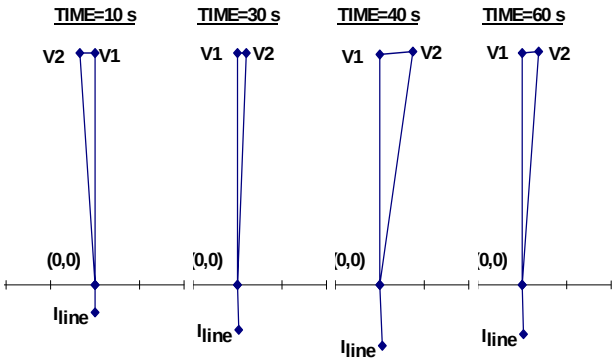


Fig. 8.9 Case 5. Series inverter operating in stand-alone SSSC Mode

8.2.2 UPFC Kangjin, Kepco, Korea

8.2.2.1 Overview

Purpose

The purpose for the UPFC Kangjin is the control of electrical power flow on transmission lines and dynamic voltage regulation of the Kangjin substation bus. Further intentions include testing of FACTS devices within KEPCO's transmission system.

Modes of operation

The UPFC Kanjin can be used as a STATCOM, a UPFC or a SSSC.

Single line

The single line of the UPFC Kanjin is shown in Figure 8.10 below.

Basic data

HV system voltage	154 kV
LV system voltage	4.285 kV
DC bus voltage	± 4.801 kV
Converter rating	2 x ± 40 MVA
Type of semiconductor	GTO 4.5 kV / 4 kA
Type of converter	3 level
Number of converter sections	4
Pulse number	24
Number of series connected GTOs	4/4
Cooling	50/50% EG/Water
Ambient temperature	–37/40 ˚C

Commissioning schedule

Commissioning took place from July to November 2002.

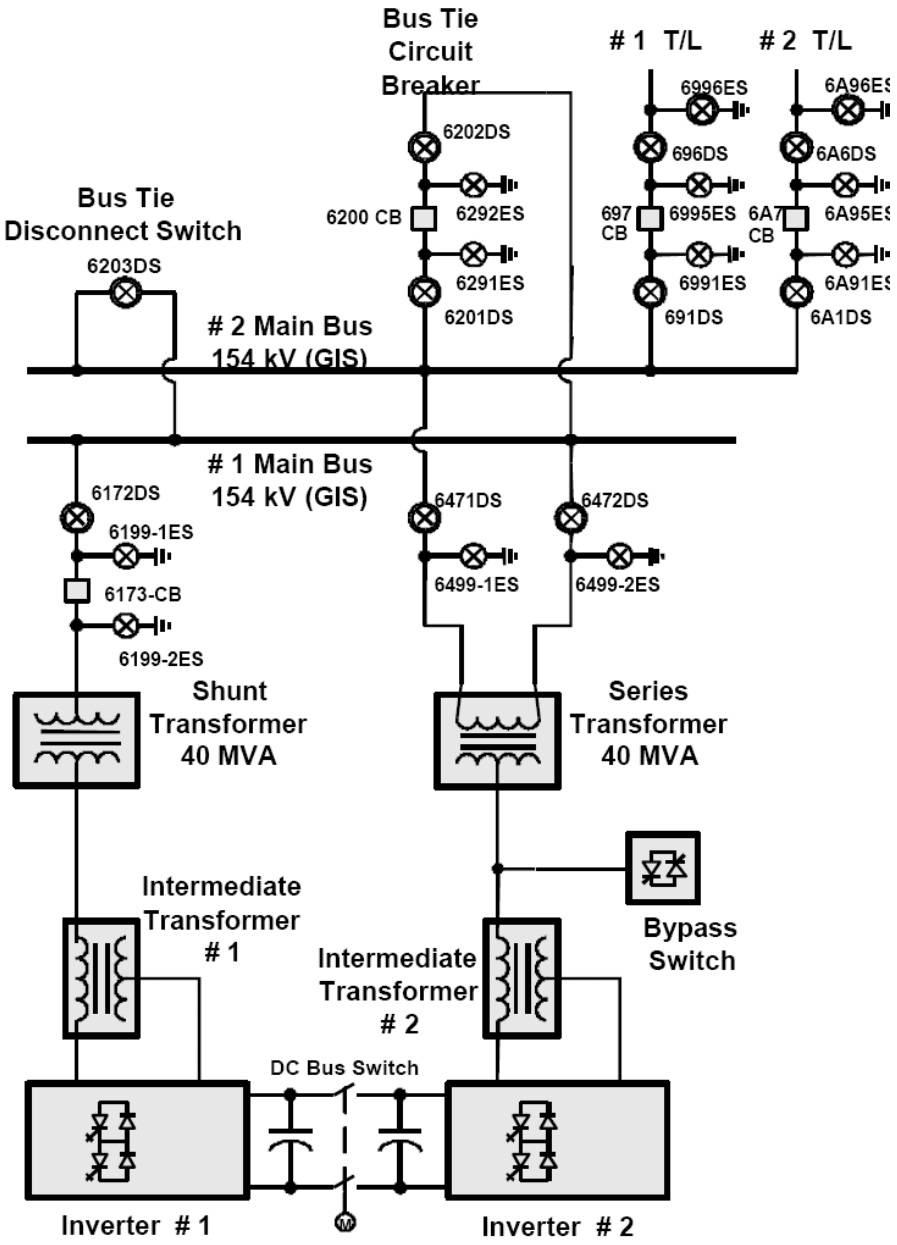


Figure 8.10 Single line of the UPFC Kanjin.

8.2.2.2 Commissioning and test results

I. Background

The purpose for the Unified Power Flow Controller (UPFC) at Kangjin is the control of electrical power flow on transmission lines and dynamic voltage regulation of the Kangjin substation bus.

The UPFC employs two identical voltage-sourced, GTO thyristor based inverters, each with a nominal steady-state rating of ±40 MVA, and each capable of full 4-quadrant operation. Each ±40 MVA inverter is structured to generate a three-phase, 24-pulse sinusoidal voltage waveform. Both converters are connected to the 154 kV Kangjin substation through a 40 MVA shunt coupling transformer and a 40 MVA series transformer.

The simplified single-line diagram in Figure 8.10 shows the configurable connection of the equipment in shunt and/or in series with the transmission lines. This allows the following three power circuit configurations:

STATCOM (DC bus switch open) Configuration # 1: Inverter #1 connected to the shunt transformer secondary and in shunt with the substation bus. Inverter #2 not used.

SSSC (DC bus switch open) Configuration # 2: Inverter #2 connected to the series transformer secondary and in series with the transmission line. Inverter #1 not used.

UPFC (DC bus switch closed) Configuration # 3: Inverter #1 connected to the shunt transformer secondary and in shunt with the substation bus. Inverter #2 connected to the series transformer secondary and in series with the transmission line.

These power circuit configurations are summarized in Table 8.1. Please note that the circuit breakers and disconnect switches shown are only the primary devices and the grounding switches and other disconnects and breakers are not shown to simplify the table. These inverters can be reconfigured to provide different modes of operation. For example, within a SSSC configuration, the series inverter may be run in either voltage injection mode or the more sophisticated power flow control mode. This is also true for the UPFC configuration, in which case also the series inverter may be run in either open loop voltage injection mode or closed loop power flow control mode.

Table 8.1 UPFC Configurations with Switch States

		Inverter Connection		Switch States (O=open, C=closed)				
Config	Type	Inv #1 to	Inv #2 to	DC Bus	6173 CB	6200 CB	6472 DS	6471 DS
1	STATCOM	Sh Transf.	not used	O	C	C	O	O
2	SSSC	not used	Ser Transf.	O	O	O	C	C
3	UPFC	Sh Transf.	Ser Transf.	C	C	O	C	C

For safety, power circuit configuration changes are only permitted when the equipment is de-energized and isolated from the line. Operating control mode changes, however, are permitted while the inverters are running.

The KEPCO SSSC was tested in both the “open-loop” voltage injection control mode and “closed-loop” automatic power flow control mode on the 154kV transmission line as indicated in Figure 8.11. The ±1.0 pu injected voltage changes the power flow on the 154kV transmission line up to +43 MW as shown in the Table 8.2.

Table 8.2 Test of SSSC Operating Range

Ref. V (p.u)	V_{inj2} (pu on 89kV)	I_{line2} (pu on 2200 A)	P_{line2} MW	Q_{line2} MVAR
0.000	0.002	0.092	55	-5
0.030	0.002	0.094	56	-5
0.100	0.006	0.100	60	-5
0.200	0.012	0.108	65	-6
0.300	0.019	0.116	69	-8
0.400	0.025	0.123	73	-9
0.500	0.032	0.131	78	-11
0.600	0.038	0.139	82	-13
0.700	0.045	0.147	89	-14
0.800	0.051	0.155	90	-16
0.900	0.058	0.162	95	-18
1.000	0.064	0.169	98	-21
-0.020	0.003	0.087	51	9

(a) Voltage injection control mode

The SSSC was first operated in open-loop voltage injection control mode to verify its operation by measuring the line current magnitude (and power flow change). With the inverter #2 gating and the bypass CB 6200 open, the injected voltage was slowly varied from 0 to +1 pu (capacitive) in gradual steps and the effect on system parameters was noted as given in Table 8.2. The line power flow changed from 55MW (at zero voltage injection or uncompensated line) to 98MW, an increase of 43MW on the 154kV transmission line. The line current magnitude increased linearly from 0.09pu to 0.17pu.

The SSSC voltage injection was not tried in the inductive region because the line current was too low for predictable operation.

Note that as explained in Section 8.1.1, with the SSSC the change in line reactive power flow is uncontrolled. With the given 154kV transmission line parameters, the line reactive power changes by approximately +15MVAR.

(b) SSSC dynamic characteristics

The dynamic characteristics of the SSSC were tested in "open-loop" voltage injection control mode. All tests were performed under normal system conditions with the nominal (uncompensated) line current of about 0.1 pu. The SSSC was energized into the transmission line at zero voltage reference. The injected voltage reference was initially changed in small steps and then larger steps as the controller was shown to be stable. The SSSC dynamic characteristics are shown with increased injected voltage reference steps and ramp rates.

Table 8.3 shows the SSSC step response to voltage injection of +0.1pu and +0.2pu. The change in the line current magnitude and the line power is shown before and after the step voltage injection. The quantities tabulated for all the tables below are:

Transmission line current ('I_{line2}' on the operator screen), per unit on 2200 Amps
Injected voltage ('V_{inj2}' on the operator screen), per unit on 88.9 kV
Transmission line active power ("P_{line2}" on the operator screen), MW
Transmission line reactive power ("Q_{line2}" on the operator screen), MVAR

Table 8.3 SSSC step response

SSSC Voltage Injection V Ref. Change			BEFORE				AFTER			
			I_{line2} (pu)	V_{inj2} (pu)	P_{line2} (MW)	Q_{line2} (MVAR)	I_{line2} (pu)	V_{inj2} (pu)	P_{line2} (MW)	Q_{line2} (MVAR)
0.3	To	0.4	0.113	0.019	67	-7	0.121	0.025	72	-8
0.4	To	0.3	0.121	0.025	72	-8	0.113	0.019	68	-3
0.3	To	0.5	0.112	0.019	68	-3	0.128	0.032	77	-5

Figure 8.11 shows the SSSC injected voltage step response from 0.3 pu to 0.6 pu. The injected voltage increase and the DC bus voltage change are shown to change in 600 ms. The injected voltage reference ramp rate is 0.94 pu/sec.

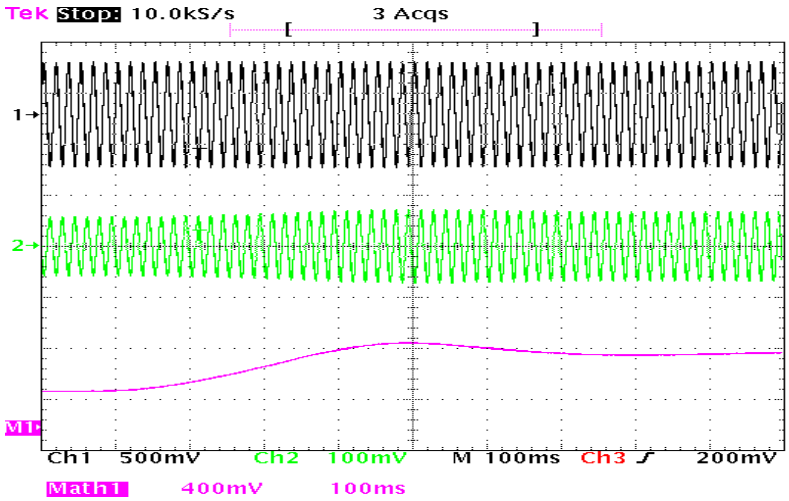


Figure 8.11 SSSC step response with injected voltage reference (+0.3pu to +0.6pu)
Channel 1 = Phase A Bus voltage (VB1A), scaling: 0.5V peak = 1pu
Channel 2 = Phase A line current (ISEP1A), scaling: 0.5V peak = 1pu
Channel M1 = Total DC voltage (VDC2P – VDC2N), scaling 1V = 1pu

Table 4 shows the SSSC step response to voltage injection of +0.4 pu and +0.5 pu with a higher controller gain. The change in the line current magnitude and the line power is shown before and after the step voltage injection.

Table 8.4 SSSC step response

SSSC Voltage Injection V Ref. Change			BEFORE				AFTER			
			I_{line2} (pu)	V_{inj2} (pu)	P_{line2} (MW)	Q_{line2} (MVAR)	I_{line2} (pu)	V_{inj2} (pu)	P_{line2} (MW)	Q_{line2} (MVAR)
0.2	To	0.6	0.106	0.013	64	2	0.138	0.039	82	-2
0.6	To	0.2	0.138	0.039	82	-2	0.106	0.013	64	2
0.2	To	0.7	0.106	0.013	64	2	0.145	0.045	86	-3

Figure 8.12 shows the SSSC injected voltage step response from 0.3 pu to 0.6 pu. The injected voltage increase and the DC bus voltage change are shown to change in 300-400 ms. This result shows

the impact of the higher controller gain resulting in a faster response. Figure 8.13 shows the SSSC injected voltage step response from 0.2 pu to 0.7 pu. The injected voltage increase and the DC bus voltage change are shown to change in 600-800 ms. This verifies that response time is proportional to the step of the injected voltage. The injected voltage reference ramp rate is 0.94 pu/sec for both cases.

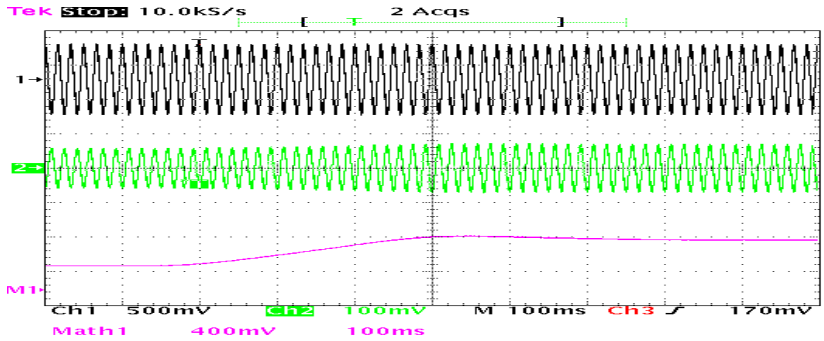


Figure 8.12 SSSC step response with injected voltage reference (+0.3 pu to +0.6 pu)
Channel 1 = Phase A Bus voltage (VB1A), scaling: 0.5V peak = 1pu
Channel 2 = Phase A line current (ISEP1A), scaling: 0.5V peak = 1pu
Channel M1 = Total DC voltage (VDC2P – VDC2N), scaling 1V = 1pu

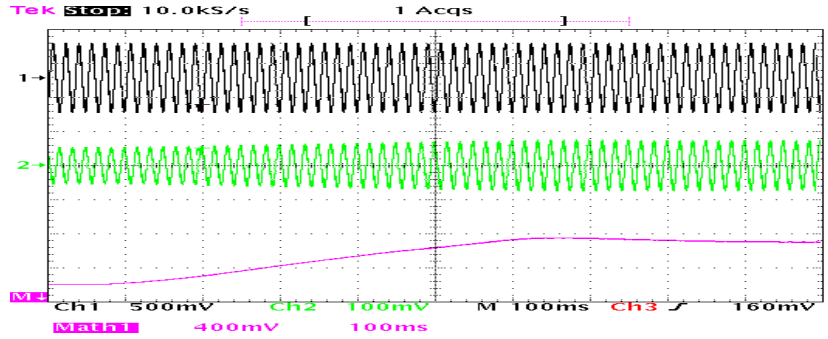


Figure 8.13 SSSC step response with injected voltage reference (+0.2 pu to +0.7 pu)
Channel 1 = Phase A Bus voltage (VB1A), scaling: 0.5V peak = 1pu
Channel 2 = Phase A line current (ISEP1A), scaling: 0.5V peak = 1pu
Channel M1 = Total DC voltage (VDC2P – VDC2N), scaling 1V = 1pu

Table 8.5 below shows the SSSC step response to voltage injection of +0.5 pu with an increased injected voltage reference ramp rate from 0.94 pu/sec to 2.8 pu/sec (three times increase). The change in the line current magnitude and the line power is shown before and after the step voltage injection.

Figure 8.14 shows the SSSC injected voltage step response from 0.2 pu to 0.7 pu. The injected voltage increase and the DC bus voltage change are shown to change in 300-400 ms. This result show the impact of the higher injected voltage reference ramp rate resulting in a faster response. The response also shows a slight overshoot in the dc bus voltage.

Table 8.5 SSSC step response

SSSC Voltage Injection *V* Ref. Change			BEFORE				AFTER			
			I_{line2} (pu)	V_{inj2} (pu)	P_{line2} (MW)	Q_{line2} (MVAR)	I_{line2} (pu)	V_{inj2} (pu)	P_{line2} (MW)	Q_{line2} (MVAR)
0.2	to	0.7	0.106	0.013	64	2	0.146	0.045	88	3
0.7	to	0.2	0.146	0.045	88	3	0.106	0.013	64	2

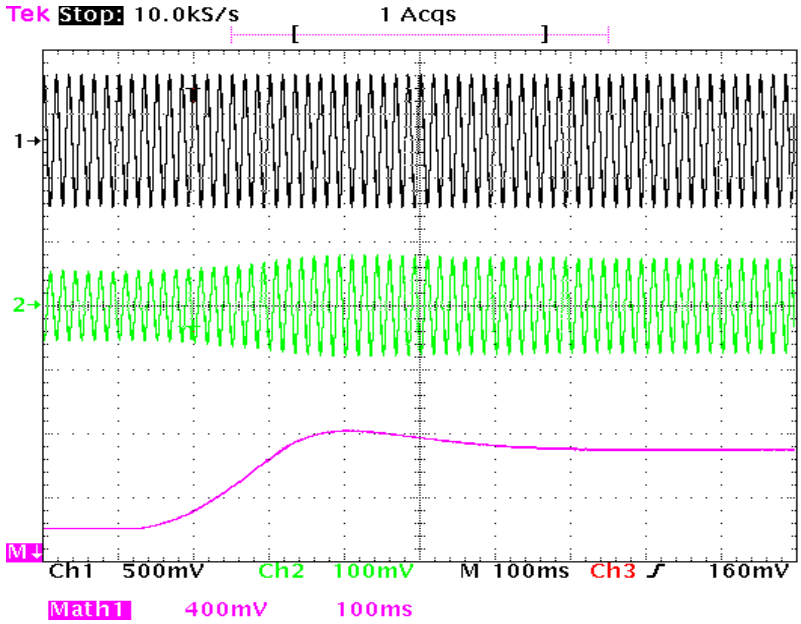


Figure 8.14 SSSC step response with injected voltage reference = 0.2 pu to 0.7 pu
Channel 1 = Phase A Bus voltage (VB1A), scaling: 0.5 V peak = 1 pu
Channel 2 = Phase A line current (ISEP1A), scaling: 0.5 V peak = 1 pu
Channel M1 = Total DC voltage (VDC2P – VDC2N), scaling 1 V = 1 pu

Table 8.6 shows the SSSC step response to voltage injection with an increased injected voltage reference ramp rate from 2.8 pu/sec to 5.6 pu/sec, and reduced integral controller gain to reduce the overshoot observed in the DC bus voltage in Figure 8.14. The change in the line current magnitude and the line power is shown before and after the step voltage injection.

Table 8.6 SSSC step response

SSSC Voltage Injection *V* Ref. Change			BEFORE				AFTER			
			I_{line2} (pu)	V_{inj2} (pu)	P_{line2} (MW)	Q_{line2} (MVAR)	I_{line2} (pu)	V_{inj2} (pu)	P_{line2} (MW)	Q_{line2} (MVAR)
0.2	to	0.8	0.106	0.013	64	2	0.152	0.052	91	2
0.8	to	0.2	0.152	0.052	91	2	0.105	0.013	63	6
0.2	to	0.9	0.105	0.013	63	6	0.160	0.058	96	1
0.9	to	0.2	0.160	0.058	96	1	0.105	0.013	63	6
0.2	to	1.0	0.105	0.013	63	6	0.167	0.065	101	0

Figures 8.15 and 8.16 show the SSSC injected voltage step response from 0.2 pu to 1.0 pu and from 1.0 pu to 0.2 pu, with the voltage injection ramp rate of 5.6 pu/sec. This means that the injected

voltage reference is ramped from 0 to 1.0 pu in approximately 180 ms which is approximately 11 cycles. The injected voltage increase and the DC bus voltage change are shown to change in 350 ms. This result shows the impact of the higher injected voltage reference ramp rate resulting in a faster response. The response shows slightly less overshoot in the DC bus voltage due to lower integral controller gain.

In this SSSC tests, it was not possible to inject inductive voltage due to limits imposed by the network, i.e., the line current was too low.

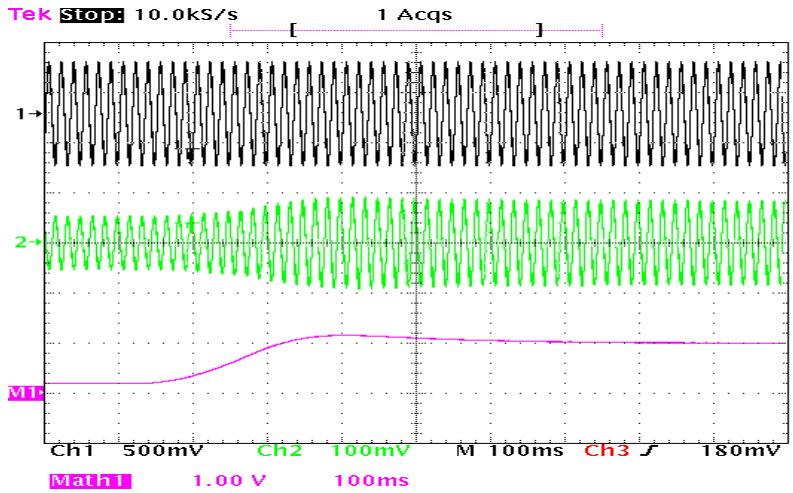


Figure 8.15 SSSC step response with injected voltage reference = 0.2 pu to 1.0 pu
Channel 1 = Phase A Bus voltage (VB1A), scaling: 0.5 V peak = 1 pu
Channel 2 = Phase A line current (ISEP1A), scaling: 0.5 V peak = 1 pu
Channel M1 = Total DC voltage (VDC2P – VDC2N), scaling 1 V = 1 pu

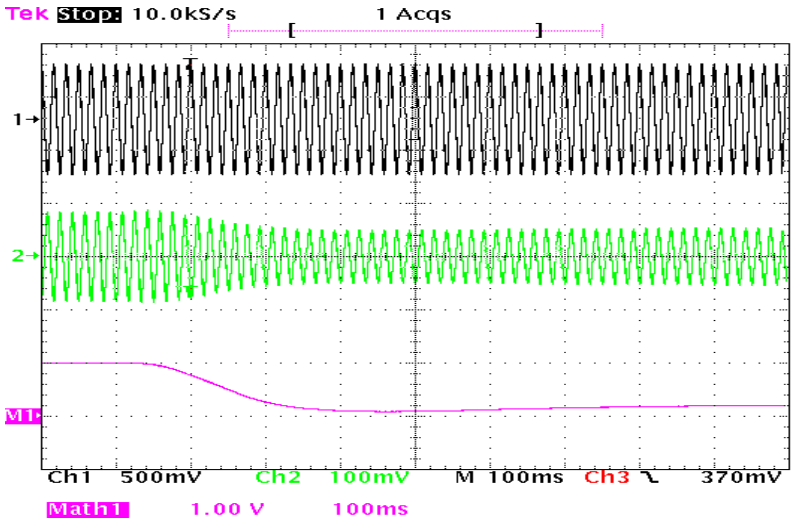


Figure 8.16 SSSC step response with injected voltage reference = 1.0 pu to 0.2 pu
Channel 1 = Phase A Bus voltage (VB1A), scaling: 0.5 V peak = 1 pu
Channel 2 = Phase A line current (ISEP1A), scaling: 0.5 V peak = 1 pu
Channel M1 = Total DC voltage (VDC2P – VDC2N), scaling 1 V = 1 pu

8.2.3 CSC Marcy, NYPA, USA

8.2.3.1 Overview

Purpose

The project Convertible Static Compensator (CSC) was developed by New York Power Athority (NYPA) and Electric Power Research Institute (EPRI) to establish further control concepts for all the inverter-based FACTS Controllers on one side and also to provide benefits to the New York Transmission system that would allow additional system flow for a variety of loading patterns and contingencies. Transmission planning studies have shown that for many conditions the CSC could allow increases of 120 MW and 240 MW across the Central-East and Total-East interfaces, respectively. In addition, the CSC has potential to improve system dynamic damping and operating flexibility.

Modes of operation

The CSC can be used in eleven configurations:

STATCOM 1
STATCOM 2
both STATCOM
SSSC 1
SSSC 2
Both SSSC
STATCOM 1 + SSSC 2
STATCOM 2 + SSSC 1
UPFC 1
UPFC 2
IPFC

Basic data

HV system voltage	345 kV
LV system voltage	5.357 kV
DC bus voltage	±6.014 kV
Converter rating	2 x ±100 MVA
Type of semiconductor	GTO 4.5 kV/4 kA
Type of converter	3 level
Number of converter sections	4
Pulse number	48
Number of series connected GTOs	5/5
Cooling	50/50% EG/Water
Ambient temperature	–34/38˚C

Commissioning schedule

The project was finally commissioned in October 2003

Single line

The single-line diagram of the CSC Marcy is shown in Figure 8.17.

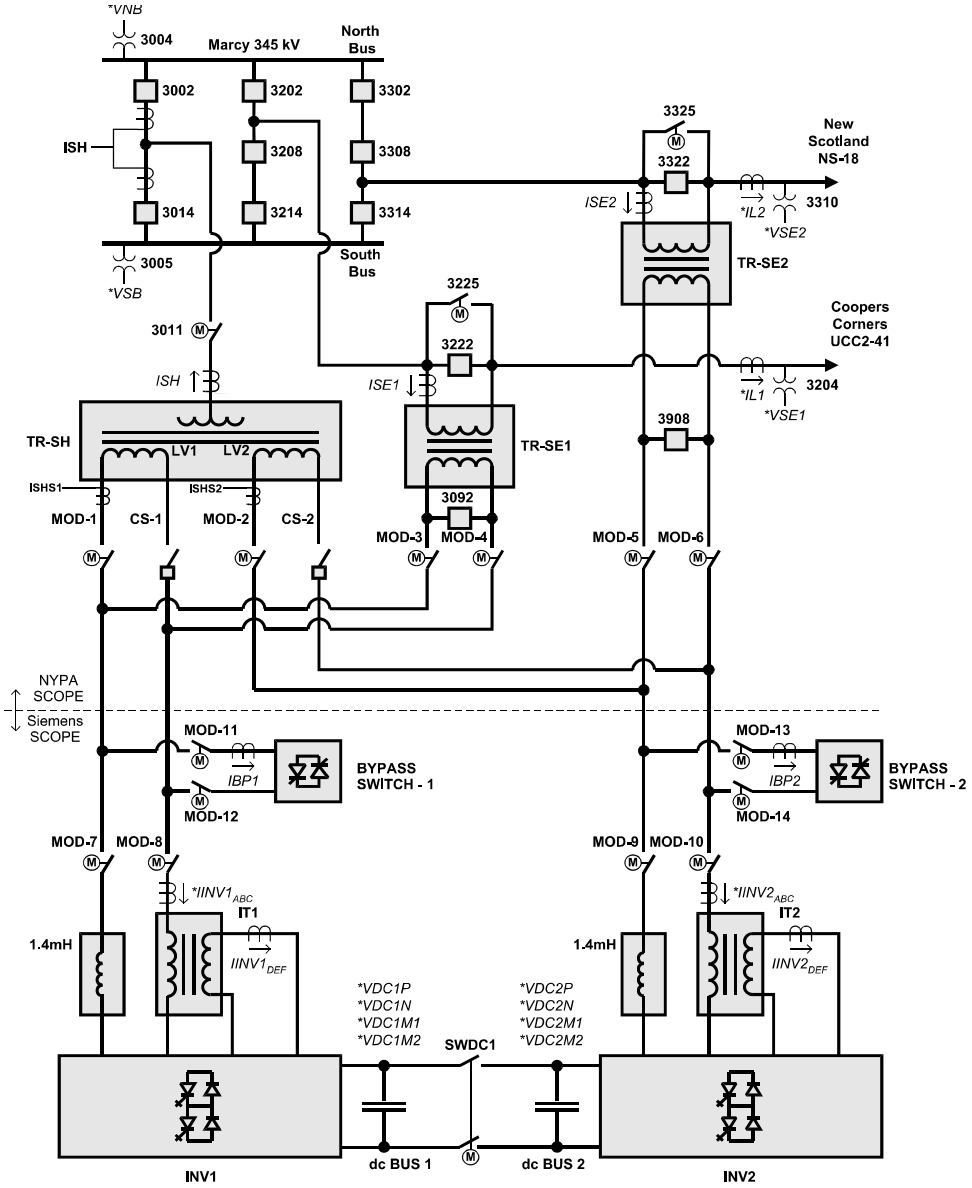


Fig. 8.17 Single-line diagram of the CSC Marcy Substation

The CSC installed at the Marcy 345 kV substation as shown in Figure 8.17, consists of two 100 MVA voltage source inverters, two 100 MVA series transformers, and a single 200 MVA shunt transformer with two identical secondary windings. The low-voltage disconnect switches allow utilization of the two inverters in various shunt and series configurations. The CSC provides four basic functionalities, namely, STATCOM, SSSC, UPFC, and IPFC, resulting in a total of 11 different configurations on both the 345 kV lines, as shown in Figure 8.17. Each series configuration also has a Thyristor Bypass Switch (TBS1 and TBS2), a low-side and high-side circuit breaker (LVCB and HSB) for fault protection as shown in Figure 8.18.

8.2.3.2 Commissioning and test results

NYPA CSC System Description

A simplified one-line diagram of the general CSC configuration is shown in Figure 8.18. The circuit configuration selection display is shown in Figure 8.19.

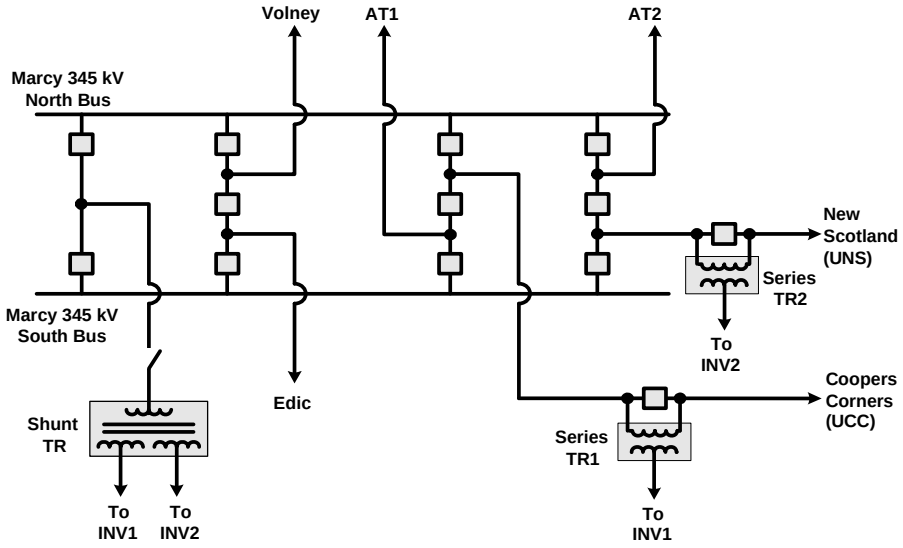


Fig. 8.18 Simplified one-line diagram of Marcy 345 kV substation with the CSC connections

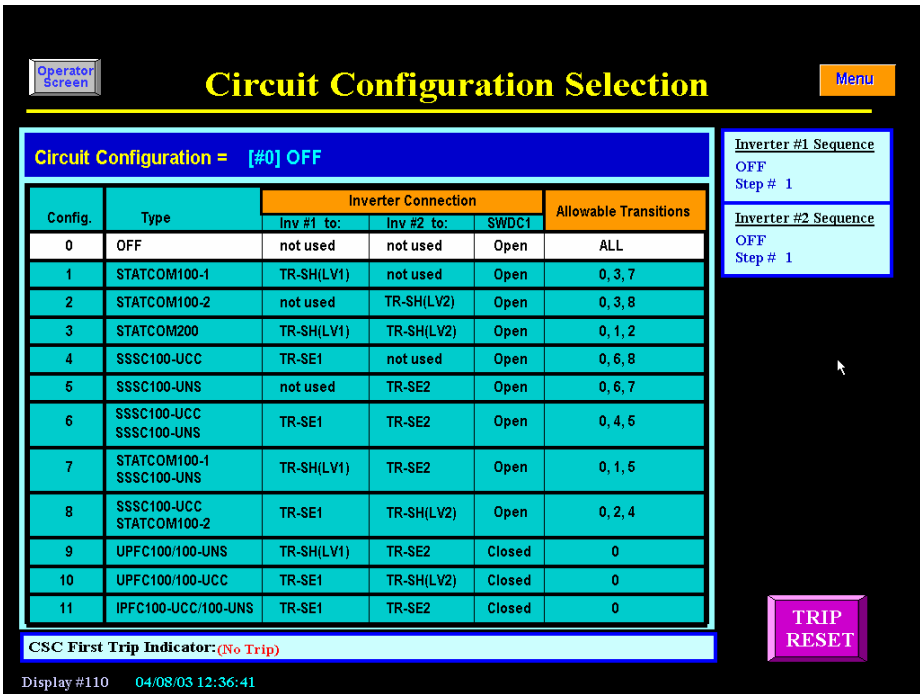


Figure 8.19 Eleven possible configuration selections of CSC

NYPA CSC System SSSC Test Result

The NYPA CSC system SSSC was tested in both the "open-loop" voltage injection control mode and "closed-loop" automatic power flow control mode on both the UCC and UNS lines (as indicated in Figure 8.18). The ±1.0 pu injected voltage changes the power flow on the UCC line up to +60 MW (Figure 8.20) and on the UNS line up to +100 MW (Figure 8.21).

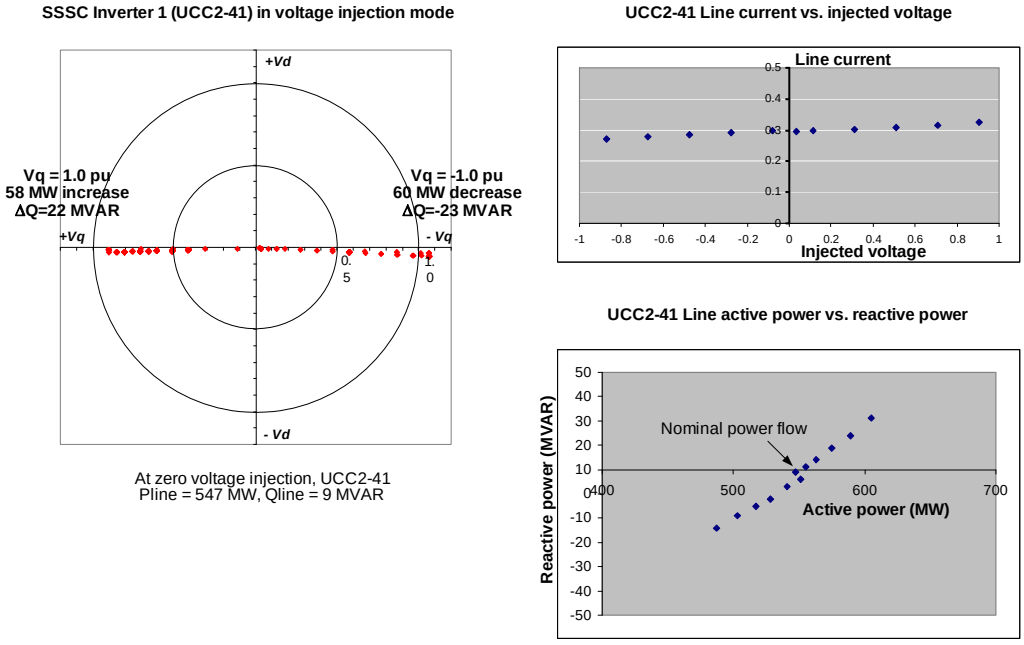


Figure 8.20 SSSC 1 Operating Characteristics

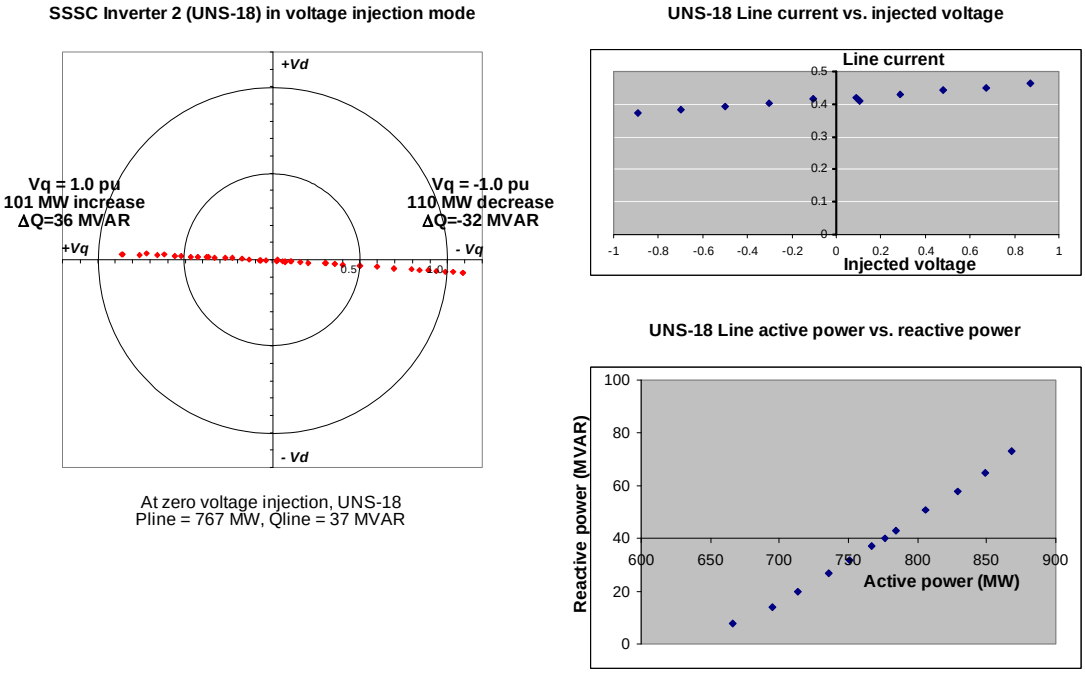


Figure 8.21 SSSC 2 Operating Characteristics

(a) Voltage injection control mode

To understand the SSSC operation and its influence in line current magnitude change and real power flow change on the UCC and UNS lines, the SSSC was started in the "open-loop" voltage injection mode. The voltage injection was slowly increased in steps of +0.1 pu to +1.0 pu on one end and then decreased to –1.0 pu. At each step, system parameters such as line current magnitude, real and reactive line power flows, and voltage across the SSSC were recorded. The SSSC voltage injection is in quadrature with the line current which was essentially in phase with the Marcy bus voltage. The quadrature (q) axis voltage injection has more influence on the real power flow in the transmission line. This is because this direction of voltage injection changes the phase of the transmission line voltage which mainly affects the real power flow in the line. The SSSC voltage injection does change the transmission line voltage magnitude enough to influence the reactive power flow but the main influence is on the real power. As mentioned above (in Section **8.1.1**), the change in line reactive power flow is uncontrolled.

Tables 8.7 and 8.8 summarize the system parameters recorded at various voltage injection reference values from +1.0 pu to –1.0 pu on the Coopers Corner (UCC) and New Scotland (UNS) lines respectively. The maximum change in power flow on the Coopers Corners (UCC) line from zero to +1.0 pu voltage injection is an increase of 58 MW and from zero to –1.0 pu is a decrease of 64 MW. The maximum change in power flow on the New Scotland (UNS) line from zero to +1.0 pu voltage injection is an increase of 101 MW and from zero to –1.0 pu is a decrease of 110 MW. From the test results it could be seen that the SSSC on the New Scotland line has more influence on the real power flow than the SSSC on the Coopers Corner line. The DC bus measurements show how the SSSC controls the injected voltage by controlling the DC bus voltage V_{dc}. In the voltage source converter (VSC) circuit topology used in the CSC, the DC bus voltage is linearly proportional to the injected voltage. If the VSC was "vector controlled", meaning that the magnitude and phase of the converter voltage can be independently controlled, then the DC bus voltage would be regulated to a constant value. In this case, the SSSC injected voltage would be controlled by varying the pulse-width of the converter voltage.

Table 8.7 SSSC 1 voltage injection affect on UCC2-41 line power flow

Pline1 (MW)	Qline1 (MVAR)	Iline1 (pu)	Vline1 (pu)	Vinj1 (pu)	SSSC1 Inj Volts Ref.	Pos. DC Bus (kV)	Neg. DC Bus (kV)
605	31	0.326	1.031	0.904	1.0	5.95	6.05
589	24	0.316	1.033	0.706	0.8	4.92	4.77
575	19	0.310	1.032	0.510	0.6	3.59	3.58
563	14	0.303	1.032	0.313	0.4	2.33	2.37
555	11	0.298	1.031	0.116	0.2	1.22	1.16
547	9	0.296	1.030	0.033	0.05	0.28	0.31
487	-14	0.263	1.026	1.065	-1.0	6.02	6.03
503	-9	0.273	1.026	0.869	-0.8	4.81	4.84
517	-5	0.278	1.027	0.671	-0.6	3.58	3.55
528	-2	0.285	1.028	0.474	-0.4	2.35	2.39
541	3	0.291	1.028	0.278	-0.2	1.18	1.21
551	6	0.298	1.029	0.079	0.0	0.02	0.02

Table 8.8 SSSC 2 voltage injection affect on UNS-18 line power flow

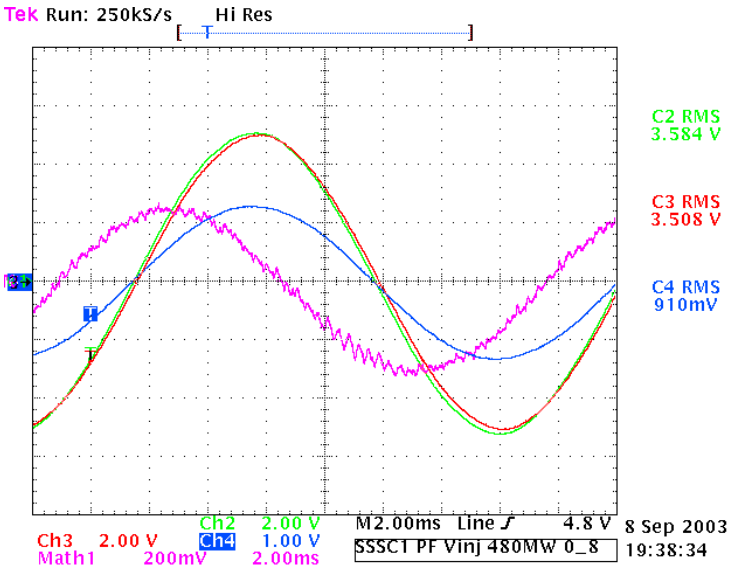
Pline2 (MW)	Qline2 (MVAR)	Iline2 (pu)	Vline2 (pu)	Vinj2 (pu)	SSSC2 Inj Volts Ref.	Pos. DC Bus (kV)	Neg. DC Bus (kV)
767	37	0.409	1.040	0.104	0.0	0.01	0.02
784	43	0.419	1.041	0.089	0.2	1.20	1.08
806	51	0.431	1.042	0.285	0.4	2.53	2.41
829	58	0.442	1.042	0.479	0.6	3.64	3.55
849	65	0.450	1.043	0.675	0.8	4.75	4.73
868	73	0.463	1.044	0.872	1.0	5.96	5.88
666	8	0.360	1.033	1.089	-1.0	5.92	6.12
695	14	0.372	1.034	0.893	-0.8	4.98	4.81
713	20	0.383	1.035	0.697	-0.6	3.55	3.61
736	27	0.393	1.036	0.502	-0.4	2.39	2.42
751	32	0.402	1.038	0.302	-0.2	1.21	1.22
776	40	0.416	1.038	0.105	0.0	0.01	0.01

Figure 8.20 shows the SSSC1 (SSSC in UCC line) operating points in "open-loop" voltage injection control mode. The change in real and reactive power flow at +1.0 pu voltage injection points are indicated. A plot of the Coopers Corners (UCC) line current versus injected voltage indicates a linear relationship. The change in real and reactive power flow at various voltage injection points is also indicated in Figure 8.20. The nominal (uncompensated) operating line power flows are 547 MW and 9 MVAR. It can be seen that the reactive power flow in the line is uncontrolled and equal to +22 MVAR. The plot of line *P* and *Q* is also shown in Figure 8.20.

Figure 8.21 shows the SSSC2 (SSSC in UNS line) operating points in voltage injection control mode. The change in real and reactive power flow at +1.0 pu voltage injection points are indicated. A plot of the New Scotland (UNS) line current versus injected voltage indicates a linear relationship. The change in real and reactive power flow at various voltage injection points is also indicated in Figure 8.21. The nominal (uncompensated) operating line power flows are 767 MW and 37 MVAR. It can be seen that the reactive power flow in the line is uncontrolled and equal to –32 MVAR and +36 MVAR. The plot of line *P* and *Q* is also shown in Figure 8.21.

Figure 8.22 shows the Marcy Bus voltage, line voltage, line current, and injected voltage on the Coopers Corners (UCC) line for a voltage injection reference of negative 0.8 pu. The line current is in phase with the bus voltage and the injected voltage is in quadrature with the line current. The phase angle convention is such that for inductive compensation the injected voltage leads the line current by 90 degrees. In this case the injected voltage is calculated from the difference between the Marcy bus voltage and the line voltage (Vbus–Vline). The waveform shows the line voltage slightly lagging the bus voltage which will tend to reduce real power flow in the line.

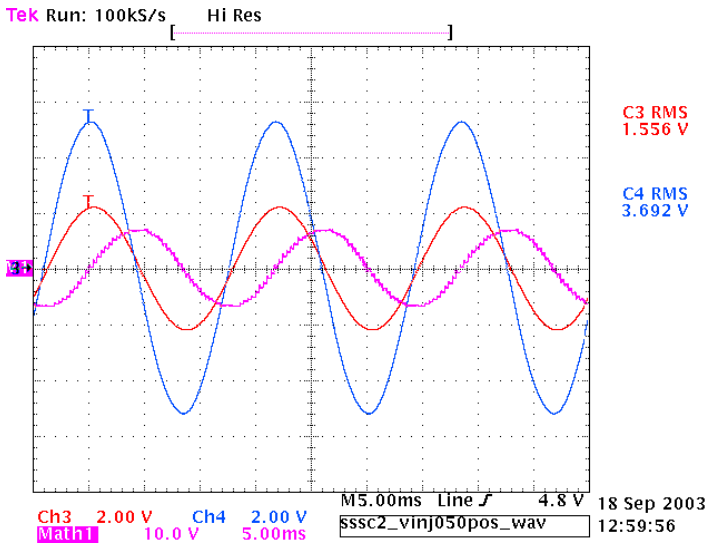
Note that with the SSSC, reactive power flow on the lines is uncontrolled, as indicated in Figures 8.20 and 8.21. The slight angular deviation of voltage injection from the q-axis (as shown in Figures 8.20 and 8.21) is due to the requirement of real power for inverter losses. Since the voltage injection is measured on the line side, the transformer leakage voltage drop is shown as subtracting/ adding on the positive/negative q-axis, respectively. This explains the small difference in the net real power flow change for +1.0 pu voltage injection, as shown in Figures 8.20 and 8.21.



Ch2=Vbus phase A, Ch3=Vline phase A, Ch4=I line phase A, Math=Ch2-Ch3

Figure 8.22 SSSC 1 voltage injection at V_ref=-0.8 pu

The Figure 8.23 shows the Marcy Bus voltage, line voltage, line current, and injected voltage on the New Scotland (UNS) line for a voltage injection reference of positive 0.5 pu. The line current is in phase with the bus voltage and the injected voltage is in quadrature with the line current. The phase angle convention is such that for capacitive compensation the injected voltage lags the line current by 90 degrees. The injected voltage was measured across the series transformer secondary winding.



Ch3 = N.S. Line current Ph-C (5V = 1pu), Ch4 = Marcy Bus voltage Ph-C (5V = 1pu)
Math = TBS C1 voltage - TBS C2 voltage (injected voltage scale 1V = 2000V)

Figure 8.23 SSSC 2 voltage injection at V_ref= +0.5 pu

(b) Power Flow control mode:

The SSSC at NYPA was also tested in "closed-loop" power flow control mode. The real power flow reference was slowly increased in steps of 5 MW until +1.0 pu voltage injection was reached. The real power flow reference was then reduced in steps of 5 MW until -1.0 pu voltage injection was reached. At each step it was verified that the control was stable and regulated the real power flow in the line properly.

The range of controllable real power flow on the Coopers Corners (UCC) line during the test was 458 MW and up to 554 MW. The range of controllable real power flow on the New Scotland (UNS) line during the test was 670 MW and up to about 910 MW. These controllable power flow ranges are as expected, and exactly the same as the results obtained by "open-loop" voltage injection control mode case as given in Figures 8.20 and 8.21.

Figure 8.24 illustrates the ability of SSSC to control real power flow on the UCC line (i.e. Coopers Corners) in the automatic power flow control mode. The real power reference in the line is 480 MW. In this case, the SSSC was used to reduce the real power flow to 480 MW from the uncompensated real power flow of 502 MW. At the end of the test the SSSC was shutdown and the line power returned to 502 MW. The regulation of the real power flow in the line is achieved by the SSSC by constantly adjusting its voltage injection magnitude as shown in Figure 8.24. This implies that due to system condition changes the line current magnitude is regulated by the SSSC to keep the real power flow constant on the line. The horizontal axis on the figure is time. This result validates the automatic power flow control mode for the SSSC.

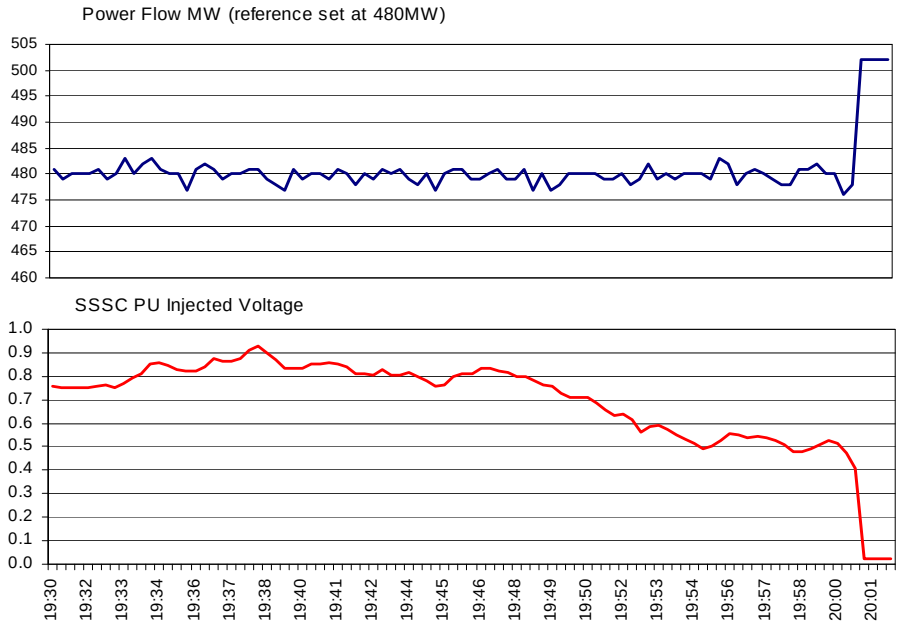


Figure 8.24 SSSC 1 in power flow control (set at 480 MW)

Figure 8.25 illustrates the ability of SSSC to control real power flow on the UNS line (i.e., the New Scotland line) in the automatic power flow control mode. In this case, the SSSC was used to boost and regulate power flow by as much as 100 MW to 840 MW. The uncompensated real power flow in the line was 740 MW. At the end of the test the SSSC was shutdown and the line power returned to 740 MW. The horizontal axis is time. The regulation of the real power flow in the line is achieved by the SSSC by constantly adjusting its voltage injection magnitude as shown in Figure 8.25. This implies that due to system condition changes the line current magnitude is regulated by the SSSC to keep the real power flow

constant on the line. The horizontal axis on the figure is time. This result validates the automatic power flow control mode for the SSSC.

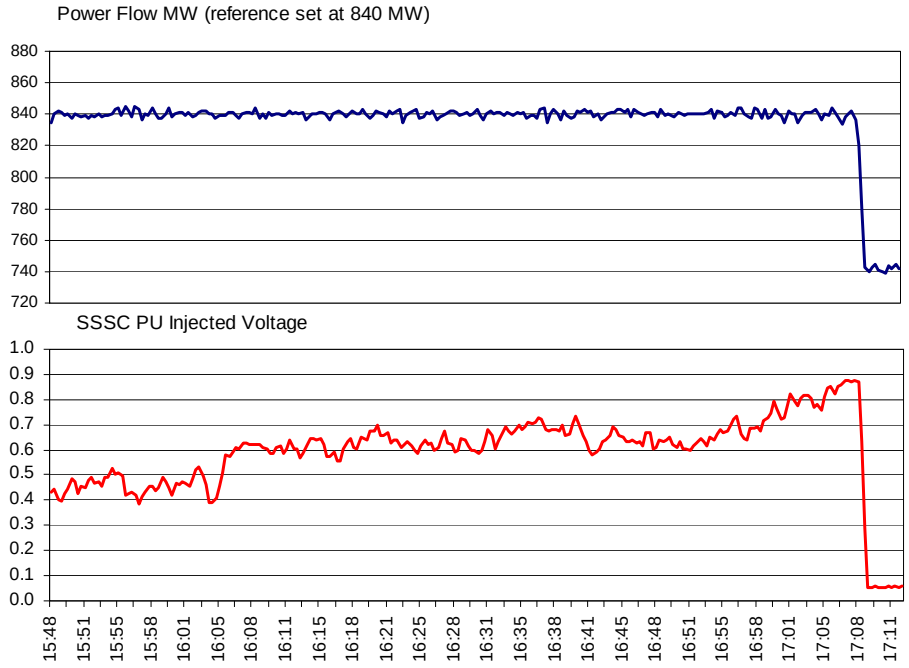


Figure 8.25 SSSC 2 in power flow control (set at 840 MW)

(c) SSSC – Dynamic System Testing

The dynamic characteristics of the SSSC were tested in both "open-loop" voltage injection mode and "closed-loop" power flow control modes. All tests were performed under normal system conditions. The effect of the step changes on the Coopers Corners (UCC) line are summarized in Table 8.9. The effect of the step changes on the New Scotland (UNS) line are summarized in Table 8.10. The ramp rate refers to maximum allowed rate of change of the injected voltage V_{inj} as a ramp. The ramp rate is important since a fast change of injected voltage may saturate the series transformer. Tables 8.9 and 8.10 show the step change in injected voltage and the resulting change in real and reactive power in the line. Note that with the SSSC voltage injection, the reactive power in the line is uncontrolled.

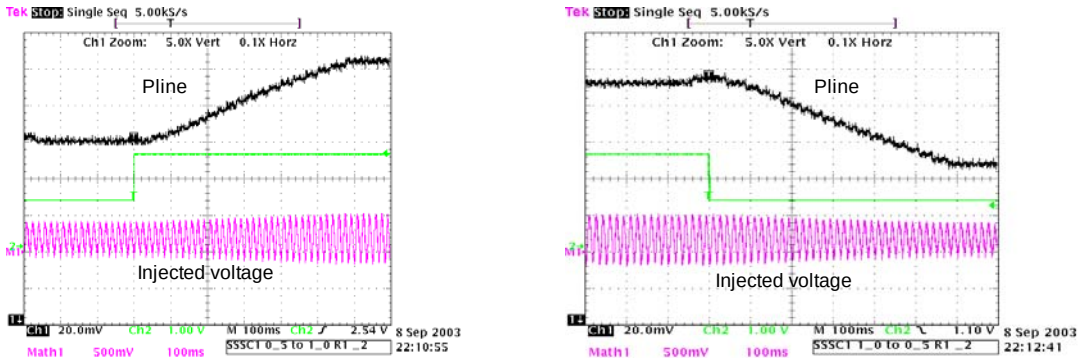
Table 8.9 SSSC 1 step response, voltage injection mode

Ramp Rate	Vq Reference Change	Δ MW	Δ MVAR
1	1.00 pu to 0.50 pu	–31	–10
1	0.00 pu to –0.50 pu	–30	–10
1	–1.00 pu to –0.50 pu	+36	+12
1	–0.50 pu to –1.00 pu	–33	–11
1	–0.50 pu to 0.50 pu	+62	+20
1	0.75 pu to –0.75 pu	–86	–24
1	–1.00 pu to 1.00 pu	+126	+38
1	1.00 pu to –1.00 pu	–123	–38

Table 8.10 SSSC 2 step response, voltage injection mode

Ramp Rate	Vq Reference Change									Δ MW	Δ MVAR
1	0.00	pu	to	0.50	pu					+66	16
1	0.50	pu	to	1.00	pu					+54	14
1	1.00	pu	to	0.50	pu					–55	–15
1	0.50	pu	to	0.00	pu					–52	–12
1	0.00	pu	to	–0.50	pu					–58	–11
1	–0.50	pu	to	–1.00	pu					–58	–11
1	–1.00	pu	to	–0.50	pu					+58	+10
1	–0.50	pu	to	0.00	pu					+54	+12

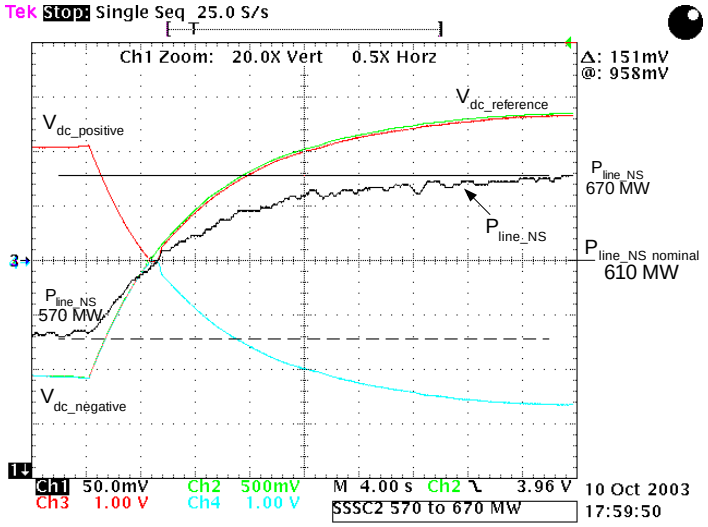
Figure 8.26 shows the dynamic response of SSSC 1 on the Coopers Corners (UCC) line for a voltage injection control mode reference of 0.5 pu to 1.0 pu (left graph) and 1.0 pu to 0.5 pu (right graph). The increase and decrease in the Phase A injected voltage is shown. Here the voltage injection ramp rate was set to 1. At this ramp rate a 0.5 pu injected voltage step change resulting in 30 MW of real power flow change takes around 500-600 ms.



Ch1: Pline MW (15 MW/div) Ch2: Reference change (trigger), Ch3: Injected Voltage

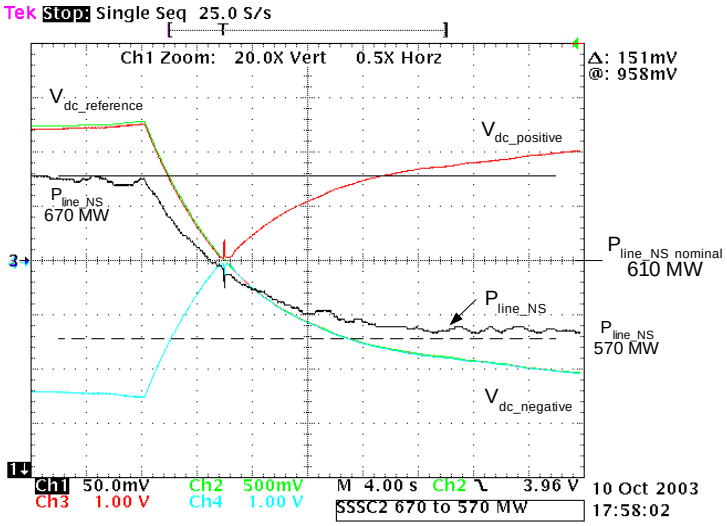
Figure 8.26 SSSC 1 voltage step change from 0.5 pu to 1.0 pu and from 1.0pu to 0.5pu

Figure 8.27 illustrates the SSSC step response of 100 MW in power flow control mode on the New Scotland (UNS) line. Here the DC bus voltage is displayed and is proportional to the injected voltage. For this step change the injected voltage transitions from negative to positive so the SSSC must control the DC bus voltage down to zero, then ramp it back up. A similar result is shown in the Figure 8.28 for a decrease in the power flow reference.



Ch1 : Pline MW (35 MW/div), Ch2: Reference change (trigger), Ch3 : Neg DC bus, Ch4: Pos DC bus (5V = 1 pu = 6 kV)

Figure 8.27 SSSC 2 step change in power flow control from 570 MW to 670 MW



Ch1 : Pline MW (35 MW/div), Ch2: Reference change (trigger),
Ch3 : Neg DC bus, Ch4: Pos DC bus (5V = 1 pu = 6 kV)

Figure 8.28 SSSC 2 step change in power flow control from 670 MW to 570 MW

(d) Dual SSSC (SSSC1 on UCC and SSSC2 on UNS line) Testing

This test demonstrated the capability of the dual SSSC (configuration 6 as shown in Figure 8.19), i.e., SSSC1 on the UCC line and SSSC2 on UNS line simultaneously. Although each SSSC operates independently, there is an interaction between the Coopers Corners (UCC) line and New Scotland (UNS) line. An increase in real power flow in one line results in a slight decrease in real power flow on the other line. The dual SSSC allows one line to operate at full positive voltage injection with the other line at full negative voltage injection. Table 8.11 shows the change in real power flow for each line at different SSSC operating points.

Table 8.11 Dual SSSC operating points - SSSC1 on UCC & SSSC2 on UNS lines

Time	Pline 1 (MW)	SSSC 1 Inj V Ref	Pline 2 (MW)	SSSC 2 Inj V Ref
18:27:31	460	1.0	718	1.0
18:28:13	398	0.0	726	1.0
18:28:52	338	-1.0	739	1.0
18:29:36	356	-1.0	642	0.0
18:30:09	366	-1.0	530	-1.0
18:31:10	428	0.0	519	-1.0
18:31:47	413	0.0	622	0.0
18:36:38	499	1.0	530	-1.0
18:37:20	424	0.0	640	0.0

In the dual SSSC configuration, both SSSCs were operated in voltage injection control mode and power flow mode. It was verified that there is no control interactions between SSSC1 and SSSC2 in both voltage injection control mode and power flow control mode.

8.2.3.3 Operational experience

CSC Description

The New York Power Authority (NYPS) is a generation and transmission utility and is the largest state-owned power organization in the United States. It provides about 25% of the total New York State load, operating 18 generating facilities and more than 1,400 circuit-miles of transmission lines. Recently, NYPA has installed a ±200 MVA Convertible Static Compensator (CSC) at the Marcy 345 kV substation. The CSC installation has been done in two phases; Phase I was commissioned in February 2001 and placed 345 kV ±200 MVAr STATCOM in service. The STATCOM regulates voltage at the Marcy bus. The second and final phase was finished in July 2004 and commissioned the so-called series and combined modes of the CSC, namely, SSSC, UPFC and IPFC. With the second phase included, the CSC has capability to regulate bus voltage and control real and reactive power flows on two transmission lines leading from Marcy substation to New Scotland (UNS-18 line) and Coopers Corners (UCC-41 line) substations.

A simplified one-line diagram of the New York transmission system is shown in Figure 8.29. It should be noted that low-cost hydro-generation is located in the northern and western parts of the NY State whereas major loads and high-cost generation are in the south east, in and around New York City. The Total East and particularly Central East interface, made of seven transmission lines ranging in voltage from 115 kV to 345 kV, are voltage-constrained to any further increase in power transfer over 6150 MW and 2880 MW, respectively . Prior to the CSC installation, two major studies were performed by NYPA to identify the NY state power system constraints and investigate benefits of using a FACTS Controller to alleviate those constraints.

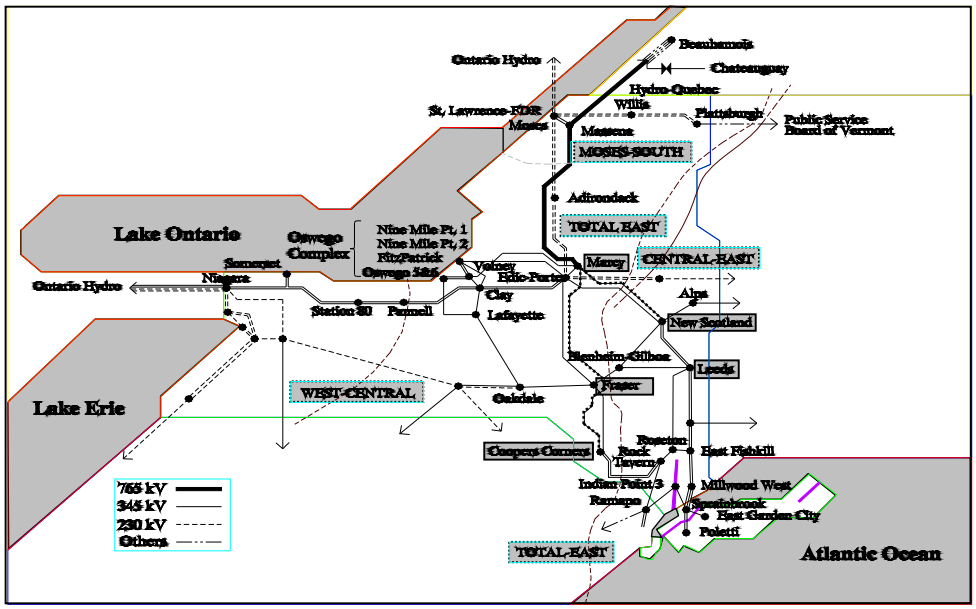


Figure 8.29 One-Line Diagram of New York State Power System

A simplified representation of the CSC scheme is shown in Fig. 8.30. The CSC employs two identical voltage-sourced GTO-based converters that can be, through disconnect switches, connected in a number of different configurations. The converters are three-level voltage-sourced converters structured to generate a three phase 48-pulse sinusoidal voltage waveform at the output terminals. The arrangement is flexible such that the converters can be connected either in shunt with the Marcy bus or in series with

the UCC-41 and UNS-18 transmission lines, respectively. The DC buses of the two converters may also be joined allowing the converters to exchange real power.

By selecting the appropriate switch positions the following configurations of the equipment are possible:

STATCOM (±100 MVAr or ±200 MVAr)
SSSC (±100 MVAr on one or ±200 MVAr both lines)
Independent STATCOM and SSSC (±100 MVA each)
UPFC (±200 MVA; switch between DC capacitors closed)
IPFC (±200 MVA; switch between DC capacitors closed)

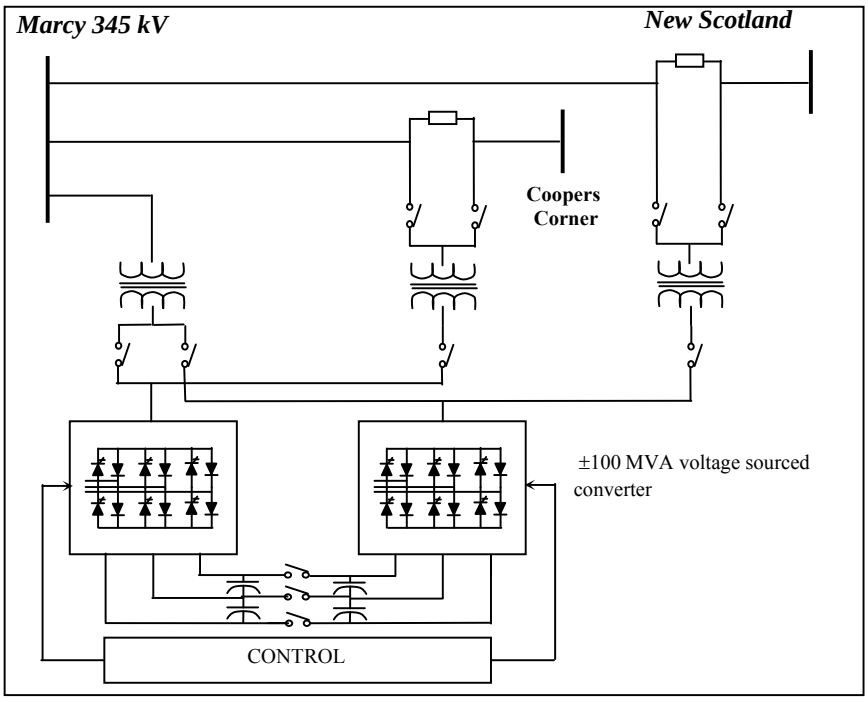


Figure 8.30 A Simplified Representation of the CSC Scheme

CSC Two-SSSC Operation

Once a year, the CSC equipment is exercised in all configurations and control modes to check the operability of the equipment and to allow the system operators time in front of the control console to refresh their skills in operating the device. In addition to this exercise, there is the CSC Operator Training Simulator (OTS) customized for NYPA to facilitate the training of power system operators and planning engineers on the functions of the device. The OTS is envisioned as a learning tool to test "what if scenarios" for advanced transmission technologies, as well as for every day use of the operators, and realistically simulates the CSC controller configurations, control modes, control setpoints, and dispatch variables.

Out of the possible eleven CSC configurations, most of the time the CSC is operated as a ±200 MVAr STATCOM in VAR reserve control mode. The STATCOM's output, when in this mode, is limited to the operating points within the pre-set inductive and capacitive boundaries. This control allows STATCOM to respond to the system voltage changes within the boundaries and still have enough VAR reserve to respond to a possible system contingency.

The two ±100 MVAr SSSC configuration, in addition to the described ±200 MVAr STATCOM configuration, was recognized as one of the preferred configurations in which to operate the CSC. There are two possible control modes for the SSSC: constant voltage insertion and automatic real power flow control mode. In the constant voltage insertion mode, the desired voltage is inserted in series with the transmission line to increase or decrease real power flow depending on the polarity of the inserted voltage. In the automatic power flow mode, the real power flow on the transmission line is adjusted to match the desired real power flow. It should be noted though, that the automatic power flow mode is not a preferred operating mode. It is used only to obtain the desired real power flow on the line, and the SSSC is switched back to the constant inserted voltage that matches the desired real power flow.

A good example of the dual ±100 MVAr SSSC operation was the system condition that occurred on August 30, 2004. Real power flows of 1437 MW and 957 MW were observed on Roseton to East Fish Kill (RFK) and Rock Tavern to Roseton (RT-R) transmission lines, respectively (see Figure 8.31). The power flow studies indicated that a loss of the RT-R line would cause 53% of real power to shift to the RFK line. This shift increases in post-contingency the real power flow on the RFK line to 1944 MW, 32 MW over the thermal line limit. To avoid a possibility of reaching the line thermal limit, the CSC was switched to dual ±200 MVAr SSSC configuration to control the real power flow on Marcy-Coopers Corner and Marcy-New Scotland transmission lines, and consequently on the two transmission lines under consideration. The real power flow on UNS-18 line was boosted by 110 MW, while the real power flow on the UCC-41 line was decreased by 65 MW. This had, in turn, reduced the real power flow in the RFK and RT-R lines by 35 MW and 32 MW, respectively. The power flow on the RFK line was 1405 MW, while the real power flow on the RT-R line was 935 MW. The power flow studies showed that in the new potential post-contingency (loss of the RT-R line), the real power flow on the RFK line would be 1900 MW, 12 MW below the 1912 MW of thermal limit.

The real power flows on the affected transmission lines is shown in Figure 8.32, as captured by NYPA's EMS.

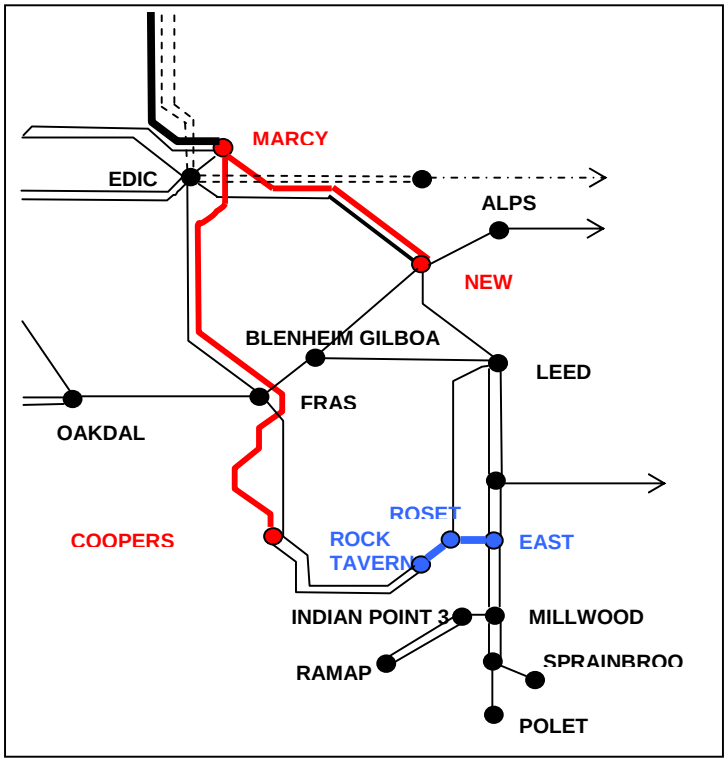


Figure 8.31 A Simplified Schematic of a portion of the NY State Power System

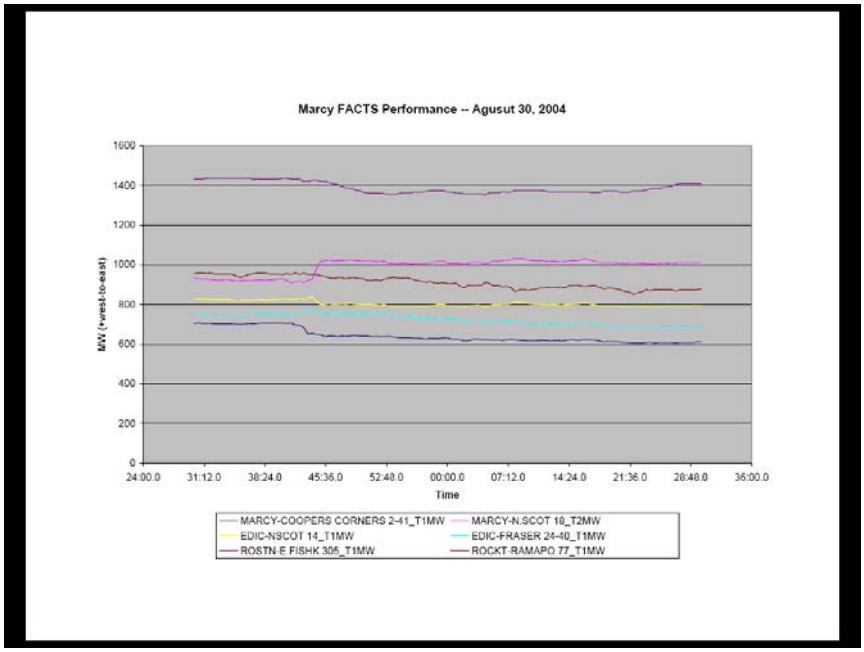


Figure 8.32 Plot of the Real Power Flows on the Affected Lines

Summary

In this section the application of the CSC Two-SSSC mode of operation to alleviate a potential lsystem emergency is described. Although the CSC normally operates in the STATCOM mode to provide voltage support due to system needs, the series mode can be effective in the control of power on two lines exiting Marcy substation. In this example, even though the lines facing the potential emergency were further away from the immediate vicinity of the CSC, the two-SSSC mode in conjunction with various other actions taken by the system operator successfully helped to avoid a potential line overload scenario.

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PART IV
FUTURE OUTLOOK

CHAPTER 9. TRANSFORMERLESS SSSC

Future trends in developing Static Series Synchronous Compensator (SSSC) are driven by the following characteristic objectives for the design of the power converter system to provide the necessary platform for high operating performance, maximum application flexibility and low cost:

(1) Sinusoidal output (no or minimum filtering requirement)
(2) Single coupling transformer with established ("standard") winding arrangements and the minimum use of auxiliary magnetic components.
(3) DC bus structure suitable to interconnect compatible converters in a back-to-back configuration. (Preferred arrangement is a single +/– DC bus to accommodate any supplies or energy storage devices with compatible voltage level.)
(4) Modular system using basic building block converters of appropriate ratings with a structural infrastructure to provide partial availability, and expandability both in rating and functional flexibility.
(5) Reasonable operating losses.

9.1 MERITS JUSTIFYING DEVELOPMENT OF TRANSFORMER-LESS SSSC

The operating and performance benefits of SSSC are well recognized and documented in the previous section of this report. Indeed, their unique operating characteristics and functional flexibility are not attainable by other type of transmission controllers. However, it appears that their cost and some of the operating problems, apparently related to the current converter designs based on the then available power semiconductor switching devices with gate turn off capability, e.g. GTOs, IGBTs, IGCT, etc. and the needed magnetic interface components, hinders their wider application. The future trends is, therefore, to develop a new, simplified converter structure using new, evolving advanced power semiconductor switches, which can be directly connected in series with the line without a coupling transformer. The converter structure envisioned would, of course, be suitable for use with a coupling transformer of *standard design*, if the application, or user preference, would call for it. Apart from eliminating the need for a series coupling transformer, the development should also aim for higher reliability, and the full MVA utilization of the converter, through simplified converter structure and rigorous protection algorithms afforded by the greatly improved characteristics of emerging power semiconductor switching devices, e.g. Emitter Turn Off (ETO) thyristor, to meet cost and availability requirements of utility applications.

An elementary converter arrangement connected directly in series with the line to operate as a transformer-less SSSC is shown is Figure 9.1. There is a single-phase "H-bridge", operating self-sufficiently with its own DC storage capacitor, for each line phase. This scheme is inherently suitable to compensate lines even with large phase-current unbalance, a condition that frequently exists in practical transmission systems. The controlled semiconductor valves, represented by a single GTO type device in Figure 9.1, would in practice be comprised of suitable gate turn-off power semiconductors (IGCT or IGBT or ETO, etc.) in series connection to match the maximum voltage requirement of the compensation. Two or more such valves could also be operated in an effective parallel connection to provide the necessary current rating and, with the use appropriate harmonic cancellation techniques, also to reduce harmonic distortion.

The transmission controller configurations outlined above in their conceptual forms not only provide much greater versatility and operating performance than the presently used configurations, but, with the elimination of the series coupling transformer, they also would eliminate the root cause for the most severe control and the consequent operation problems, and, at the same time, would reduce significantly the equipment cost.

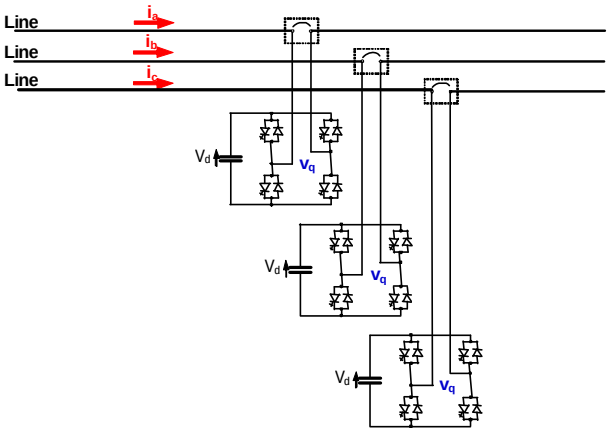

Figure 9.1 Basic transformer-less SSSC scheme using "H-bridge" converters

The transformer-less converter structure would probably have an even greater cost benefit for distribution system applications, where the voltage levels would not require any special insulation arrangement for directly connected converters. Cost-effective, directly-connected distribution Static Synchronous Compensators (STATCOMs) and Dynamic Voltage Restorers (DVRs), with much increased speed of response and greatly reduced operating problems, which could be employed in demanding power quality applications to solve voltage sag, flicker, and harmonic problems in addition to providing voltage support, voltage regulation, and power flow control.

It is realized that the degree of success the above converter structures potentially offer will depend on innovative power circuit configurations and, in particular, in the waveform synthesis techniques applied for the operation of the valves. However, the recent and ongoing innovations in power semiconductor technology, resulting in greatly improved switching characteristics at high power ratings, provide a creditable basis for the optimism that the technical means to meet the challenges are becoming available.

9.2 NEW CONVERTER PLATFORM

Historical trends in the preceding development of converter technology for low power applications, and the recent *impressive progress of power semiconductor technology*, suggest that the *new generation of power converter technology should employ the technique of pulse-width-modulation (PWM) as the basic method for output waveform synthesis together with the use of modular circuit structures to neutralize the resulting high frequency carrier component in the output and thereby eliminate or significantly reduce filtering requirements.* Therefore, ***a carrier-neutralized PWM converter platform could be adopted for future generation of converter-based transmission Controller.***

Figure 9.2 shows a possible converter platform for transformer-less SSSC, where each phase is structured using four building blocks, modules, using Carrier-Neutralized PWM switching.

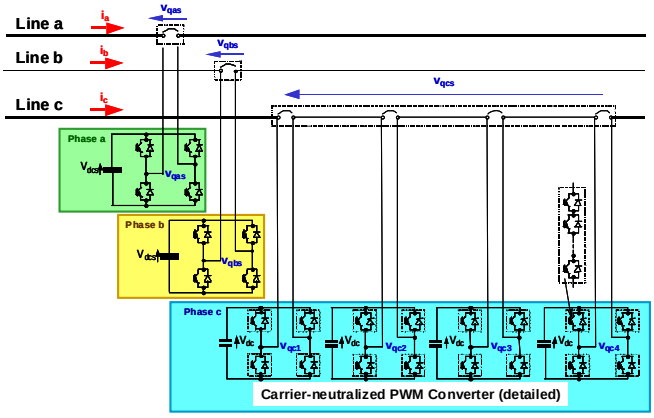

Figure 9.2 Three-phase Transformerless SSSC

9.2.1 Carrier Neutralized PWM

The implementation of carrier-neutralization inherently *requires a modular converter structure* that is necessary to achieve the desired flexibility, expandability, and application tailored partial availability, together with minimum production cost.

Carrier-neutralization, based on the summation of the successive phase-shifted carrier components and in-phase fundamentals, eliminates or reduces filtering requirements and allows *full rating utilization* of the converter. Figure 9.3 illustrates the principle of Carrier-Neutralized PWM, where four modules are using coordinated PWM in such a way that the sum of the output voltage has a high-pulse sinusoidal wave form with no filtering requirement. A loss of one module could be compensated through a change in the switching frequencies of the remaining modules. Similarly, adding another module to increase the capacity of the SSSC could be accommodated by adjusting the switching frequency.

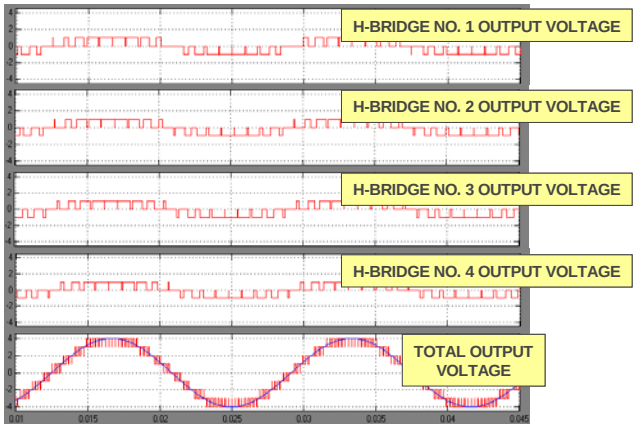

Figure 9.3 Building a high-pulse sinusoidal output voltage from four modues

9.2.2 SSSC Platform Structure

The transformerless SSSC requires the power electronic converters to be placed on high potential. In order to reduce cost and increase robustness and reliability a similar platform arrangement as for

transmission thyristor controlled series capacitors (TCSC) is suggested. The platform, isolated to ground, provides a new potential surface that provides for corona protection and electrical field shielding. In the TCSC system already solutions for transferring cooling media between high potential and ground and systems for providing auxiliary power on the platform are developed and proven. Figure 9.4 shows a TCSC installation and it is suggested a SSSC use the same type of platform arrangement.

Figure 9.4 A TCSC Platform

The advantages of using similar, field proven, solutions are that the development costs and time to market is reduced. Further, the risk of initial problems due to failures of auxiliary systems is reduced. Systems already developed and proven are:

- Cooling media distribution between low and high potential
- Environmental control of converter housing
- Isolated auxiliary power supply systems
- Fault bypass systems

9.3 POWER SEMICONDUCTOR TECHNOLOGY DEVELOPMENTS

Power semiconductors are the most critical elements influencing the cost, reliability and performance of converter-based transmission controllers. The key parameters of power semiconductors and their main effects on converter design are listed below.

Steady-state parameters:

- *Blocking voltage and R.M.S /average current* basically determine the number of devices the converter will need for a given MVA rating. The number of devices largely determine the cost because the number of all converter auxiliary components (heat sink, gating circuit, snubber, communication fiber optics, mechanical hardware) and assembly labor change in proportion with the number of power semiconductors.
- *Forward voltage drop* is an important parameter that determines largely the operating losses, cooling requirements, and influences the physical size of the device as well as that of the whole equipment.
- *Surge current* capability may be important to implement low cost protection schemes, particularly for converters operated in series with the line.

Switching characteristics:

- *Peak current turn-off* is the maximum *instantaneous* current the device can turn off without failure. This parameter largely determines the de-rating required to accommodate harmonic ripple

current and the safety margins needed for over current protection; thereby, it is a critical factor for the high utilization of the converter MVA rating.

- *Turn-off time delay* is the maximum delay time from the application of the turn-off signal to the completion of turn-off process. This parameter is crucial for reliable over current protection without large safety margins and, thereby, another significant factor to achieve high converter utilization (and low equipment cost).
- *Switching speed and losses* are the maximum time required for the device to transit from ON state to OFF state, and vice versa, and the corresponding internal losses in the device. These determine the applicable range of switching frequency and the corresponding operating losses and cooling requirements. The capability to operate the devices at relatively high switching frequencies is important for the implementation of pulse-width-modulation techniques for output waveform synthesis that requires small output filters (inductance and capacitance), and thereby allows the high utilization of converter MVA. It is also important for providing relatively wide operating frequency band for the converter necessary to sustain *reliable* operation, with rigorous current limitation, under abnormal operating condition causing transformer saturation.

9.4 EMERGING POWER SEMICONDUCTOR SWITCHES

There has been important progress made in power semiconductor technology with focus on the improvement of switching speed and characteristics. The following is recently introduced and expected future power semiconductor switches, which have considerable potential for improved converter designs of lower cost and higher reliability:

Integrated Gate Commutated Thyristor (IGCT or GCT). The Integrated Gate Commutated Thyristor (IGCT) is a press-pack device. The IGCT is pressed with a relatively high force onto heat-sinks which also serve as electrical contacts to the power terminals. The IGCT's turn-on/off control unit is an integral element of the component. It only requires an external power supply and its control functions are conveniently accessed through optical fiber connections. It is a recent derivative of the Gate Turn-Off (GTO) thyristor. It offers significant improvements over the latter in the important areas of:

- Turn-off time delay: reduced from about 22 μs to about 1 μs
- Reduced forward voltage drop
- Increased peak turn-off current
- Increased switching speed

The device's control power consumption typically ranges from 10 - 100 W. The IGCT is optimized for low conduction losses. Its typical turn-on/off switching frequency is in the range of 500 Hz. However, in contrast to the GTO, the upper switching frequency is only limited by operating thermal losses and the system's ability to remove this heat. This feature, in conjunction with the device's fast transition between on and off state, enables short on-off pulse bursts with switching frequencies of up to 40 kHz. IGCTs require a turn-on protective network (in essence an inductor) to limit the rate of current rise. However, in contrast to the GTO, the turn-off protection network is optional. It can be omitted at the price of a somewhat reduced turn-off current capability.

Emitter Turn-off (ETO) Thyristor. The ETO is another new derivative of the GTO, focusing on drastically reduced gate drive requirements and, also, increased switching speed.

- Optical control interface
- Turn-off time delay: reduced from about 22 μs to about 1 μs
- Forward voltage drop: 2 V
- Increased switching speed and capable of > 1 kHz operation

Super-GTO (S-GTO). The S-GTO is also a GTO type device with dramatically finer cell structure (160,000 vs. 50 cells/cm^2) than the conventional GTO. This is expected to result in considerable improvements over the conventional GTO in:

- Turn-off time delay (1 μs vs. 22 μs)
- Switching speed (3 times)
- Current density and turn-off current density (2 times and 10 times)
- Forward voltage drop (0.7 times)

Insulated Gate Bipolar Transistor (IGBT). The Insulated Gate Bipolar Transistor (IGBT) is the youngest member of the high voltage switch family. Current flow through the device is conveniently controlled through a 15V high-impedance voltage source, thus enabling control of high currents with very low control power. IGBTs are available both as press-packs and modules. The high power IGBT press-packs and diodes are placed in an advanced modular housing which guarantees uniform chip pressure even in multiple-device stacks. Although the most common package for IGBTs is the isolated module, for applications requiring series connection, non-isolated, pressure-assembled devices (press-packs) are preferred for many reasons, not least of which is their ability to fail *short* as opposed to *open* circuit. Higher voltages are in development.

IGBT is, in contrast to the previous devices, a *non-latching* transistor rather than a thyristor. In the last few years it has been breaking all previously believed limits in voltage rating and power handling capability. Its development has been fueled by many industrial and traction applications as well as the potential of converter-based technology for dc transmission. Although high power IGBTs have been proven in transmission applications (shunt compensation and DC transmission), there are still on-going intense development efforts to increase the switching speed and to reduce the forward voltage drop of the presently available devices. Except for forward voltage drop and corresponding *losses*, the capabilities of present IGBTs are generally comparable to those of advanced GTO type devices, and superior to most of them in the area of gate drive requirements. Moreover, IGBTs have a major, *inherent advantage* over the GTO type devices in that they have a transistor like characteristic of not latching into a conducting state, and thus their internal turn off process is fully controllable from the gate. The transistor-like characteristic can be utilized effectively to minimize the snubber requirements and the physical size of high voltage valves, as well as to provide sustained converter operation and tight protection under abnormal transmission system conditions.

Injection Enhanced Gate Transistor (IEGT). This is substantially an IGBT which was subjected to carrier injection enhancement to improve some of the operating characteristics, particularly the forward voltage drop.

Silicon Carbide Devices. It has been recognized for a long time that the characteristics of semiconductor devices are heavily dependent on the material used for their fabrication. All of the present power semiconductors use silicon. However, on-going research has concluded that *silicon carbide* is a superior material for semiconductors with a potential to drastically improve (several times increase or decrease) presently attainable

- Switching speed
- Current density
- Operating junction temperature
- Forward voltage drop

The forecasted device improvements would have a dramatic impact on the design of converter-based controllers, *resulting in significant size and cost reduction and reliability improvement*. The silicon carbide devices are equally advantageous for other than utility application (i.e., defense and industrial) and therefore intense development is going on.

Primarily due to their improved switching characteristics, the recently introduced new power semiconductor switches, can already facilitate new power circuit approaches, control and protection

algorithms to improve reliability and reduce cost of converter based transmission controllers. Historical technology trend clearly indicates that continuous future improvements can be expected, ultimately with the appearance of revolutionary new devices based on silicon carbide and other new materials. The recent power semiconductor technology developments strongly suggest that the new converter platform for transmission applications should fully *exploit the considerable improvements in switching speed and current turn-off capability* of new switches in the design of simpler power circuit structures, higher utilization of power semiconductors, and more rigorously executed protection strategies in order to achieve increased equipment reliability and availability, and lower cost.

9.5 STATE OF THE ART OF POWER SEMICONDUCTOR SWITCHES

Standard thyristors are still the most important controllable switch for very high power applications. Recently manufacturers have increased the ratings and performance of high power thyristor switches with bi-direction thyristor wafers and optically laser triggered thyristors. Manufacturers concluded that the thyristor is still the workhorse switch for high power electronics [9.0,9.0].

Thyristors however cannot be used for modern voltage sourced converter topologies since the device can only be turned on by means of the gate and not turned off under current carrying conditions. For medium to high power applications fully controlled switches include the Gate Turn-off Thyristor (GTO), High-Voltage Insulated Gate Bipolar Transistor (HVIGBT), and Integrated Gate Commutated Thyristor (IGCT). The IGCT brings together a versatile new power handling switch, the GCT, (Gate Commutated Thyristor) and the switch control circuitry in an integrated package. Research is still conducted on a high power MOS controlled thyristor technology (MTO and MCT). The semiconductor technology of modern power semiconductors is studied extensively in several textbooks [9.3].

9.5.1 Voltage and current rating

Device cells for high power are usually single crystal silicon wafers, 75-125 mm in diameter, and pushing toward 150 mm in diameter. The same diameter device can be made for higher voltage with lower current and vice versa. Potentially, silicon crystal has a very high voltage breakdown strength of 200 kV/cm and a resistivity somewhere in-between that of metals and insulators.

A larger diameter naturally means higher current carrying capability. A 125 mm device may have a current-carrying capability of 3000-4000 amperes and a voltage-withstand capability in the range of 6000-10,000 Volts.

With higher device ratings, the total number of devices as well as the cost of all the surrounding components decreases. The highest blocking capability along with other desirable characteristics is somewhere in the range of 8-10 kV for thyristors and 5-8 kV for IGBTs. In a circuit, after making various allowances for over voltages and redundancy, the useable device voltage will be about half the blocking voltage capability. Often, it will be necessary to connect devices in series for high-voltage valves. Ensuring equal sharing of voltage during turn-on, turn-off, and dynamic voltage transients, becomes a major exercise for a valve designer in considering trade-offs. One of the techniques used is matching of devices, especially the switching characteristics of a specific match of devices.

Apart from the voltage withstand and the current-carrying capabilities, there are many characteristics that are important to the devices. The most important among these are:

- forward-drop and consequent losses during full conducting state
- production costs and yield of semiconductor devices
- speed of switching
- switching losses
- gate-driver power.

Apart from the trade-off between voltage and current capability, other trade-off parameters include:

- power requirement for the gate
- *di/dt* capability
- *dv/dt* capability
- turn-on time and turn-off time
- turn-on time and turn-off capability (so-called Safe Operating Area (SOA))
- uniformity of characteristics
- quality of starting silicon wafers
- class of clean environment for manufacturing of devices

Types and ratings of power semiconductor switches

The state of the art of the power semiconductors essentially influenced the rating and topologies of high power converters. The thyristor technology has achieved ratings of 9 kV, 4000 A (36 MW peak switching power per device). The gate turn-off technology GTO has achieved 4.5 kV, 4000 A (18 MW peak switching per device). Similar parameters are achieved with the IGCT and ETO thyristors. The IGBT technology is approaching the power level of the GTOs with the 6.2 kV and 2000 A. Figure 9.5 schematically compares the controllable power of a single power device from different types.

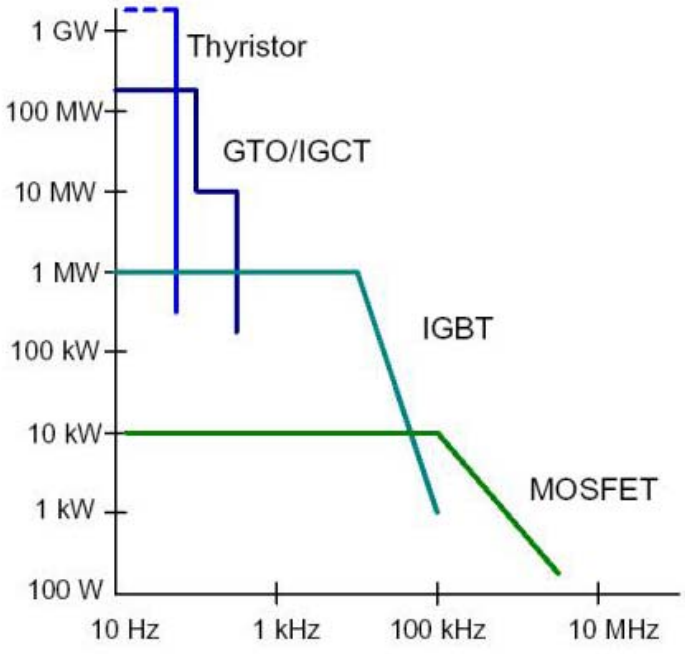

Figure 9.5 Comparison of controllable power of different power electronic devices

These different devices are depicted in Figures 9.6 to 9.11, and described below.

Figure 9.6: Traditional High Voltage Thyristor

Figure 9.7 Bi-directional Thyristor (BCT) from ABB

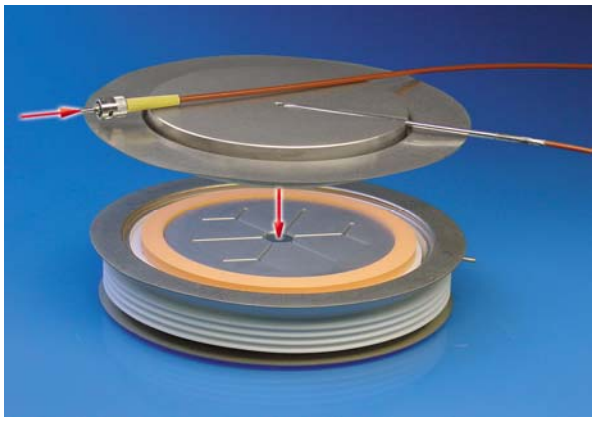

Figure 9.8: Laser Triggered Thyristor (LTT) from Siemens

Figure 9.9: Gate Turn-off Thyristor (GTO)

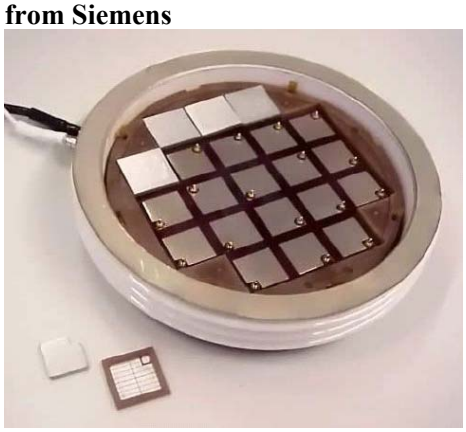

Figure 9.10: Press-pack High Voltage IGBT

Figure 9.11: IGCT Device from ABB

Table 9.1 Comparison of rating of most high power semi-conductor switches.

Device	V_{max} (V)	I_{max} (A)	t_{off} (μs)	f_{max} (Hz)	On-State (V)	Gate Drive	Gate and Snubber
Thyristor	9000	4000	50	50	4	Current	Low
LTT	7500	3500	35	50	4	Light	Very low
GTO	4500	4000	10	500	4,5	Current	Very high
IGCT	4500	4000	5	1000	2,5	Voltage	Low (Integrated)
IGBT	5200	2000	2	1 - 5	4,5	Voltage	Very low
MOSFET	1000	100	0,3	20 - 200	0,5 - 5 V	Voltage	Very low

9.5.2 Recent developments of thyristor devices

As discussed above, thyristors are still the most important controllable device for high power applications. In addition, in the high power thyristor technology, several breakthroughs have been achieved. The most relevant for this study was the development of a commercial available high power back-to-back thyristor pair for SVC and TCSC applications by ABB and the laser light triggered thyristors now standard for nearly all Siemens SVCs and HVDCs.

The bi-directional thyristor (BCT) technology of ABB is based on an integrated waver with two thyristor structures. The electrical behaviour of a BCT corresponds to that of two anti-parallel thyristors (e.g. of approximately 27 cm^2 area each for the 96mm wafer diameter) integrated onto one silicon slice, as shown in Figure 9.6. Each thyristor-half performs like the corresponding full-wafer thyristor in respect to its static and dynamic properties. The advantage of such a device is less packaging and a compact valve design for phase-controlled applications, i.e. SVCs and TCSCs.

Siemens has its own development on thyristors. They commercialised a standard 7,5 kV, 3500 A rms thyristor fully triggered by laser light (LTT) as shown in Figure 9.6. This implies major savings on insulated drive, protection and status measuring electronics. A 40 mW laser pulse is used to trigger the LTT with an equivalent of 50 A peak gate current. This high gate pulse results in better di/dt capabilities and gives a better margin for dynamic phenomena.

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