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Components Testing of

VSC System for HVDC Applications

Working Group
B4.48

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FOREWORD

INTRODUCTION

In 1997, a Voltage-Sourced Converter (VSC) based HVDC demonstration project rated at 3MW and ±10kV was put into operation in Hellsjön, Sweden. Up to early 2010, there have been 10 commercial VSC-HVDC projects in service, among which the two largest projects are the 400MW/±150kV offshore wind farm interconnection project Borkum1 in Germany and the 400MW/±200kV Transbay Cable project in USA. The operating experience to date indicates that VSC-HVDC systems work effectively in grid interconnections, wind farm integration, drilling platform or passive system power supply applications.

Technical advantages of the novel dc transmission technique based on VSC and semiconductors with turn-off capability have been verified by successful operation of VSC transmission systems. The performance advantages：

- Independent decoupled control of active and reactive power without the need for additional reactive power compensation equipment or telecommunication links between the converter stations.
- Power supply for weak or even passive networks without a need for ac network to provide commutating voltage.
- Simultaneous emergent support of both active and reactive power to the ac power systems, which is great for enhancing system reliability and improving power quality.
- Compact converter station and environmentally-friendly design.

The aforementioned features promote the demand for VSC-HVDC project application in HVDC field and it can be foreseen that in the future more and more VSC transmission project will be put into operation.

The progress in VSC technology and its technical benefits lead to an increasing demand for this converter type for HVDC applications. Consequently the need for understandable test philosophies, useful test procedures and reasonable acceptance criteria for VSC technology in HVDC applications arose.

Therefore, working group B4.48 committed itself to evaluate testing aspects of VSC system components. The working group not only focused on VSC valves but also on power stack components like phase/valve reactors and VSC dc capacitors. Different feasible topologies like two-level and one specific multi-level topology have been considered in the work as well as the different types of schemes (back to back configuration, cable transmission etc.). The following issues were the group's contributions:

- Defined components and subsystems to be tested.
- Defined operational and fault scenarios to be considered for the tests.
- The proposed tests are justified by relevant references to stresses at operation and at faults.

In order to establish adequate guide for operational tests, a representative procedure for determination of the operational losses of VSC system was developed.

The working group have made use of work developed within SC B4 (WG B4-37, VSC Transmission) and of

the principles in IEC 62501, and procedure described in IEC 61803.

GUIDE TO THE BROCHURE

In this report, the symbols and glossaries of VSC transmission system components, subsystems, operating modes, tests of the components and losses are defined; background knowledge of VSC transmission system structure and function of the components etc. are presented. In addition, operating states and fault modes which shall be considered are described; various stresses under steady state, disturbance and fault states are analyzed. Finally, test methods and procedures for the component tests as well as test data and criteria of successful tests are summarized.

The information presented in this document is aimed primarily at the following groups of people:

- The developers and designers of a VSC transmission scheme;
- The manufacturers of the components for the VSC transmission system;
- Transmission network owners/operators planning to build and maintain a VSC transmission scheme;
- Anyone who wants to know more about the performing and testing of VSC transmission systems and their components..

Some readers of the document have technical interests and some have non-technical interests. Therefore, the document has been structured such that different needs can be met by reading selected sections.

Readers without a particular interest in the technical details are expected to find the following chapters of great value: Chapter 1 Definitions, Chapter 2 Basic Configuration, Chapter 3 Function of the components and subsystems.

For readers with a good technical background, it may be advantageous to read chapters 4, chapter 5 and chapter 8 to obtain a deeper insight into VSC transmission operation.

Chapter 6 and 7 may be valuable for the manufacturers or the investors in a VSC transmission scheme.

OVERVIEW OF THE DOCUMENT

The report consists of 9 chapters and an Appendix.

Chapter 1 provides a list of definitions of symbols and terms related to VSC transmission scheme. An explanation for terms about power semiconductor, valve structure, and VSC transmission is given. The definitions of valve operating states, test types and power losses are covered. Those terms that are either identical to or obvious extensions of the IEC 60633, IEC60700-1, IEC61803 and CIGRE B4-37 Report terminology are not repeated.

Chapter 2 describes the general system configuration of VSC transmission and defines its components and sub-systems. Different converter topologies， neutral grounding arrangements, and different system configurations for various applications are presented.

Chapter 3 gives a brief overview of the function of different components and subsystems to be tested. The modulation strategies of different converter topologies are presented. Especially the functional structure of the valve is introduced.

Chapter 4 analyses the electric stresses of VSC valve and other important components under steady-state operation. Typical steady-state current and voltage waveforms of the valve are given, and the key factors of those stresses are analyzed. For the other key components, the focus is on special stresses in VSC transmission system.

Chapter 5 confirms the fault and disturbance modes which are mainly sorted into ac system faults, internal faults in VSC substation and dc transmission line and cable faults. The transient processes of these fault modes are presented and the electrical stresses of valves and other components are analyzed.

Chapter 6 checks the stresses of each component one by one, summarizes steady state stresses and transient stresses that need to be taken into consideration for the components testing, identifies the critical ones, and makes further analysis according to the test requirements. Specific component stresses and relevant testing requirements are outlined.

Chapter 7 discusses the components of VSC valve and other components' losses. The calculation methods and their limitation issues are also presented. And analysis on the factors that correlate with the losses is performed.

Chapter 8 creates principal test items for the components and specifies the purpose and objective of each test, and proposes safety margins for the tests. The fault scenarios to be considered within tests are also listed.

Chapter 9 is a brief conclusion.

Appendix illustrates the real voltage and current waveforms of different VSC topologies during continuous operation of the VSC converter.

WORKING GROUP MEMBERSHIP

As the convener of this Working Group, I have been fortunate to have the enthusiastic support of knowledgeable and hard working members. Each member has contributed many hours, both through the work in between and during each meeting. We began in Oct 2006, and have held a total of five meetings. I hope that all the members have enjoyed our friendship. Thanks to you all.

I also want to express my gratitude to 5 specialists, Mr. Grigory M. Tsfasman, Mr. Mohamed Rashwan, Mr. John Gleadow, Mr. Peter Lips and especially Mr. Stig Nilsson, for their valuable comments on perfecting the wording of the brochure and clarification of confusing problems.

The members of the working group were:

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ABBREVIATIONS

The following Abbreviations have been used in this Technical Brochure:

AC	Alternaing Current

DC	Direct Current
VSC	Voltage Sourced Converter
PWM	Pulse Width Modulation
RFI	Radio Frequency Interference
EMI	Electromagnetic Interference
THD	Total Harmonic Distortion
LTC	Load Tap Changer
LCC	Line Commutated Converter
SOA	Safe Operating Area
EMC	Electromagnetic Compatibility
SPT	Soft Punch Trough
IGBT	Insulated Gate Bipolar Transistor

Dr Guangfu Tang

Convenor WG B4-48

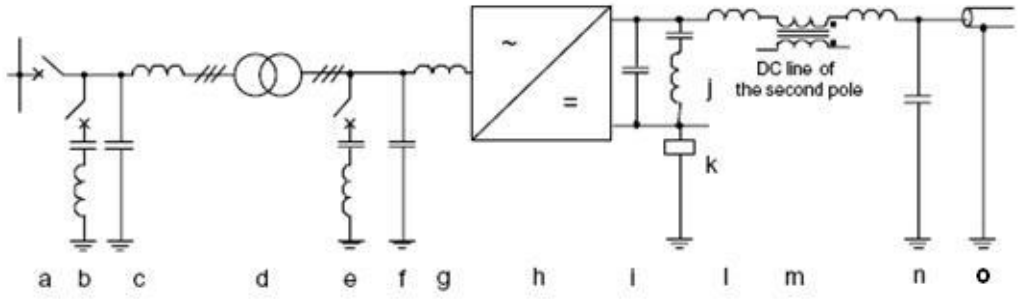
Oct 2009

1. DEFINITIONS

1.1 INTRODUCTION

This report uses the terminology established by IEC 60633, [1-1], IEC 62501, [1-2], IEC61803, [1-3] and CIGRE B4-37 Report, [1-4]. However, due to the differences in the scope of the work, the Working Group has felt it appropriate to define some new terms used in this report. Those terms that are either identical to or obvious extensions of the IEC 60633, IEC 62501, IEC61803 and CIGRE B4-37 Report terminology have not been defined.

To support the explanations, Figure 1.1 presents the basic diagram of a VSC system. Depending on the converter topology and the requirements in the project some components can be omitted or can differ.



a) VSC substation circuit breaker

b) system side harmonic filter

c) ac side power line carrier harmonics filter

d) interface transformer

e) valve side harmonic filter

f) ac side RFI filter

g) phase reactor

h) VSC unit

i) VSC dc capacitor

j) dc harmonic filter

k) neutral point grounding branch[1)]

l) dc reactor [2)]

m) common mode blocking reactor [2)]

n) dc side RFI filter [2)3)]

o)dc cable or overhead transmission line

1) The location of the neutral point grounding branch may be different depending on the design of the VSC unit.

2) Optional for dc side filtering.

3) Only required if power line carrier communication is used on the connected ac lines.

Figure 1.1 Basic diagram of a VSC system.

1.2 LIST OF LETTER SYMBOLS

U_{conv}	Line-to-line ac voltage of the converter unit(s), rms value, including harmonics.
I_{conv}	Alternating current of the converter unit(s), rms value, including harmonics.
U_L	Line-to-line ac voltage of the ac system, rms value, including harmonics.
I_L	Alternating current of the ac system, rms value, including harmonics.
U_d	dc voltage of the dc bus to ground of the VSC transmission system
I_d	dc current of the dc bus of the VSC transmission system

1.3 POWER SEMICONDUCTOR TERMS

There are several types of switched valve devices which can be used in voltage sourced converters (VSC) for HVDC and currently the IGBT is the major device used in such converters. The term IGBT is used throughout this report to refer to the switched valve device. However, the report is equally applicable to other types of devices with turn-off capability in most of the parts.

1.3.1 Switched Valve Device

A controllable valve device which may be turned on and off by a control signal, for example an IGBT.

1.3.2 Insulated Gate Bipolar Transistor, IGBT

A controllable switch with the capability to turn-on and turn-off a load current. An IGBT has three terminals: a gate terminal (G) and two load terminals emitter (E) and collector (C).

By applying appropriate gate to emitter voltages, current in one direction can be controlled, i.e. turned on and turned off.

1.3.3 Free-wheeling Diode, FWD

Power semiconductor device with diode characteristic. A FWD has two terminals: an anode (A) and a cathode (K). The current through FWDs is in opposite direction to the IGBT current.

FWDs are characterized by the capability to cope with high rates of decrease of current caused by the switching behaviour of the IGBT.

1.3.4 IGBT-Diode Pair

Arrangement of IGBT and FWD connected in inverse parallel.

1.4 VSC TOPOLOGIES

1.4.1 Two-level Converter

A converter in which the voltage at ac terminals of the VSC unit is switched between two discrete dc voltage levels.

1.4.2 Three-level Converter

A converter in which the voltage at ac terminals of the VSC unit is switched between three discrete dc voltage levels.

1.4.3 Multi-level Converter

A converter in which the voltage at ac terminals of the VSC unit is switched between more than three-dc voltage levels.

1.4.4 Modular Multi-Level Converter, MMC

Multi-level converter in which each VSC valve consists of a number of self-contained, single-phase Voltage Sourced Converters connected in series.

1.5 VSC UNIT

Three VSC phase units, together with VSC unit control equipment, essential protective and switching devices, submodule dc capacitors, valve reactor and auxiliaries, if any, used for conversion.

1.5.1 VSC Phase Unit

The equipment used to connect the two dc busbars to one ac terminal.

NOTE – In the simplest implementation this consists of two VSC valves. In some case, this consists of two VSC valves and valve reactors. The VSC phase unit may also include control and protection equipment, and other components.

1.5.2 VSC Valve

Complete controllable device assembly, which represents a functional unit as part of a VSC phase unit and characterized by switching actions of the power electronic devices upon control signals of the converter base electronics

NOTE - Dependent on the converter topology, a valve can either have the function of controllable switch or a controllable voltage source.

1.5.3 Diode Valve

A semiconductor valve containing diodes but no switched semiconductor devices, which might be used in some VSC topologies,

1.5.4 Valve

Refer to VSC valve or diode valve according to the context.

1.5.5 VSC Valve Level

Part of a VSC valve comprising a controllable switch and an associated diode, or controllable switches and diodes connected in parallel, or controllable switches and diodes connected in a half bridge arrangement, together with their immediate auxiliaries, storage capacitor and bypass switch, if any.

NOTE - In the context of Modular Multi-Level Converters, the term “Submodule” is also used to refer to a VSC Valve Level.

1.5.6 Diode Valve Level

Part of a diode valve composed of a diode and associated circuits and components, if any.

1.5.7 Redundant Levels

The maximum number of VSC valve levels or diode valve levels in a valve that may be short-circuited externally or internally during service without affecting the safe operation of the valve as demonstrated by type tests, and which if and when exceeded, would require shutdown of the valve to replace the failed levels or acceptance of an increased risk of failures.

1.5.8 Valve Protective Blocking

Means of protecting the valve or converter from excessive electrical stress caused by the emergency turn-off of all IGBTs in one or more valves.

1.5.9 Submodule DC Capacitor

A capacitor (if any) used as part of a certain VSC valve level, which is used as an energy storage dc source.

1.5.10 Valve Reactor

A reactor (if any) which is connected in series with the VSC valve. One or more valve reactors can be associated with one VSC valve and might be connected at different positions within the valve. According to this definition valve reactors are not part of the VSC valve. However, it is also possible to integrate the valve reactors in the structural design of the VSC valve, e.g. into each valve level.

Note: at present valve reactors are used in a converter topology with valves acting like controllable voltage sources only.

1.6 VALVE STRUCTURE

Physical structure holding the levels of a valve which is insulated to the appropriate voltage above earth potential.

1.6.1 Valve Support

That part of the valve which mechanically supports and electrically insulates the active part of the valve from earth potential.

NOTE – A part of a valve which is clearly identifiable in a discrete form to be a valve support may not exist in all designs of valves.

1.6.2 Multiple Valve Unit, MVU

Mechanical arrangement of two or more valves or one or more VSC phase units sharing a common valve support.

NOTE – A MVU might not exist in all topologies and physical arrangement of converters.

1.6.3 Valve Section

Electrical assembly, composing a number of VSC or diode valve levels and other components, which exhibits pro-rated electrical properties of a complete valve

1.6.4 Valve Base Electronics, VBE

Electronic unit, at earth potential, which is the interface between the converter control system and the VSC valves.

1.7 VSC TRANSMISSION

1.7.1 Interface Transformer

Transformer (if any) through which power is transmitted between the ac system connection point and one or more VSC units.

1.7.2 Phase Reactor

A reactor connected directly to the ac terminal of the VSC phase unit, and combined with interface transformer leakage reactance (if any), in order to provide the commutating reactance.

1.7.3 VSC DC Capacitor

Capacitor bank (s) (if any) used as energy storage and / or for filtering purposes.

1.7.4 AC System Side Harmonic Filter

A filter (if any) used to prevent harmonics generated by VSC from penetrating into the ac system. The filter can be located at a point of common coupling (outside the interface transformer) or/ and on the valve side (inside the interface transformer).

1.7.5 AC side Radio Frequency Interference Filter (RFI Filter)

Filters (if any) used to reduce penetration of Radio Frequency (RF) into the ac system to acceptable level.

1.7.6 HF-blocking Filter

Filters (if any) used to reduce penetration of high frequency (HF) harmonics into the ac system to acceptable level.

1.7.7 Valve Side Harmonic Filter

Filters (if any) used to mitigate the HF stresses of the interface transformer.

1.7.8 Common Mode Blocking Reactor

A reactor (if any) used to reduce common mode harmonic currents flowing into a dc overhead line or cable of a symmetric monopole long distance transmission scheme.

1.7.9 DC Harmonic Filter

DC filters (if any) used to prevent harmonics generated by the VSC valves from penetrating into the dc system. The filter can consist of a tuned shunt branch, smoothing reactor or common mode blocking reactor or combinations thereof.

1.7.10 DC Reactor

A reactor (if any) connected in series with a dc overhead transmission line or cable, used to reduce harmonic currents flowing in the dc line or cable and to detune critical resonances within the dc circuit. A dc reactor might also be used for protection purposes.

1.7.11 DC side Radio Frequency Interference Filter

Filters (if any) used to reduce penetration of Radio Frequency (RF) into the dc system to acceptable limits.

1.8 OPERATING STATES

This report only defines some operating states of the components of the VSC system, but the system operating states are not included.

1.8.1 Rectifier Operation

Operating mode of a VSC unit or a VSC substation when energy is transferred from the ac side to the dc side.

1.8.2 Inverter Operation

Operating mode of a VSC unit or a VSC substation when energy is transferred from the dc side to the ac side.

1.8.3 VSC Blocking

Operation preventing further conversion by a VSC unit by inhibiting valve control signal or applying a signal to turn off IGBTs.

1.8.4 VSC Deblocking

Operation permitting the start of conversion by a converter by removing blocking action.

1.8.5 Conducting State

The condition in which load current flows through an IGBT-Diode pair. In IGBT-Diode pair, both positive and negative conducting states may exist.

1.8.6 Positive Conducting State

The condition of an IGBT-diode pair in which load current flows through the IGBT from Collector to Emitter

1.8.7 Negative Conducting State

The condition of an IGBT-diode pair in which load current flows through the FWD from Anode to Cathode

1.8.8 Blocking State

The condition of an IGBT-diode pair in which load current does not flow and a voltage is applied to the IGBT-Diode pair such that a positive voltage exists on the Collector of the IGBT with respect to the Emitter.

1.8.9 Reverse Recovery State

The condition in which the FWD carries reverse current during commutation at the specified conditions, starting at the zero-crossing of the current and ending when the reverse current has decayed to the reverse off-state current after the tail-current phase.

1.9 TYPE TESTS

Those tests which are carried out to verify that the components of VSC transmission system design will meet the requirements specified. In this report, type tests are classified into two major categories: dielectric tests and operational tests.

1.9.1 Dielectric Tests

Those tests which are carried out to verify the high voltage withstand capability of the components of a VSC transmission system.

1.9.2 Operational Tests

Those tests which are carried out to verify the turn-on (if applicable), turn-off (if applicable), and current related capabilities of the components of VSC transmission system.

1.10 PRODUCTION TESTS

Those tests which are carried out to verify proper manufacture, so that the properties of the certain component of VSC transmission system correspond to those specified.

1.10.1 Routine Tests

Those production tests which are carried out on all items of specific components in a VSC transmission system.

1.10.2 Sample Tests

Those production tests which are carried out on a small number of items of certain VSC transmission components, e.g. valve sections or special components taken at random from a batch.

1.11 INSULATION CO-ORDINATION TERMS

1.11.1 Test Withstand Voltage

Value of a test voltage of standard wave shape at which a new component, with unimpaired integrity, does not show any disruptive discharge and meets all other acceptance criteria specified for the particular test, when subjected to a specified number of applications or a specified duration of the test voltage, under specified conditions.

1.11.2 Internal and External Insulation

Air external to the components and insulating materials of the valve, but contained within the profile of the valve or multiple valve unit is considered as part of the internal insulation system of the valve. The external insulation is the air between the external surface of the valve or multiple valve unit and its surroundings.

1.12 POWER LOSSES

1.12.1 Auxiliary Losses

The electric power required to feed the VSC substation auxiliary loads. The auxiliary losses depend on whether the substation is in no-load or carrying load states, in which case the auxiliary losses depend on the load level.

1.12.2 Standby Losses

The losses produced in an item of equipment with the VSC substation energized but with the converter valves blocked and all substation service loads and auxiliary equipment connected as required for immediate pick-up of load. If a tap changer is used, the calculation is done at the tap position for immediate pick up of load.

1.12.3 No-load operating losses

The losses produced in an item of equipment with the VSC substation energized and with the VSCs de-blocked but with no real or reactive power output.

1.12.4 Operating Losses

The losses produced in an item of equipment at a given load level with the VSC substation energized and the converters operating.

1.12.5 Total System Loss

The total system loss is the sum of all operating losses, including the corresponding auxiliary losses.

1.13 REFERENCES

[1-1] IEC 60633. *Terminology for high-voltage direct current (HVDC) transmission*, October 16, 1998.

[1-2] IEC 62501. *Electrical testing of voltage sourced converter (VSC) valves for high-voltage direct current (HVDC) power transmission*, June, 2009.

[1-3] IEC 61803. *Determination of power losses of in high voltage direct current (HVDC) converter stations*, February, 1999.

[1-4] Cigré WG B4.37 *DC Transmission Using Voltage Sourced Converters*. Cigré Technical Brochure No**.** 269; 2005.

[1-5] International Electronic Vocabulary 551-14-03. *Controllable valve device a valve device the current path of which is bitable controlled in its conducting direction*.

[1-6] International Electronic Vocabulary 551-14-08. *Switched valve device a controllable valve device which may be turned on and off by a control signal*.

2. BASIC CONFIGURATION

2.1 OVERVIEW OF THE VSC SYSTEM

Figure1.1 shows the typical arrangements of the VSC transmission system, which is quite similar to the Classic HVDC technology. The major difference is the converter technology; Classic HVDC is based on line-commutated converters utilizing thyristors without turn-off capability, whereas VSC-HVDC is based on self-commutated converter technology.

Depending on the design the main components of VSC transmission system might vary. Some components, such as VSC converter, dc voltage source, phase/valve reactors, transformers or a combination of these components, are essential. The dc voltage source may be a capacitor bank connected in parallel with the dc transmission circuit and earth or a capacitor distributed in the valve unit. The other components may include ac and dc filters, transformers, surge arresters, circuit breakers and switches, measuring equipment, etc,

In contrast to Classic HVDC, the polarity of the dc voltage in a VSC-HVDC system is constant and power transfer direction is changed by changing the polarity of the dc current. Due to that fact, it is expected to be simpler to control and to protect so called multi-terminal systems using VSC technologies. In such systems, more than two converters are connected to the dc link.

The conversion of ac to dc voltage and vice versa is realized in the converter itself. Many VSC topologies and configurations have been proposed and discussed in literature.

The interface inductance can be implemented as phase reactors (if any), as valve reactors (if any), as leakage inductances of the transformers, or as combination thereof. Depending on the converter topology ac filters are necessary to reduce harmonic distortion caused by the ac voltage generated by the converter.

2.2 GENERAL DESCRIPTION OF POWER SEMICONDUCTOR DEVICES

In normal operation of voltage-sourced converters the power semiconductors are exposed to dc voltage and have to be able to conduct the current in both directions. Therefore power semiconductor switches with turn-on and turn-off capability and with a high voltage blocking capability (typically several kV) in forward direction are needed.

Today these requirements are achieved by a parallel connection of a controllable switch and a FWD as shown in Figure 2.1.

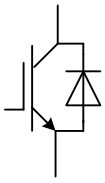


Figure 2.1 Symbol of a controllable switch and associated FWD

Different semiconductor switches are possible for VSC technology, but only IGBTs (Insulated Gate Bipolar Transistor) have been used in the commercial VSC-HVDC systems implemented today. Therefore the description of semiconductor switches in this document is dealing with IGBTs although other semiconductors such as GTOs and IGCTs are also possible.

Like all diodes, the free-wheeling diodes, which are connected in parallel to the controllable switch, have a significant reverse recovery current when they turn off. Both the IGBTs and the free-wheeling diodes have to cope with switching transients, particularly current gradients and voltage gradients.

An IGBT is a voltage controlled device only capacitive currents can flow in the gate terminal. The device can be controlled at any instant, even during the switching, i.e. the load current can be influenced by the gate voltage.

IGBTs are short-circuit proof within defined operating conditions. This means that in case of a short circuit the IGBT limits the load current to several kA. Within some microseconds, an appropriate gate turn-off signal has to be applied to turn off the fault current in order to avoid thermally overstressing the device.

Switching time of IGBTs is in the range of microseconds or less. Furthermore, the switching slopes can be adjusted by the gate drive circuit, achieving the optimal waveforms concerning over-voltage peaks and switching losses. Snubbers to keep the rates of rise of current and voltage to acceptable limits are not necessary in many cases. The gate drivers for IGBTs can be quite simple, because they need only a few watts of control power to drive the gate.

High power IGBTs are made up by parallel connection of several chips to achieve the required current capability. The chips are mounted in press packs or module housings. In most cases the FWD chips are included in the same housing.

Press pack housings are intended for double sided cooling. They are usually clamped between heat sinks; the paths for current and heat are the metallic surfaces of the collector and emitter sides of the devices, which are separated by a ring of insulating material. For high voltage devices, this material is high strength porcelain in most cases, though glass fiber reinforced resin is also used. In the press pack IGBT design shown in Figure 2.2 the semiconductor chips are sub-divided in so called sub-modules, each one containing a number of IGBT and diode chips. The press pack IGBT is typically designed to fail in a short circuit mode. Such design enables a continuous current flow through the faulted VSC valve level without the need for bypass devices.

Figure 2.2 Photograph of an IGBT Press pack

Standard IGBT modules, Figure 2.3, have for years been commonly used in industry and traction drives with and without series or parallel connection. They are designed for single sided cooling, and spring loaded clamping is not necessary. The electrical terminals are on the top side of the module, the heat flows through the base plate of the module to the heat sink. Since the electrical part of the module is insulated to the base plate, it is possible to mount modules with different voltage potentials on a shared heat sink.

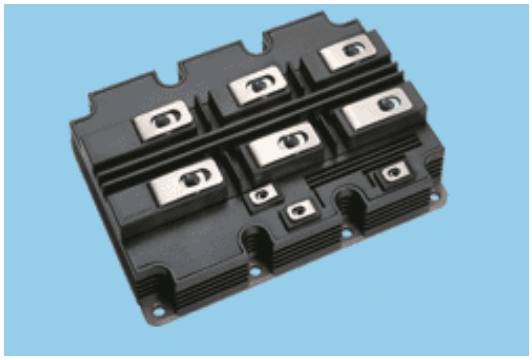


Figure 2.3 Photograph of an IGBT module

As of this writing, IGBTs are commercially available up to 6.5 kilovolts (kV) and with both housing technologies and maximum turn-off currents up to 5~10 times the rated current.

2.3 CONVERTER TOPOLOGIES

The basic ac output waveform of a VSC is determined by the topology of the converter and characterized by the number of possible voltage levels. Two-level and three-level converter topologies are well known since these topologies are also widely used in drive applications.

In VSC-HVDC the two-level and three-level converters utilize VSC valves, which are characterized by a series connection of VSC levels to achieve the required voltage capability. All the IGBTs have to be switched simultaneously in order to ensure an even voltage distribution of the different levels not only statically but also transiently. In these topologies, one or more common dc link capacitors are utilized, to which the VSC phase units are connected. In that case, the VSC valves have a switching character, i.e. to enable or disable current flow in one direction. Therefore the term ‘valve’ describes its behavior quite well as the purpose of the VSC valve is to switch the current (VSC valves of the ‘Switch’ type).

In contrast to that, so called modular multilevel converter (MMC) topologies are relatively new. These topologies are characterized by the fact, that there are no common dc link capacitors for all VSC phase units but the capacitors are distributed within the VSC valve levels. The purpose of the valve is to generate a controllable voltage, which leads to the term of the 〝Controllable voltage source〞 type. For MMC topology it is not necessary to switch all the IGBTs in one valve simultaneously.

2.3.1 Converter topologies with VSC valves acting as a Switch

VSC valves of this type consist of a large number of series-connected IGBT devices which are switched simultaneously. Valves of this type are normally used with converters with a relatively low number of output levels. There is no significant energy stored within the valve.

2.3.1.1 Two-level converter

A two-level phase unit is the simplest switching arrangement capable of producing ac output from a dc source in the form of a simple square-wave. A three-phase converter using three two-level phase units is illustrated in Figure 2.4.

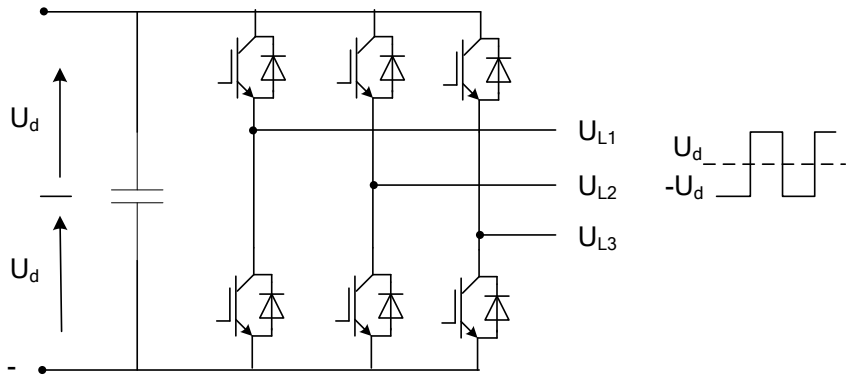


Figure 2.4 Diagram of a three-phase two-level converter and associated ac waveform for one phase

The ac waveform shown in the Figure 2.4 is the phase-to-neutral voltage assuming fundamental frequency switching of the phase units. The neutral voltage is the voltage at the midpoint of the VSC dc capacitor.

Due to the square-wave output voltage waveform, the two-level phase unit is unable to facilitate direct control of the amplitude of its fundamental output voltage without the application of PWM.

A typical PWM switched waveform, using a carrier based control method with a switching frequency of 21 times the fundamental is given in Figure 2.5. For the purpose of this illustration the VSC dc capacitor has been assumed to have an infinite capacitance (i.e. no dc voltage ripple).

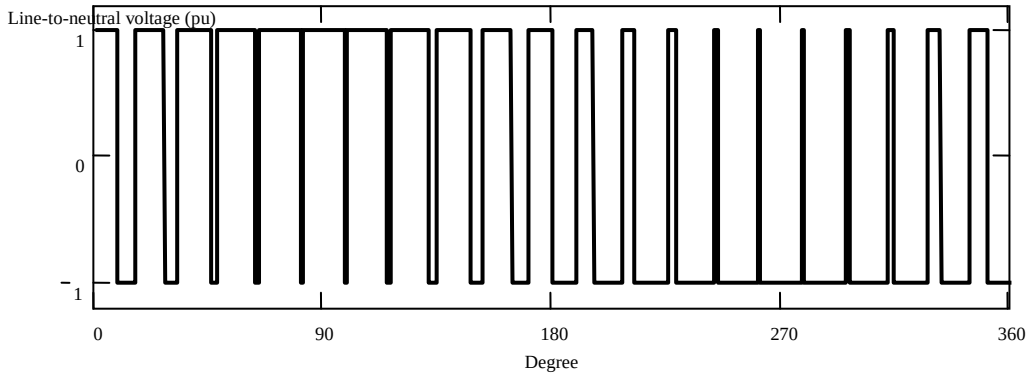


Figure 2.5 Single Phase ac output for 2-level NPC converter with PWM switching at 21 times fundamental frequency

2.3.1.2 Multi-Level Flying Capacitor Topology

In the multilevel converter(more than three levels) it is possible to realize an amplitude modulation of the

converter voltage by small voltage steps. The number of devices in series connection which switch at the same time is reduced, resulting in lower dv/dt in the realized voltage waveform on the ac terminals. Furthermore the pulse frequency of a single device can be reduced.

Based on the same switching frequency and equal dv/dt per switching device harmonics and electromagnetic interference (EMI) emission is lower compared to two-level and three-level converters. Thus filter circuits can be much smaller or even eliminated.

2.3.2 Converter topologies with VSC valves of the 〝Controllable voltage source〞 type

VSC valves of this type consist of a large number of series-connected VSC valve levels. Each VSC valve level contains power semiconductors and a capacitor for energy storage. Each level has two main terminals used for the series connection of the VSC valve levels within the valve. By appropriate control of the IGBTs within the valve level, either the voltage of the capacitor or zero volts can be applied to the main terminals of the VSC valve level.

By individual and appropriate control of the VSC valve levels, a desired valve voltage can be applied to valve terminals. The valve voltage is the sum of those capacitor voltages, of which the voltage is applied to the main terminals of the VSC valve level.

Assuming infinite storage capacitances with equal voltages in the individual valve levels, n+1 different voltage steps can be applied to the terminals of a valve consisting of n valve levels. Assuming a high number of VSC valve levels per valve the topology can be approximated by electrical equivalent as shown in Figure 2.6. Each valve can be considered as a controllable voltage source.

The valve reactors are part of the interface inductance and are essential for the current control within the phase units. Furthermore they also limit the peak current and current gradients in case of severe faults, such as short circuit between the dc terminals.

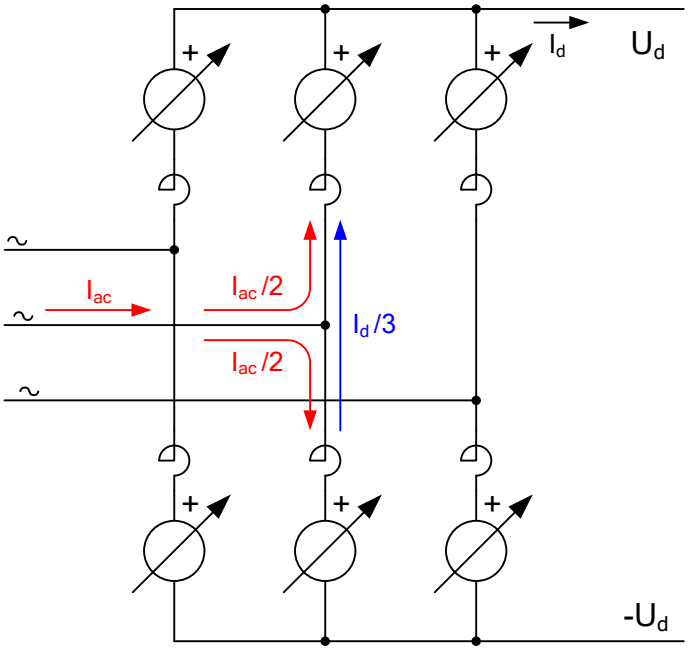


Figure 2.6 Electrical equivalent a converter with VSC valves acting like controllable voltage sources

So far, only one converter topology with valves acting like voltage sources has been realized for a commercial HVDC project. Due to its modular design and the multi-level technology it is referred to as Modular Multi-level Converter (MMC) topology.

Each of the 6 variable voltage sources shown in Figure 2.6 is realised with series connection of identical submodules with an electrical equivalent as shown in Figure 2.7. According to definitions in chapter 1.5.5, each submodule represents one VSC valve level.

The submodule is a two-terminal component with its own submodule dc capacitor unit as shown in Figure 2.7. These submodules are individually controlled and can be switched between a state with full module voltage (voltage of the associated storage capacitor) and a state with zero module voltage for both current directions. If the module voltage is applied to the submodule terminals, the capacitor can be charged and discharged dependent on the current direction of the converter phase arm.

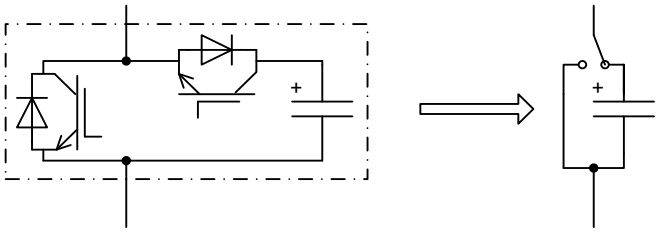


Figure 2.7 Submodule arrangement and equivalent circuit in Topologies with valves acting like controlled voltage sources

The electrical arrangement of submodules and valve reactors in a converter block is shown in the Figure 2.8.

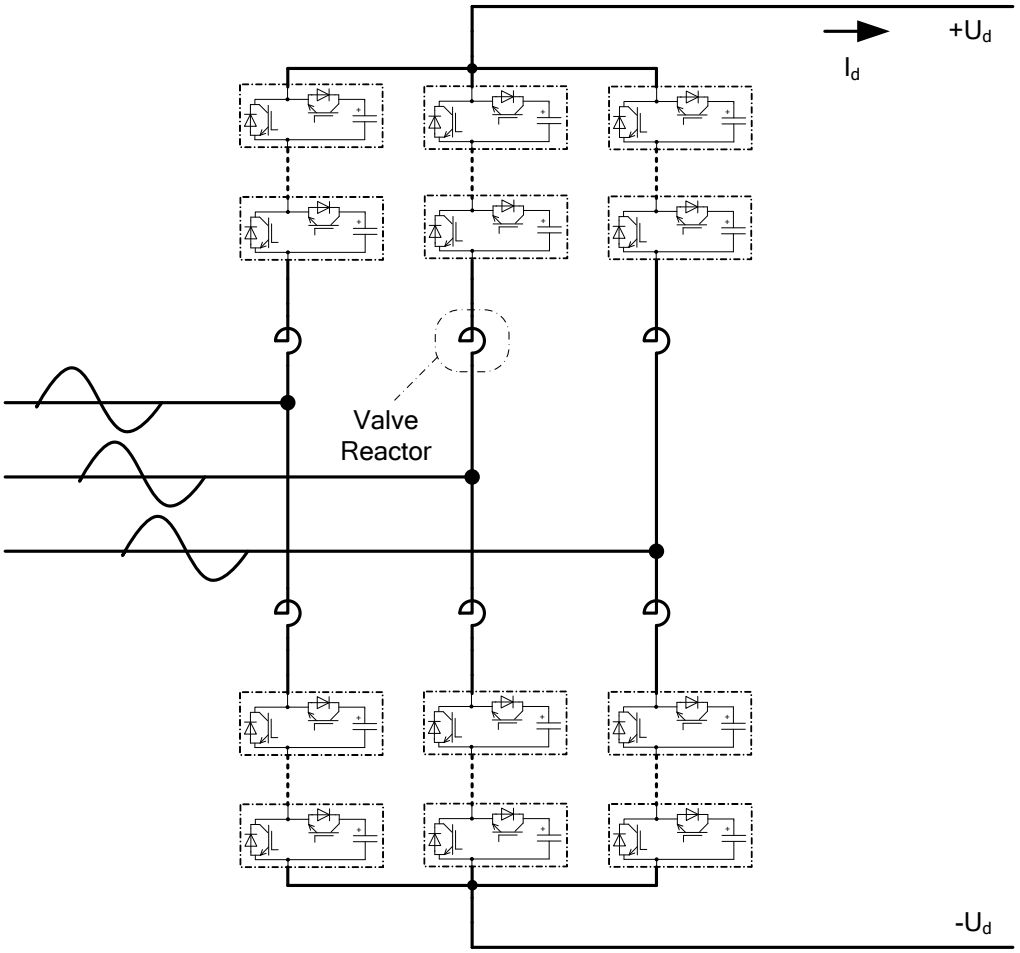


Figure 2.8 Converter block arrangement with topologies with valves acting like controlled voltage sources

The submodules are controlled in a way that the sum of the upper and lower arm of one phase unit equals to the dc voltage whereas the instantaneous voltage on the ac terminals is determined by the ratio of the voltages of the two converter phase arms of one phase unit.

Since the circuit is inherently modular, it is relatively straightforward to obtain high numbers of output levels, without requiring either PWM or series-connected IGBTs (which require ensuring voltage distribution). Thus, ac filters can be omitted in many cases.

2.4 NEUTRAL GROUNDING ARRANGEMENTS

The purpose of the neutral grounding arrangement is to provide a defined voltage bias from the dc circuit to ground in order to define the potential of the dc circuit with respect to ground and to ensure that the station ground grid is not exposed to sustained dc currents. One very important aspect is that the grounding arrangement must ensure that the dc voltage of a dc transmission line is a true dc voltage. Depending on the design concept, the dc neutral grounding can be arranged in different ways. In case of a balanced bipolar scheme, as in Figure 3.11a, the capacitor neutral point can be directly grounded.

In case of an asymmetric monopolar VSC-HVDC scheme, the converter neutrals must be grounded via an

HVDC electrode, as for classical HVDC, see Figure 2.9.

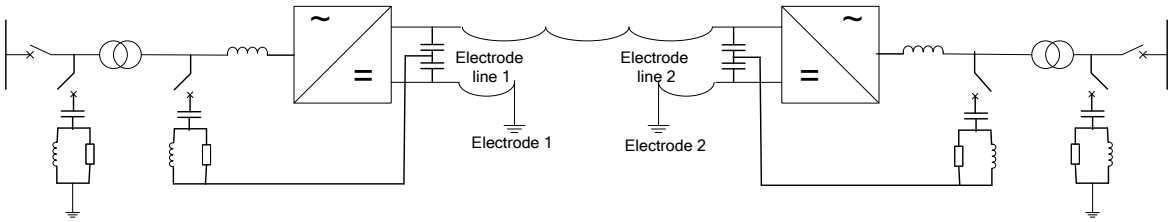


Figure 2.9 Neutral grounding arrangements for an asymmetric monopolar VSC-HVDC transmission system.

As an alternative a metallic return arrangement can be used. With reference to Figure 2.9, it can be seen as the electrode line 2 is extended to the electrode 2, which then is a common electrode for both stations. However, when the neutrals of the two stations are connected via a metallic return neutral conductor as shown in Figure 5.23, the electrode is only conducting insulator leakage currents and corona currents flowing to ground and not any dc load current.

When the VSC converter is grounded via an electrode line, the converter neutral must be protected by capacitor, arresters or a combination of capacitors and arresters.

The grounding options for topologies with valves acting like controlled voltage sources are shown in Figure 2.10. In case of a balanced bipolar scheme, special grounding devices arranged on the ac side could be used in order to provide high impedance for line frequency and low impedance for dc. And also it could be arranged on the dc side to provide high impedance for dc.

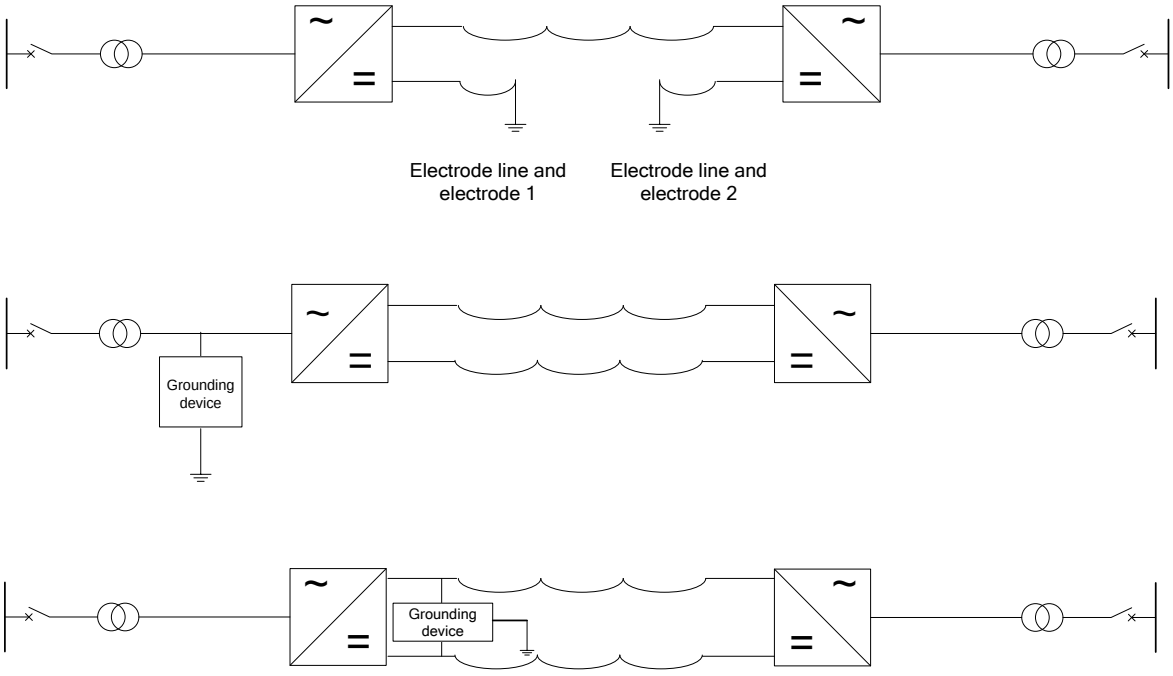


Figure 2.10 Grounding arrangement for an asymmetric monopolar (top) and symmetric monopolar VSC-HVDC transmission system based on topologies with valves acting like controlled voltage sources.

2.5 VSC TRANSMISSION SYSTEM STRUCTURE IN DIFFERENT APPLICATION FIELDS

Due to the various applications, VSC transmission may have rather different electric structure, and thus different voltage and current stress. The main aspects are as follows:

(1) Long-distance VSC transmission

In long-distance VSC transmission systems, the dc network consists of the long-distance transmission lines or cables and optional dc reactors connected in series connection with the lines or cables. As compared to LCC based HVDC systems, the dc reactors of a VSC will have significantly lower inductance. The impedance of the dc network has to be considered when analyzing of system states and stresses. For instance, variations in transmitted dc power will lead to the changes of dc current but minor changes in the dc voltage. The prerequisite for normal operation of VSC transmission is to keep the dc side voltage within a normal range. Secondly, the dynamic behavior of the system is largely dependent on the rate of change in the dc current. The rate of change of the dc current is different for long-distance line or cable systems, and consequently influences the dynamic behavior of system.

(2) BTB VSC transmission

Back-to-back (BTB) VSC transmission is primarily adopted for the interconnection of asynchronous ac systems with the same or different frequency ratings. The electrical link between the VSC substations is very short in a BTB system as they are directly connected without any dc lines or reactor. Therefore variation of electric parameters in either side tends to spread rapidly to the other side. In the event of an ac system fault, the spread of the fault via the VSC substations should be specially taken into account.

(3) Supply to isolated network

When VSC substations are used to supply power to isolated networks they are generally connected to a weak or passive ac systems, the equivalent impedances of the ac systems and the loads are relatively large. Under such conditions, the VSC substation normally adopts fixed ac voltage control and may inject large amount of reactive power to the ac system to ensure the system voltage stability. Therefore when we study the states and stresses of the transmission system, the control strategies and the ac system power factors must be taken into account.

(4) VSC based multi-terminal HVDC transmission

As the power flow reversal in VSC transmission will be conducted by the reversal of the dc current but not by the reversal of dc voltage, VSC systems could be best suited for multi-terminal HVDC schemes. The drawback of this structure is that due to the multiple connections of VSC converter stations in the dc network, variation of any electric parameters (voltage, current and power) is likely to spread to the whole system via the dc network. AC system faults in sending and receiving ends can be easily handled by blocking the converters so this type system could be robust as long as there is power balance in the system.

2.6 REFERENCES

[2-1] Cigré WG B4.37 *DC Transmission Using Voltage Sourced Converters*. Cigré Technical Brochure No. 269; 2005

[2-2]Cigré Joint Working Group B4/A3/B3.43, *Increased System Efficiency by use of new Generations of Power Semiconductors* Cigré Technical Brochure No. 337; 2007.

3. FUNCTION OF THE COMPONENTS AND SUBSYSTEMS

3.1 INTRODUCTION

There are many components necessary for a VSC transmission system. In principle the two converter stations are identical. The main components which are essential for the converter station are the VSC valves, interface transformer, phase/valve reactor, VSC/submodule dc capacitors and their auxiliary equipments. Other components, such as ac and dc filters, smoothing reactor, common mode blocking reactor, etc are selectively adopted according to the VSC topology.

The interface inductance between VSC and the ac system is required and can be implemented as phase reactors (if any), as valve reactors (if any), as leakage inductance of the transformer, or as combination thereof. The interface inductance serves two main purposes: it enables the control of active and reactive output power from the VSC and it limits the fault current in case of certain failures. The proper ac voltage is provided by interface transformer and the dc voltage is supported by the dc storage capacitors.

Each VSC can be operated as an inverter, injecting real power into the ac network, or as a rectifier, absorbing power from the ac network. Similarly, the VSC can be operated either capacitive, injecting reactive power into the ac network, or inductively, absorbing reactive power from the ac network. Active and reactive power can be independently controlled within the specified limits of the VSC.

In this chapter the components of VSC system and their functions are discussed. The stresses analysis in chapters 4 and 5 are based on the discussion here.

3.2 FUNCTION OF THE DIFFERENT COMPONENTS AND SUBSYSTEMS TO BE TESTED

3.2.1 VSC Valve in topologies where a valve acts as a controllable switch

3.2.1.1 General

The IGBTs in the VSC valves operate in the converter as switches and are capable of turning on and off in response to control signals. The power and voltage conversion between ac and dc is performed by valves [3-1]. The control signal for a valve is derived from PWM algorithm and the switching frequency is several kHz so the IGBT valves turn on and off a few ten times during the power frequency period.

The basic ac output waveform of a VSC is determined by the topology of the converter. The operating principle of a 2-level VSC is described in the following paragraphs.

A schematic of one-phase of a 2-level converter is presented in Figure 3.1. As shown, it is capable of generating the two voltage levels. In order to improve the quality of the output voltage, PWM can be used to produce an output waveform with dominant fundamental component, but also high-order harmonics, as described in [3-2].

In a VSC, the switches are implemented as solid-state switches and the voltage source input characteristic is obtained by connecting two VSC dc capacitors in series, as shown in Figure 3.1.

The midpoint of the capacitors can be considered as the reference point for the ac output voltage of the phase unit Uac = Uconv. The output terminals can only be connected at two voltage levels: the positive dc voltage + U_d, or the negative dc voltage -U_d (two-level converters). Thus the direct voltage in Figure 3.1 can only have one polarity due to the free-wheeling diodes, whereas the current can flow in both directions.

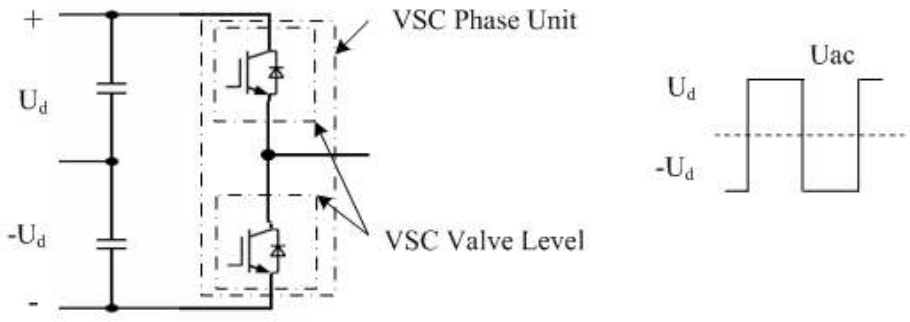


Figure 3.1 Basic Configuration of VSC Valve

Voltage withstanding capability of the insulation of the VSC valve must be designed adequately. Various stresses which will be experienced by the equipment must be considered, such as maximum continuous voltage which will appear in normal operating conditions, and peak transient over-voltage which will appear only during fault conditions. The valves must be designed considering the stresses to avoid the valve failure under both steady state and fault conditions.

Variation of the insulation capability and characteristics with the atmospheric conditions, such as temperature, humidity, air pressure should be taken into account during the VSC valve design.

PWM is typically applied as a control strategy for this type of converter. The PWM utilizes the switching of the IGBTs in a manner to convert the dc voltage into voltage pulses of certain shape, so as to realize frequency conversion and voltage variation, and thus effectively control and eliminate harmonics. PWM control technology provides the fast control of the converter output voltage. The disadvantage of PWM is the increase in the converter losses due to the high frequency switching of the IGBTs.

The functions of PWM:

- Control of the output ac voltage ,
- Minimizing the harmonic content of output ac voltage,
- Improving the response of the converter under fault conditions and load variations.

Sinusoidal pulse width modulation PWM (SPWM)

Sine pulse width modulation PWM adopts sine wave as the modulation wave and triangular wave as the carrier wave.

Corresponding to 2-level and multilevel VSC, there are single-carrier and multi-carrier modulation techniques.

PWM with 3-rd harmonics (3PWM)

For the three-phase system with floating neutral, the introduction of a third harmonic component or a dc component into the 3-phase VSC output voltage will have no effect on the grid side voltage wave. In addition the injection of zero-sequence component in sine modulation wave will not change the fundamental frequency component of 3-phase VSC output voltage. Therefore carrier PWM can be optimized by injection of various zero-sequence components.

In 3 PWM a third harmonic is added into the fundamental frequency modulation wave. The third harmonics in the VSC output phase voltage are canceled in the line voltage. Figure 3.2 shows the 3PWM wave (blue) which consists of a third harmonic (red) wave and a fundamental (black) wave.

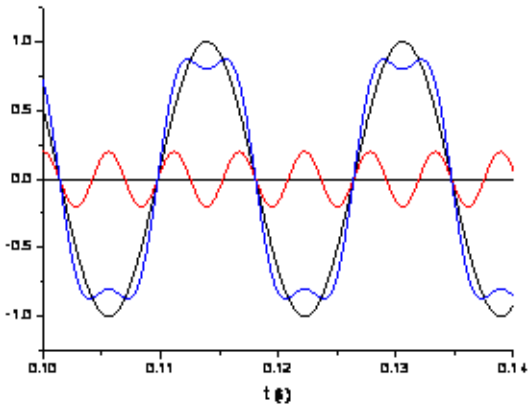


Figure 3.2 Third harmonic injection PWM modulation

Optimized PWM (OPWM)

In addition to satisfying the fundamental frequency output voltage (modulation index), OPWM can eliminate certain harmonics, low order harmonics in general, or achieve other optimization targets such as reducing the switch losses, decreasing the total harmonic distortion (THD) and harmonic stress, etc. A bipolar OPWM with three switching angles is illustrated in Figure 3.3.

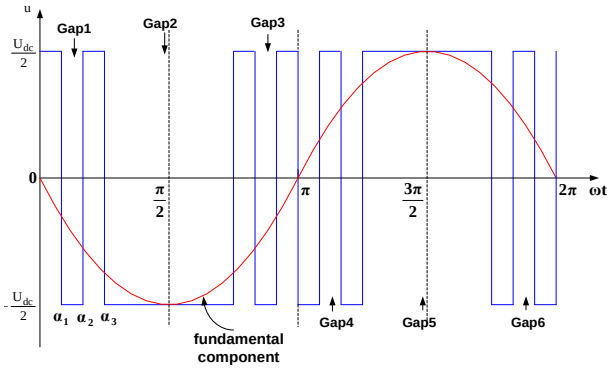


Figure 3.3 Bipolar OPWM with three switching angles

The principle of OPWM is to choose the right triggering pulses (α_1、 α_2、 … α_M) to achieve the

fundamental frequency output of the converter, and at the same time eliminate low order harmonics and realize optimization. In spite of the increased content of higher order harmonics, the overall capacity of the filter is reduced. It's necessary to point out that the equations for solving for the angles are nonlinear transcendental equations. The switching frequency is defined as:

$$f_{sw} = (2M + 1) \cdot f ,$$

where M is the number of angles per quarter period and f is the fundamental frequency.

Space Vector Control

Space Vector control is different from carrier modulation. It is derived from control of electric motors and used to decide the switching of each IGBT in VSC valves. It aims to get steady amplitude circular magnetic field, i.e. sine shaped magnetic flux. With the reference to the ideal flux circle of ac motors supplied by three phase symmetrical sine voltages, it utilizes the actual flux generated by various switching modes of the VSC to approach the reference flux.

3.2.1.2 Functional structure of converter valves

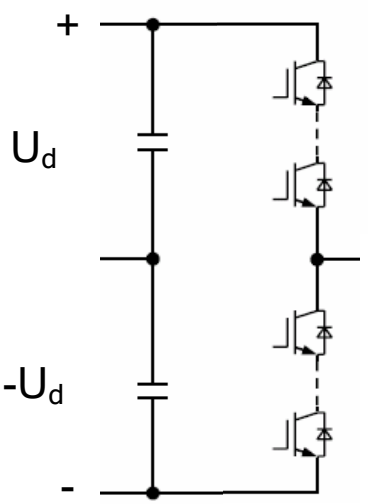


Figure 3.4 VSC Valve with series connected power electronic device

Because of the very high voltage rating of an HVDC converter, each single valve is comprise a large number of series-connected IGBT levels as shown in Figure 3.4. Proper voltage sharing is therefore crucial to ensure similar operating conditions for all devices. The use of snubber circuits will improve the voltage sharing between the different IGBT levels, but they also add to the complexity of the VSC valve and may increase the power losses. It is possible to design the VSC valve such that it does not use traditional snubber circuits for protecting the individual IGBTs. In this case, the IGBTs must themselves maintain sufficient voltage sharing, during both switching and blocked conditions, by means of gate control.

The VSC valve level must include the anti-parallel connected FWD because the IGBT is not capable of reverse conduction. In addition the VSC valve level has the components which fulfill the function of voltage

grading, monitoring, control, protection and cooling. So a complete VSC valve level consists of IGBTs, gate driver units, voltage grading circuits and heat sinks. Each gate driver unit includes power supply, firing circuits, measuring and monitoring circuits and optical interfaces. The firing–electronics controls the gate voltage and current at turn-on and turn-off, to achieve optimal turn-on and turn-off processes of the IGBT. The voltage across the IGBT is measured, and the information is sent to the valve base electronics via optical fiber cables. The voltage grading circuit connected across the IGBT may be used to provide the gate driver unit with power.

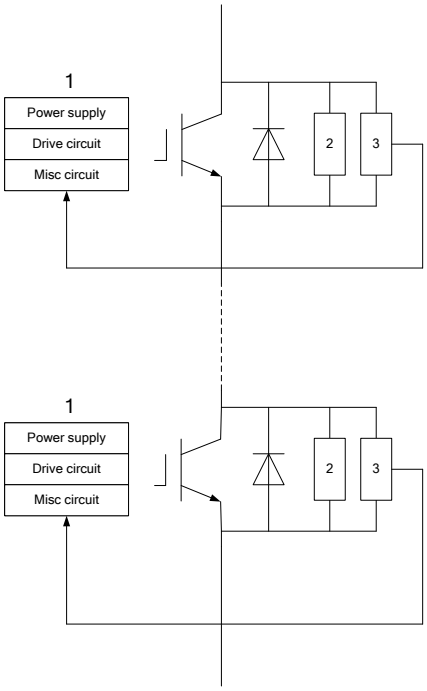


Figure 3.5 Typical structure of VSC valve units

In Figure 3.5, 1 is gate driver unit, 2 is voltage grading circuit, 3 is voltage measuring circuit.

Gate driver unit

Gate driver unit (GDU) is the most important electronic subsystem in the valve. Serving as the interface between the VSC valve level and valve base electronics through–optical fiber cables, it incorporates the functions of firing signal amplification, local signal processing, and protection of IGBT.

Voltage grading circuit

Voltage grading circuit is connected in parallel to a valve level to provide good voltage sharing under steady state and switching transient state between series connected valve levels.

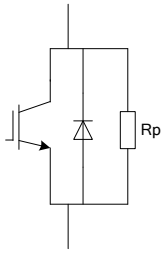


Figure 3.6 Voltage grading circuit on steady state

Voltage measuring circuit

The voltage across the IGBT during switching is measured by a voltage measuring circuit and then sent to the valve control unit. Based on this information, the valve control unit can determine if the operating state of IGBT is good and block the current immediately if a short circuit is detected so as to prevent damage to the converter.

Valve Protection System

Valve Over Voltage Protection, VOVP

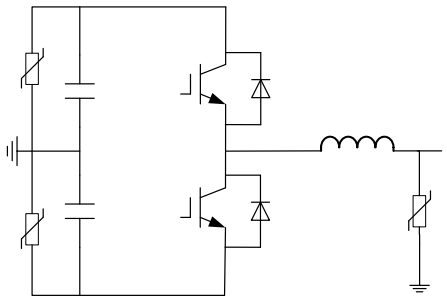


Figure 3.7 Arrester locations

Valve overvoltage protection is achieved in two ways. One of them is realized by the application of valve arresters shown in Figure 3.7. Valve Arrester is connected directly in parallel across the valve terminals. If turn-on occurs during the arrester operation, the valve must be designed to withstand the commutation of the maximum arrester current. The corresponding arrester current is determined from system studies considering the worst overvoltage at the instant the valve turning on. The choice of the protection level of the valve arrester determines both the stresses of the valve and of the arrester. Valve arresters are not commonly used in VSC-HVDC applications, and the overvoltage protection is typically achieved by arresters on the dc and ac side to ground.

Another way to implement valve overvoltage protection is achieved by the so called the active gate which is provided at each VSC valve level. Gate voltage control makes it possible to control the voltage between the two main terminals of IGBT at its turn off process. Suppressing the speed of turn off makes the energy stored in the loop stray inductance dissipates in the IGBT itself. With the application of the gate voltage control technology, the snubber circuit can be eliminated; however the switching losses are increased.

Valve Over Current Protection, VOCP

If current exceeds the design value, the valve is protected by blocking control signal or tripping the converter breaker. It should be recognized that overcurrent typically encountered by VSC valve may not directly damage the IGBT. However an increase in temperature of the IGBT caused by the overcurrent may impair its voltage withstand capability and can lead to its damage by the re-applied voltage.

3.2.2 VSC Valve in Topologies Where a Valve Acts as a Controllable Voltage Source

3.2.2.1 General

In comparison to topologies where the valves act as controllable switches, waveforms and principle of functionality are different in multilevel topologies with distributed capacitors as described in chapter 2.3.2, where the VSC valve levels are controlled individually.

A schematic of the converter including the individual valves is shown in Figure 2.8. Usually, not more than one VSC valve level is switched at a time instant during continuous operation. The topology is capable to generate a high number of voltage levels (see also Figure 10.13). Therefore the voltage steps at the ac terminals are equal to the voltage of the capacitor of the switched VSC valve level. The level of harmonics of the ac voltages is drastically reduced enabling the elimination of the ac filters.

During continuous operation intervals with positive and negative valve current within each cycle, charging and discharging the individual submodule dc capacitors during one line cycle period is possible.

It is therefore possible to separately and selectively control each of the individual submodule in a converter leg. So, in principle, the two converter legs of each phase module represent a controllable voltage source. In this arrangement, the total voltage of the two converter legs in one phase unit equals the dc voltage, and by adjusting the ratio of the converter leg voltages in one phase module, the desired sinusoidal voltage at the ac terminal can easily be achieved. See Figure 3.8

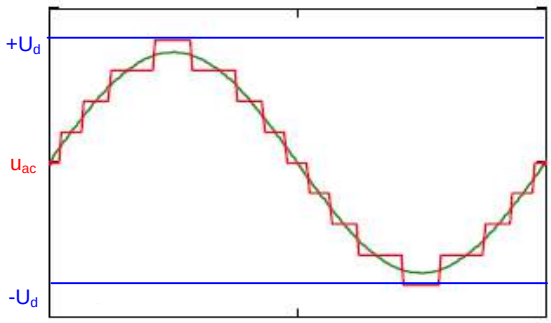


Figure 3.8 The simple principle of multilevel approach

In topologies with valves acting like controllable voltage sources, the modulation strategy is different as the VSC valve cannot be controlled as a whole. In this case, the VSC valve levels have to be controlled individually. The VSC valve levels are controlled to meet the following requirements:

- Adjust an even dc voltage of each of the three VSC phase units in order to minimize circulating currents between the VSC phase units.
- Realize a sinusoidal voltage at the ac terminals or sinusoidal ac current waveforms by adjusting the ratio of the voltage of the upper and lower VSC valve of a VSC phase unit.
- Minimization of the dc component of the current in the ac terminals due to transformer requirements.

- Balancing of the capacitor voltage of the individual VSC valve levels, i.e. keep the voltages within a defined range.

- Control power transfers between ac and dc side.

To achieve these requirements in the topologies with valves acting like controlled voltage sources, a current control system (CCS) calculates six voltage order values for each valve every few microseconds. A pulse pattern generator for each valve has to calculate the submodule states of the respective valve accordingly. The pulse pattern generators are transmitted to the module management system (MMS). The MMS communicates with the individual sub-modules via fiber optic link.
Actual switching states and the actual capacitor voltages are transmitted from the submodule electronics to the MMS system cyclically in the microsecond range. The pulse pattern generators create the switching commands for the submodules based on the desired and the actual voltages on the individual submodule dc capacitor. The command signals for the submodules are calculated every few microseconds; these commands are then transmitted to submodule electronics by the fiber optics.

The pulse pattern generator has to determine the submodules that have to be switched on or off next. The selection depends on the direction of the current and on the capacitor voltage. The aim is to avoid unnecessary charging or discharging of the capacitors, and to achieve proper balancing of the individual submodule dc capacitor voltages and balancing of the thermal load of the submodules' semiconductors of one valve.

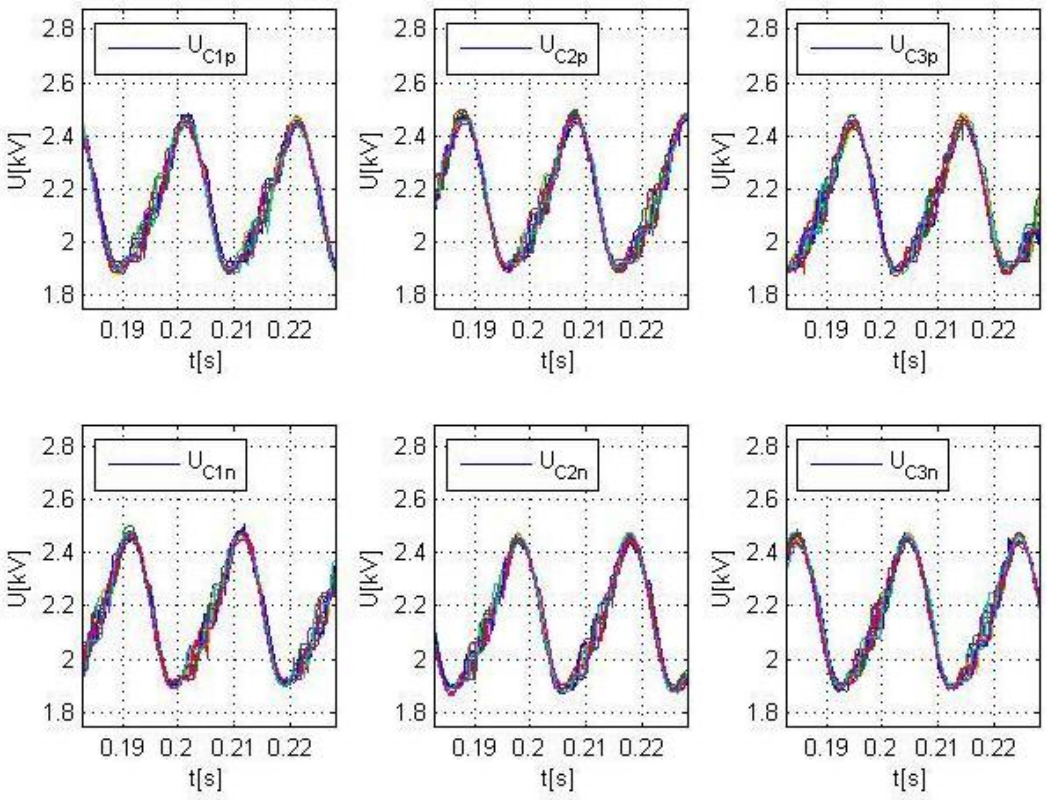


Figure 3.9 Simulation of individual storage capacitor voltages of the six valves in the topologies with valves acting like controlled voltage sources

3.2.2.2 Function structure of converter valves

The VSC valve comprises a number of series connected VSC valve levels, realized as so called submodules. Each submodule consists of a submodule dc capacitor, an IGBT half bridge with associated FWD to each IGBT and electronics. The electronics include power supply, gate drivers, capacitor voltage measurement, and communication to the MMS via fiber optic cables. Static and dynamic voltage sharing is ensured in that topology due to the capacity storage capacitors in the submodules. The switching frequency is determined by balancing requirements of the submodule voltages rather than harmonic requirements. In continuous operation, the switching frequency of the semiconductors is in the range of one hundred to two hundred hertz (Hz) depending on the number of submodules in a valve and the modulation strategy.

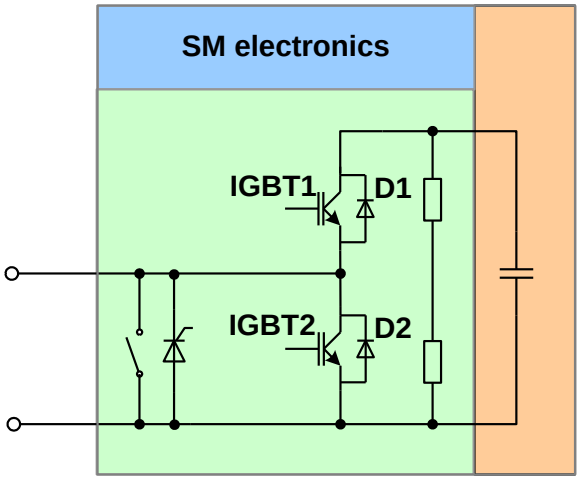


Figure 3.10 Submodule Design

Submodule

A complete submodule consists of IGBTs, storage capacitor, submodule electronics (SM electronics) and heat sinks. To ensure a voltage grading during blocking of the converter, grading resistors may be utilized.

Bypass switch

If the wire bonded IGBT (not press pack) modules are utilized, a defined short circuit is not ensured following an IGBT failure. Therefore a bypass switch can be used to ensure a low-ohmic connection at the main terminals of the submodule. The bypass switch is closed after a severe submodule failure, such as short circuit failure in a submodule or the damage of GDU, to avoid interruption of the converter operation.

Parallel thyristor

One possibility to overcome the low surge current capability of fast freewheeling diodes is to utilize a thyristor which is connected in parallel to diode D2 in Figure 3.10. In case of a dc line to line fault, the IGBTs are turned off and a signal to open the circuit breaker is commanded and trigger signals are sent to the thyristors. If on-state voltage drop of the thyristor is lower than the parallel connected FWD, a high fraction of the fault current flows through the thyristor rather than through the diode.

Structural design of the submodules

As described before, a converter valve unit consists of a simple series connection of submodules. Therefore the structural design of the converter valve unit includes the mechanical arrangement for that series connection and the manifold pipes including the associated grading devices for the water cooling of the submodules. All other components, such as free-wheeling diodes, IGBTs, cooling plates and all auxiliary electronics are integrated in the submodules. A low inductive design of the converter valve units is not necessary, because the commutation happens within the individual submodules.

Valve arresters

The over voltage protection is typically afforded by arresters on the dc and ac side to ground as mentioned in 3.2.1.2.

3.2.3 Interface Transformer

3.2.3.1 Function of the interface transformer

The interface transformer is arranged according to system requirement in a VSC transmission to fulfill the following tasks:

- Adapt a standard ac system voltage to a value matching the VSC ac output voltage and allow optimal utilization of VSC valve ratings;
- Prevent zero sequence currents from flowing between the ac system and the converter dc side;
- Provide a galvanic isolation between the dc and the ac systems;
- Provide an isolation for the dc side zero sequence voltage, especially in case of a dc voltage;
- Facilitate the variation of the valve side ac voltage for optimal utilization of the converter depending on the reactive and active power exchange.

3.2.3.2 Type and winding connection of interface transformer

The transformer may be an ordinary single or three-phase power transformer. The tap changer can be used on the primary side as well as on the secondary side or may not be needed at all. All of these concepts have been applied in different project so far.

If the interface transformer does not have an earthed neutral on the dc side, the windings of the transformer are not exposed to the stress of zero sequence harmonic and dc component currents, and the type of connection prevents the low frequency zero-sequence voltage from being injecting into the ac system. In addition, the transformer may be provided with a tertiary winding to feed the station auxiliary power system.

Furthermore, the transformer on load tap changer (LTC) allows the valve side ac voltage to be controlled to a suitable level depending on the load conditions. Therefore, the variation of the modulation index will be kept to a reasonable level. The advantage is that this will limit both the losses and the ac side harmonics, hence the

size of the ac harmonic filters.

3.2.4 Phase Reactors

In topologies where the valve acts as a controllable switch, the phase reactor is one of the key components in a VSC to perform ac output current control [3-3].

The stray capacitance across the reactor should be kept as low as possible in order to minimize the harmonics coupled to the ac system side of the reactor. The high dv/dt on the bridge terminal at each switching will result in current pulses through all capacitances to ground.

The phase reactor technology selected for the existing VSC-HVDC projects to date is the dry-type, air core. Dry-type air-core reactors are a design family of coils without a magnetic core, usually with concentric multilayer windings for natural air cooling. Each layer consists of epoxy fiberglass encapsulated conductors regularly distributed along the vertical axis of the coil. The layers are connected in parallel so that the voltage between the reactor terminals results in axial voltage stress along the winding only. After curing of the epoxy resin the winding constitutes a rigid, mechanically robust unit which is mounted on a number of support insulators to provide the insulation to ground.

There are economical and technical reasons which favour the selection of the dry-type technology for phase reactors. The main technical argument is the simplicity of the reactor's insulation to ground, providing a low stray capacitance of the reactor. A not negligible argument in favour of air core dry type reactors is the lower investment cost as compared to other design technologies.

The phase reactor fulfills the following tasks:

- Filter the high-frequency harmonic of converter output voltage to get desired waveform
- Provide the active and reactive power control
- Limit the short circuit current

In topologies where the valve acts like a controllable voltage source, the phase reactor might be omitted. In that case, some functions of the phase reactor can be fulfilled by the valve reactor.

3.2.5 Valve Reactors

Valve reactors are connected in series with the VSC valve levels as shown in Figure 2.8. Although the valve reactors are not part of the valve, the topology allows the distribution of the reactors among the VSC valve levels in small portions which are assigned to the submodules.

These reactors have various functions:

- The three phase units represent three dc voltage sources, connected in parallel. During operation, these voltages cannot be exactly equal, resulting in circulating currents between the three phase units. The valve reactors limit these circulating currents and enable the control of them.

- Limit the valve short circuit current.
- Contribute to the interface impedance between the converter and the ac network.

3.2.6 VSC DC Capacitors

VSC dc capacitors serve the purpose as energy storage in a VSC. Their capacitance will have a direct impact on dc side ripple levels as well as on the converter dynamic performance. In addition to stabilizing the dc voltage, the VSC dc capacitor is also capable of filtering high frequency current harmonic.

In case of high voltage dc capacitors series connection of capacitor units are required. In order to operate safely a uniform voltage distribution across VSC dc capacitor units and elements must be ensured. Typically this is achieved by grading resistors.

3.2.7 Submodule DC Capacitors

In principle, the function of the submodule dc capacitors for MMC technology is similar to that of the VSC dc capacitors.

3.2.8 Other Components

3.2.8.1 Radio frequency interference filter

The frequency range to control with radio frequency filters is 150kHz-10MHz.

For the harmonics generation of voltage source converters in this frequency range, regardless of valve topology, the decisive parameters are voltage drop and rise time during valve switching and the switching frequency. These parameters have to be taken into consideration for the RFI filter design.

Stray capacitances and stray inductances within the valve structure may lead to internal resonances within the valve, which has to be taken into consideration during the valve design regardless of valve topology. And it may, therefore, be necessary to integrate additional damping circuits within the valve.

In addition, internal oscillations within the IGBTs should be considered, as this is a known phenomenon that may occur. The typical frequency range of interest is 100MHz-1GHz depending on physical dimension of the IGBT. Any oscillations need to be identified and remedied.

To prevent HF harmonics in the converter valves spreading to the switchyard and the connected ac network, a RFI filter can be introduced on the ac side as close as possible to the valve area. The RFI filter can consist of a low inductance capacitor connected between the ac bus and earth and an ac line filter reactor. Radio frequency filters are not needed on the dc side if the transmission consists of a shielded dc cable.

If power line carrier communication is used nearby in the connected ac network, normally in the frequency range 30kHz-500kHz, additional power line carrier harmonics filters may be required.

Requirements for equipment included within the RFI filters and power line carrier harmonics filters are covered by international standards.

3.2.8.2 Substation circuit breaker

Figure 3.11 shows the ac circuits normally applied for a VSC converter.

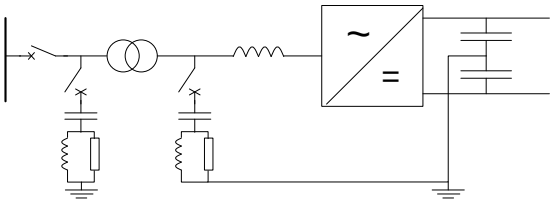
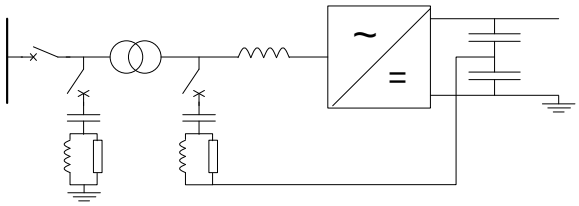


Figure 3.11 a). Circuit breakers for balanced VSC including ac filter breaker (if any)



b) Circuit breakers for asymmetric monopolar VSC converter including ac filter breaker (if any)

The VSC substation ac circuit breaker is used to connect and disconnect the VSC converter and the ac filters to and from the ac system. There are no special requirements compared to what is used for normal circuit breaker applications as ordinary device, as illustrated in Figure 3.11 a) and b).

AC circuit breakers may be used (project specific) to connect and disconnect filter branches.

AC circuit breakers used for connection and disconnection of filters located on the valve side of the interface transformer may be exposed to dc voltage to ground, in case of an asymmetric monopolar VSC converter, as illustrated in Figure 3.11 b). However, the breaker chambers are not exposed to any abnormal stress.

3.2.8.3 AC/dc filter

For classical HVDC converters the characteristic harmonics are significant and well defined. The amplitude of the high frequency harmonics is very small compared to the characteristic harmonic. For VSC-HVDC converters, the situation is much more complex. There are no well defined characteristic harmonics. The harmonic spectra depend significantly on several parameters such as switching frequency (pulse number), PWM pattern, number of converter voltage levels etc. However the generation of certain ac harmonics can be suppressed by the choice of the PWM characteristic leaving specific harmonics for which filters can be designed.

The function of the ac filters is to suppress ac side harmonics, when needed, to an acceptable level. Correspondingly, the function of the dc filters is to suppress dc side harmonics, when needed, to an acceptable level.

Acceptable level for ac side harmonics is typically determined by local grid guidelines and other recommendations. For a comprehensive discussion on ac filters see CIGRE Technical Brochure No.139[3-4]..

Acceptable levels for dc side harmonics are almost solely determined by the possibility of the dc transmission causing telephone interference.

3.2.8.4 DC transmission line

As for classical HVDC, transmission systems with VSCs can use both cables and overhead transmission lines. The main difference is that VSC transmission lines are not exposed to polarity reversals. Cables often have

less impact on the environment than overhead transmission lines and they are not exposed to direct lightning strikes. For VSC overhead transmission there should be provisions for temporary shut down and restarts in order to clear temporary dc line faults, which are much more frequent than permanent faults. However VSC cable transmission does not need temporary dc faults clearing capability as all cable faults are permanent faults.

3.2.8.5 Smoothing reactor

The purpose of the smoothing reactor is to reduce the harmonics on the dc transmission lines. This may be most important in case of overhead transmission lines. The inductance of the smoothing reactor in VSC-HVDC is small compared with those used for classical HVDC.

The smoothing reactor has practically no impact on the converter steady state stresses. However it may impact the dynamic stresses during faults and disturbances.

3.2.8.6 Common mode blocking reactor

The common mode blocking reactor, which is an optional part for dc side filtering, is designed to suppress the common mode component (or zero sequence components) of the dc side harmonic currents in VSC transmission lines. Harmonic currents flowing into a dc line of a bipolar long distance transmission scheme can be split up into different mode component currents, pole mode harmonic currents and common mode harmonic currents. Because the pole mode harmonic current components flow in the pole conductors in opposite direction, and the forward and return conductor of the transmission system are arranged in close proximity, the resulting electromagnetic field caused by the different mode component currents is comparatively small. While common mode component currents flow in the pole conductor into the same direction and may cause interference especially with telecommunication lines running nearby and in parallel to the dc transmission system. This justifies the use of a common mode blocking reactor.

Another advantage of a common mode reactor is its capability to reduce the zero sequence dc side harmonics current without impacting the dynamics for the main pole mode current loop. For some PWM pattern the zero sequence harmonics may be dominant. By reducing the zero sequence current the thermal loading of dc transmission cables and the cable screens will decrease. As the surge impedance of HVDC cables is quite low, the dc harmonic loading of the transmission cables might be significant if there is no dc side smoothing feature.

A common mode blocking reactor consists of two magnetically-coupled windings having the same self impedance and high common mode impedance and consequently common mode current is suppressed.

3.2.8.7 Grounding device

The grounding device as show in the Figure 2.10 is connected between the ac terminals and ground, providing a high impedance to ground for ac system frequency and low impedance for dc. It might consist of high inductive reactors. In case of using saturable reactors resistors can be connected in series for protection purpose.

3.3 PROTECTION SYSTEM

3.3.1 General

The purpose of the protection system is to cause a prompt removal of any element of the transmission system from service in case of a fault, e.g. when the transmission system suffers short-circuit or when it starts to operate in any abnormal manner that might cause damage or otherwise interfere with the effective operation of the rest of the system. The protection system is aided in this task by the ac circuit breakers, which will disconnect the ac network from the converters and are capable of de-energizing the interface transformer, thereby eliminating the direct current. The protection function settings are dimensioned with a margin to allow maximum stress for all acceptable conditions but the protection must act within the limits of component dimensioning.

Protections with impact on component testing of HVDC applications are described in this chapter.

3.3.2 AC Protections

3.3.2.1 AC Bus Abnormal Voltage Protection

The primary objective is to protect the equipment on the incoming ac bus from operating in abnormal voltage conditions.

The protection measures the voltage on the incoming ac bus and detects abnormal voltage levels. The protection zone includes all equipment connected to the incoming ac bus.

3.3.2.2 AC Bus Differential Protection

The primary objective is to detect phase-to-phase or phase to ground faults on the ac bus and to open the appropriate breakers to isolate the faulted part of the substation from the rest of the ac system.

The protection zone covers the phase reactors, the transformer valve side and the ac filter. The incoming currents entering and leaving the zone are measured and summed with proper signs. A sum deviating from zero indicates a fault within the zone. Saturation of the converter transformers if the neutral of the transformer is grounded have to be considered.

3.3.2.3 Transformer Overcurrent Protection

The primary objective is to protect the converter terminal including the transformer from excessive stresses during overcurrent conditions.

The protection zone covers the complete converter terminal including the transformer. A definite time stage is employed for Short Circuit Protection and an inverse time stage is employed as a general backup for the complete converter terminal.

3.3.2.4 Transformer Differential Protection

The primary objective is to detect internal transformer from internal earth faults and to trip the ac circuit

breaker in case a fault is detected.

The bushing CTs of the converter transformer limit the protection zone. The currents injecting and leaving the transformer are measured and summed with proper signs. A sum deviating from zero indicates a fault. Saturation of the converter transformers if the neutral of the transformer is grounded have to be considered.

3.3.2.5 Transformer Protective Relays

Given are a set of transformer protective relays commonly used in VSC-HVDC applications.

Interface transformer oil temperature indicator

The objective is to protect the interface transformer from overheating as a consequence of sustained operation during overload conditions or disturbances on the cooling equipment.

The oil temperature is measured at the top of the transformer.

Interface transformer winding temperature indicator

The objective is to protect the transformer from high winding temperature.

In the modern IED-based C/P systems more precise methods of calculating the windings temperatures can be used in accordance with IEC 60076-7.

Interface transformer gas detector relay

The primary objective is to detect incipient transformer failures but a Bucholtz relay could be used as a backup to the differential relay to detect winding short-circuits and internal flashover and initiate breaker tripping.

If the insulation of the winding is damaged, the intensity of the electric field at the point where the winding is defective may rise high enough so that gas is produced. High spot temperature may decompose oil and produce gas. Such hot spots might also occur in the transformer's core or in the LTC. The gas detector relay collects the gas and operates if a certain volume has been collected. A sudden pressure relay or a Bucholtz relay also operates when it detects a surge wave in the oil due to an internal flashover.

3.3.3 DC Protections

3.3.3.1 Converter Overcurrent Protection

The primary objective is to protect the converter (valves and phase reactors) in overcurrent conditions.

The current is measured outside the phase reactors with respect to the converter valves. The protection detects overcurrent at any type of disturbance when the control system fails to limit the current.

3.3.3.2 AC Terminal Short-circuit Protection

The primary objective is to prevent the IGBTs in the converter bridge from being exposed to excessive current especially in case of a short-circuit to ground inside the phase reactors on the ac terminal. In this case the VSC dc capacitors will discharge through the valves. The valve must be blocked in time before the current reaches the maximum turn-off level of the IGBTs.

3.3.3.3 Valve Short-circuit Protection

The primary objective is to prevent the IGBTs from being exposed to excessive power dissipation at high current, and to prevent switching at too high current.

The protection utilizes the current self limiting effect of the IGBTs. When short-circuit current is passing through the valve the on-state voltage of each IGBT will rise to a high level, which is sensed by the protection which immediately blocks the valves.

3.3.3.4 Valve Current Derivative Protection

The primary objective is to prevent the IGBTs from being exposed to excessive power dissipation at high current, and to prevent switching at too high current levels.

One measurement per valve is located on the positive and negative dc pole potential. The protection measures the current derivative in the valve. A high di/dt that prevails longer than the normal off/on-state transition indicates that short-circuit current flows through the valve and the IGBTs are immediately blocked.

3.3.3.5 DC Abnormal Voltage Protection

The primary objective is to protect the converter from overvoltage especially at high current and unbalanced voltage mainly in case of earth faults. The converter bridge, dc bus equipment and the dc cable are protected.

There is also an undervoltage function, which prevents operation at a dc voltage below the operating limit for the gate driving units.

The protection consists of three main functions:

- Pole-to-pole overvoltage protection compounded with the reactor current
- Pole differential voltage protection
- Pole undervoltage protection

3.3.3.6 Thermal Overload protection

The primary objective is to prevent the valves from overheating.

An algorithm is used to estimate the IGBT junction temperature. If the temperature exceeds the limit the IGBTs are immediately blocked.

3.3.3.7 Converter DC Differential Protection

The primary objective is to protect converter equipments between valve ac and dc wall bushing from ground

faults.

The incoming currents entering and leaving the dc bus are measured and summed with proper signs. A sum deviating from zero indicates a ground fault within the converter.

3.4 REFERENCES

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[3-2] Chokhawala, R., Danielsson, B., Amgquist, L., *Power Semiconductors in Transmission and Distribution Applications*. Proceedings of the 2001 International Symposium on Power Semiconductor Devices & ICs (ISPSD), Osaka: 3-10

[3-3] Cigré WG B4.37 *DC Transmission Using Voltage Sourced Converters*. Cigré Technical Brochure No. 269; 2005

[3-4] Cigré Working Group 14.30. *Guide to the specification and design evaluation of AC filters for HVDC systems.* Cigré Technical Brochure No. 139; 1999.

4. STRESSES UNDER STEADY-STATE OPERATION

4.1 GENERAL

Analysis of component stresses of the VSC transmission system under steady-state operation is important for component rating selection and for devising the appropriate type test levels. Voltage sourced converters may be arranged in many different topologies and may be controlled using different modulation methods, but the process of energy conversion is common. The power flow between the ac and dc side is defined by the line frequency voltage across the phase reactor. The active and reactive power can be controlled independently by varying the phase shift and amplitude of the converter's ac voltage [4-1].

Several factors impact the VSC transmission system component stresses under steady-state conditions. These are mainly operational state, topology, modulation strategy and equivalent reactance of the ac system, which is dependent on the characteristics of the ac system.

The converter is the key component of the VSC-HVDC transmission system. The VSC valve in topologies where the valve acts as a controlled switch withstands VSC dc capacitor voltage and ac bus current during the switching process. Especially, the dc voltage ripple is dependent on the VSC dc capacitor size and the ac current ripple is determined by the phase reactor's size. As for a two-level converter, the IGBT and the anti-parallel FWD in the upper and lower arm of one phase unit conduct current alternately, and only one IGBT or FWD conduct at any time. The typical 2-level valve voltage and current waveforms at normal operating state are shown in Figure 4.1.

The VSC valve in topologies where the valve acts like a controlled voltage source withstands step voltage and half ac bus current plus one third dc current. The IGBT, diode and submodule dc capacitor of a submodule is exposed to a line frequency current in the switching process and the resulting relative capacitor voltage ripple is higher.

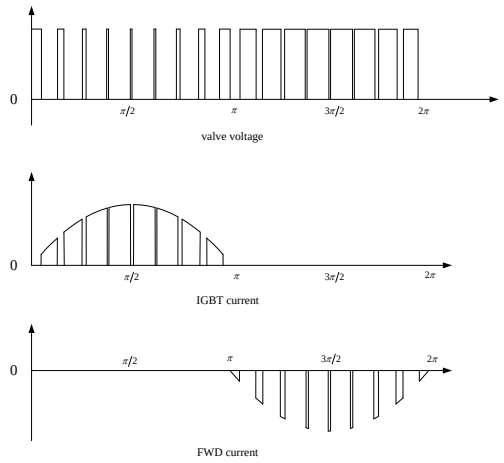

Figure 4.1 Typical 2-level VSC valve voltage &current waveform during normal operating state

Other important components are:

- VSC dc capacitor / submodule dc capacitor
- Phase reactor / valve reactor

- Interface transformer
- AC/dc harmonic filter

4.2 VALVE STRESS

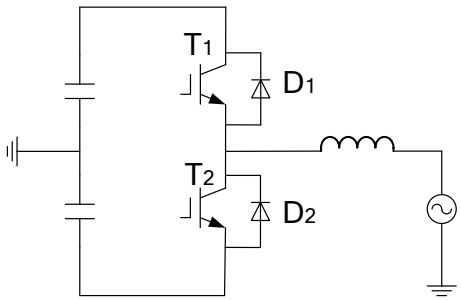

Figure 4.2 A phase unit of 2-level VSC

In topologies where the valve acts as a controlled switch, taking the typical 2-level VSC as an example (analysis of 3-level VSC is similar), this section describes the switching stresses of a VSC valve consisting of T_1, D_1, T_2 and D_2 (see Figure 4.2). Related to wave forms for one cycle as in Figure 4.1, Figure 4.3 shows the turn on and turn off process of IGBT T_1, when the ac phase current is in the direction going out of the valve ac terminal (equivalent to switching of T_2 when the ac phase current is coming in at the valve ac terminal) . Figure 4.4 shows the current and voltage of a FWD during the switching process.

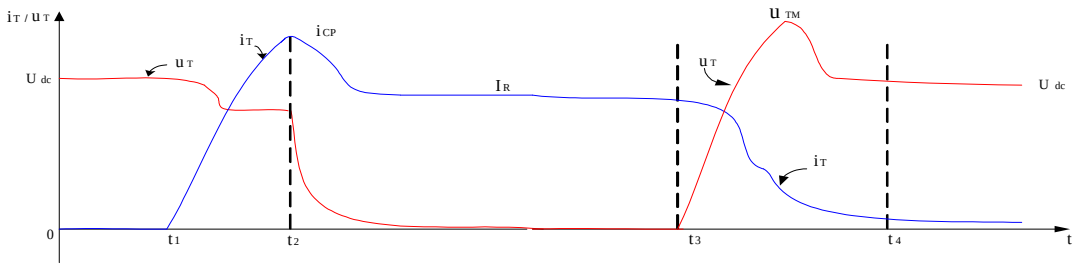

Figure 4.3 Switching process of IGBT

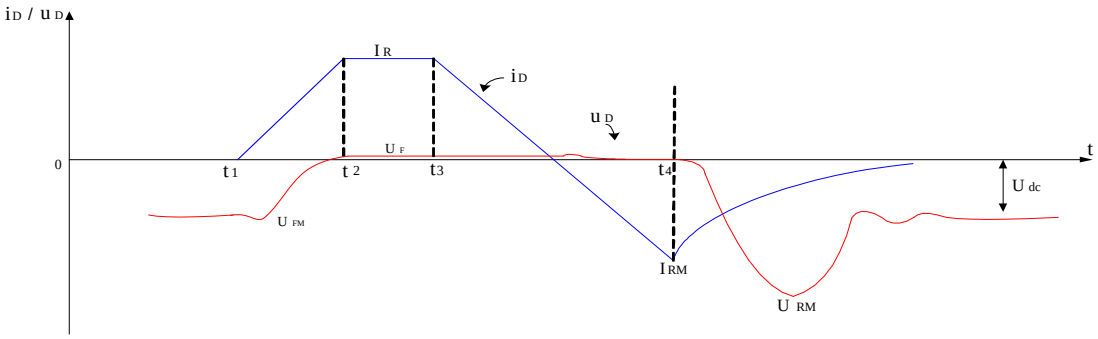

Figure 4.4 Switching process of FWD

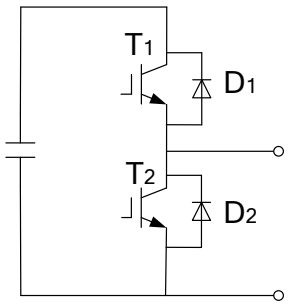

Figure 4.5 A submodule in topologies with valves acting like controlled voltage sources

Many descriptions of section 4.2 can also be applied to the half bridge semiconductor arrangement of one submodule in the topologies with valves acting like controlled voltage sources, in which the effects of direct series connection can be neglected and switching frequency is much lower. As shown by Figure 4.5 the circuit of a submodule constitutes a 2-level converter having the same type of commutations between IGBT and diodes as described above in this section. One difference is however the external terminal being a dc bus instead of the midpoint of the VSC dc capacitor. This implies a different loading of the switches T_1 D_1 and T_2 D_2. However, the detailed analysis of the switching stresses of VSC valves in the following sections remains valid in general for both types of valves.

4.2.1 IGBT Turn-on

In the case of MOS gate semiconductor devices such as IGBT, firing the device can be achieved by setting the gate potential positive. It takes time for the IGBT to respond to the gate potential. Figure 4.6 shows the voltage and current waveforms during an IGBT turn-on with an inductive load. It also shows the turn-on energy loss generated in the IGBT. For turning-on the IGBT, G-E voltage (V_{GE}) is biased from negative to positive. The rate of rise of V_{GE} is affected by the gate resistance and the capacitance between gate and emitter. After applying the positive gate voltage the C-E voltage (V_{CE}) at first decreases slightly followed by the collector current (I_C) flowing. After I_C almost reached its crest value, V_{CE} starts to fall almost exponentially. When discussing the turn-on process, there are two important characteristics, turn-on delay time, td(on) and rise time, tr. The definitions of these characteristics are shown in Figure 4.6. These values tend to become larger when the device voltage rating is higher. The typical td(on) value is 0.5 to 2 μs and the typical tr value is 0.3 to 2μs. Because VSC valve consists of a number of IGBTs connected in series the distribution of td(on) among the IGBTs may cause the turn-on over voltage to the late turn-on device. The td(on) distribution is usually controlled by means of gate signal adjustment, precise production control of the devices or others. The tr is important from the loss dissipation point of view. In the Figure 4.6 the turn-on energy loss, Eon is shown and Figure 4.6 clearly shows that it increases with the larger tr. Eon is typically 2 to 10 Joule.

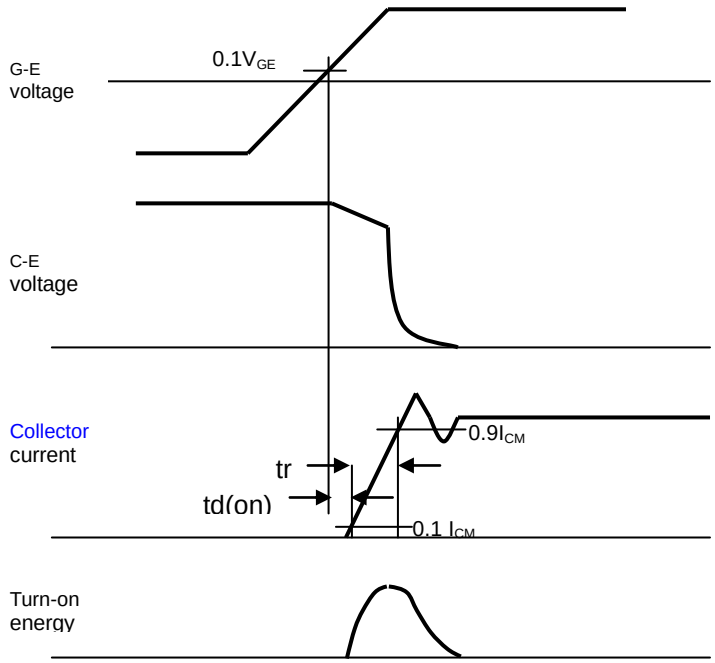

Figure 4.6 Waveforms during an IGBT turn-on with inductive load

During the turn-on of IGBT, due to the reverse recovery of FWD, current overshoot will occur in the conducting IGBT valve and certain voltage overshoot will occur in the blocked IGBT valve.

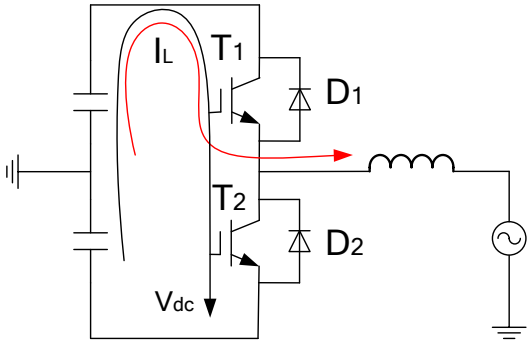

Figure 4.7 Turn-on of IGBT and turn-off of FWD

Take one bridge arm of the two-level converter for example, assuming the original state is such that D_2 is conducting and T_1 is blocked. Refer to Figure 4.7. Now issue a gating signal to T_1 to turn it on, then positive voltage will be added across D_2 and render it off. Therefore the turn-on process of IGBT actually includes the turn-off of the diode in the corresponding bridge arm. During this course, the direction and amplitude of load current almost remain unchanged; hence the sum of currents through IGBT and diode is constant. As a result the falling rate of the current through FWD can be controlled through regulation of the current rising rate of IGBT during its turn-on. Additionally shown in Figure 4.8 and Figure 4.9, due to the reverse recovery charge, Qrr of the p-n junction in FWD, a rather high reverse recovery voltage overshoot, U_{RM} and reverse recovery current, I_{RM} occur before the complete blocking [4-3]. Consequently T_1 will experience an obvious current overshoot during turn on but no voltage overshoot.

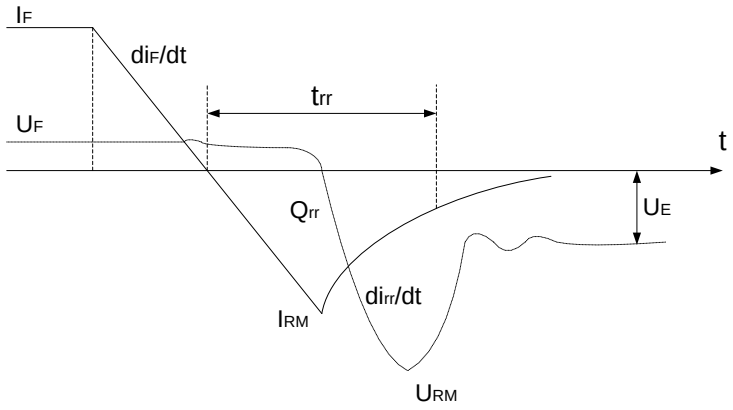

Figure 4.8 Reverse recovery during diode turn-off

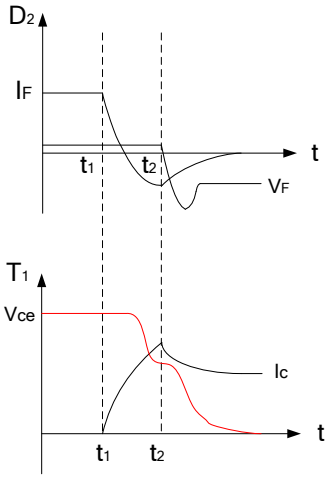

Figure 4.9 IGBT turn-on and the voltage and current changes during FWD turn-off

At the same time the existence of voltage overshoot during diode reverse recovery along with the stray inductance may generate voltage overshoot in T_2, which is a positive voltage to IGBT and has to be limited through appropriate measures to below the protection level of surge arrestor, otherwise may cause short-circuit of IGBT valve. Consideration should also be taken to the voltage and current stresses when T_2 is triggered again following the acting of surge arrestor under impulse voltage. The solutions mainly include adoption of optimized diode, matching of appropriate RC circuit, and reduction of valve arm inductance or current change rate during diode turn-off as far as possible during system integration.

4.2.2 IGBT Turn-off

As shown in Figure 4.10, when T_1 starts to turn off, the current direction remains the same, D_2 will turn on to provide a current path. Therefore through the regulation of IGBT turn-off rate, the current variation stress during diode turn-on can be controlled. The IGBT turn-off process actually covers the turn-on of the corresponding diode.

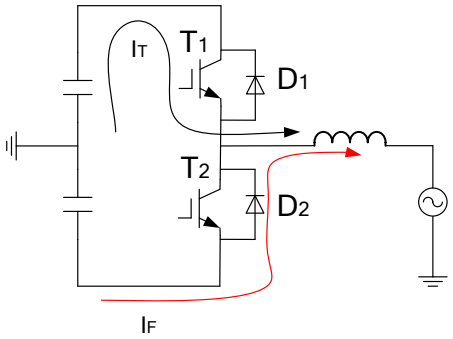

Figure 4.10 IGBT turn-off and FWD turn-on

During the turn off of IGBT, due to the stray inductance in the loop, an obvious voltage overshoot may occur to the blocked IGBT, while the current through FWD will not overshoot (refer to Figure 4.11).

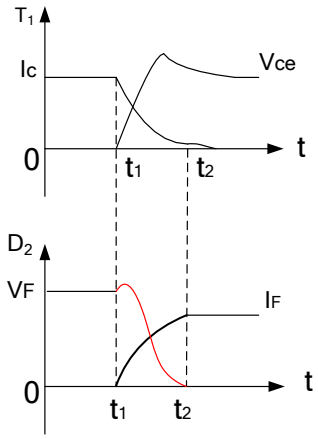

Figure 4.11 IGBT turn off and the change of current and voltage during FWD turn on

For the same reason, during IGBT turn off, the rising rate of voltage should be limited below certain value, and the current rising rate of corresponding diode should also be restricted through control of IGBT turn off rate. In fact various types of IGBT may generate rather different voltage overshoot, with optimally designed IGBT, optimization of tail current in particular (such as SPT type IGBT), it is possible to significantly reduce voltage overshoot during IGBT turn off [4-4].

4.2.3 On-state

VSC valve on-state refers to conduction of IGBT or FWD. If ac current is positive the on-state one is T_1 or D_2 according to the control pulse, and if ac current is negative the on-state one is T_2 or D_1 according to the control pulse. See Figure 4.7. Take the conduction of T_1 as an example, after T_1 fully turns on, i.e. FWD is blocked, the voltage of D_2 is dc voltage V_{dc} . The positive current flows through T_1 while the D_2 undertakes reverse voltage.

Generally speaking, the on-state voltage drop of the IGBT is higher than that of the FWD, and correspondingly the IGBT conduction loss is higher than that of the FWD. It is important to keep the forward

voltage drop consistent between IGBT level and FWD level as much as possible, because it is of greater significance to the loss equalization of IGBT/FWD level. Due to the high switching frequency of 1-2 kHz, switching loss of VSC valve that operates under PWM mode, is high and occupies a great proportion in the overall loss, while for multi-level converters that are at line frequency or low frequency working mode, the on-state loss and balance of IGBT and FWD are more important.

In the event of load increase, ac bus temporary undervoltage, or ac system short circuit, the current through IGBT is likely to increase, which in excess of certain level may cause IGBT temperature rise and damage, or even cause IGBT turn-off failure and bridge shoot-through if the current exceeds the IGBT maximum turn off current. Therefore appropriate measures should be taken to limit this current below the safety level.

4.2.4 Off-state

Off- state VSC valve blocks the dc voltage. The main losses considered as voltage-losses are caused by the leakage current.

Normally it is the VSC dc capacitor voltage which appears between the two terminals of the off-state VSC valve. When the control circuit does not work correctly, dc voltage may become greater than what IGBT or diode can withstand. Protection circuit must be designed adequately to avoid this unexpected voltage applied to the IGBT device in the VSC valve levels.

When the VSC valve is off-state, surge voltage from ac circuit must be considered and protected. Surge voltage from dc circuit (like dc cables or reactors outside the valve structure) usually needs not to be taken into account, because the large VSC dc capacitor clamps the surge voltage from the dc circuit.

At off-state, the voltage characteristics dependent on the temperature of IGBT and FWD is closely related to the security of the VSC valve, hence the maximum junction temperature of IGBT and FWD should be controlled within reasonable limit. On one hand, the voltage capability of the FWD is more sensitive to the junction temperature, so more consideration should be given to the FWD's thermal design. On the other hand, the IGBT is a voltage driven semiconductor and is more vulnerable to the effect of cosmic rays [4-5]. How to avoid the mis-firing of IGBT caused by rapid voltage change is another important issue for reliable blocking of VSC valve.

4.2.5 Short Time Over-Load

Short time over-load operation is not continuous but temporary. It is one of the issues for thermal design. So it is necessary to discuss the over-load level and its duration. For the IGBT, its maximum junction temperature and safe operating area (SOA) usually determine the operating limit for the device. The equipment must be designed to withstand the short time over-load operation under the worst case environmental conditions and after the maximum normal operating stress with worst case condition of the coolant.

4.3 INTERFACE TRANSFORMER

The additional stresses on converter transformers for LCC-HVDC and interface transformers for VSC-HVDC are the loading of current harmonics and the valve side voltage.

The harmonic loading depends on the characteristics of the converter (number of voltage levels combined with the switching pattern) and the location of the ac harmonic filters. If all ac filters are located on the valve side of the interface transformer, the transformer current harmonics will be very low. However, if some of the ac harmonic filters are located on the network side of the interface transformer, the transformer will be loaded with some harmonic current. In general terms, the harmonic current for VSC converter interface transformers is much lower than the harmonic current loading for LCC-HVDC converter transformers. Anyhow, from case to case it has to be evaluated if the current harmonics will impact the transformer design.

In a symmetric monopole VSC-HVDC scheme as shown in Figure 3.11 a) the valve side windings are not exposed to a dc voltage. However, in an asymmetric monopolar configuration as shown in Figure 3.11 b), the valve side winding are exposed to combined ac and dc voltage stress as is the case for a LCC converter transformer. However, in VSC-HVDC there is no dc voltage reversal.

In a symmetric monopole scheme the transformer neutral of a valve side Y-winding is impacted by the valve side zero sequence voltage. However, the zero sequence voltage does not normally increase the voltage stress on the transformer valve side phases. Furthermore the secondary winding voltage differs according to the grounding type of the valve side harmonic filters. If the high frequency filter branches are connected in Yn with high frequency grounding of the filter neutrals, the zero-sequence high frequency harmonic voltage will drop on the phase reactor, otherwise, zero-sequence high frequency harmonic voltage will drop on the secondary winding of the transformer directly. Therefore the design of valve side harmonic filters is important for the determination of the transformer stresses.

Anyhow, from case to case it has to be evaluated if the valve side voltage waveforms will impact the transformer design.

In topologies where the valve acts like a controlled voltage source, multi-level voltage of valve side approach sinusoid wave and the current through interface transformer is also sine-wave, so the normal interface transformer can be used.

4.4 VSC DC CAPACITOR

VSC dc capacitor banks are built up with units of dry-type self healing capacitor modules.

The decisive steady state stresses for VSC dc capacitors are the voltage stresses made up of the direct voltage component (U_d) with the superimposed ripple voltage, $U_d + \sqrt{2}\sum U_h$.

The harmonic current stresses, $\sqrt{\sum I_h^2}$.

Given the converter topology and PWM technique and assuming a constant direct voltage the decisive parameters for stationary harmonic stresses are the fundamental frequency current and converter power factor ($\cos\varphi$) together with the modulation index used to achieve the operating point.

Considering that the capacitor bank is subjected to a direct voltage a uniform voltage distribution across units and elements must be ensured. This is achieved through grading resistors.

The stray inductance of the VSC dc capacitor strongly influences the switching behaviour of the converter

valves. In particular a low stray inductance is required in order to obtain low switching losses.

In addition to steady state stresses, consideration has to be made for temporary overvoltage stresses that might occur during ac and / or dc side faults, see discussion in chapter 5.

4.5 SUBMODULE DC CAPACITOR

The submodules can be individually switched "off" or "on" depending on output voltage generation. In case the submodule is switched "off" the valve current does not pass the submodule dc capacitor and the capacitor current is zero. Whereas in case the submodule is switched "on" the full valve current is flowing through the capacitor. In the "on" state components of fundamental and low order currents have to be considered, see Figure 3.9. The current flow in the "on" state results in a significant ripple voltage of the submodule dc capacitors per power cycle. The average and RMS capacitor current stresses are calculated based on current contribution in the "on" state.

The stray inductance of the submodule dc capacitor strongly influences the switching behaviour of the associated semiconductors of the submodule.

4.6 PHASE REACTOR

Phase reactor located at the ac outlet of the converter is exposed to the voltage difference between the ac system and the converter terminals. The latter is a string of high and fast rising pulses. The voltage level number is determined by the converter topology and the pulse frequency is determined by the switching frequency. The typical phase reactor voltage is shown in Figure 4.12. The maximum step voltage on the valve side of the phase reactor voltage is twice the dc voltage U_d with a short overshoot related to the switching transients defined by the valve commutation loop inductance.

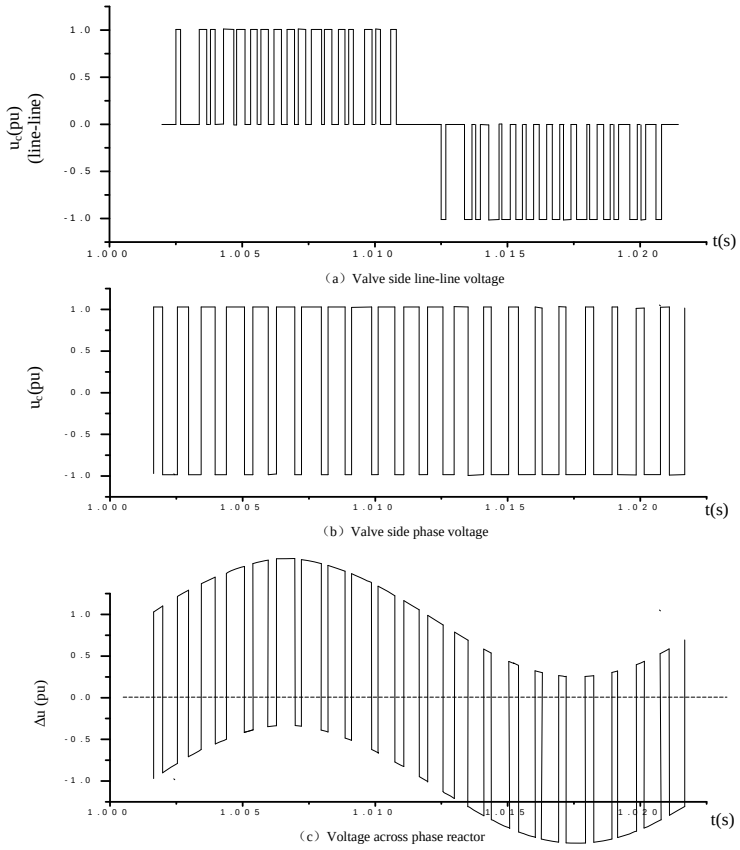

Figure 4.12 Phase reactor voltage about 2-level VSC

For different topologies, the peak value of the phase reactor's valve side voltage is identical, whereas they are different in the fundamental frequency voltage amplitude and characteristic harmonics. The reactor acts as a low-pass filter and thus the harmonic voltage component is reduced after the reactor, resulting in a sine voltage with ripple.

The voltage stress along the phase reactors of two level or three level VSC converters usually precludes the outdoor installation of the reactors. They must be installed indoors such that the level of pollution will be kept at a minimum.

In order to meet requirements for electromagnetic compatibility (EMC), phase reactors of two and three level converters must be enclosed in adequate shielding cages to mitigate the electromagnetic field emanating from the reactor. The cage may be configured either as a structure consisting of a number of conducting rings enclosing the reactors or as a complete metal housing. The shielding cage will impact the technical parameters of the reactor by lowering the inductance, increasing the losses and increasing the capacitance to ground as compared to free-field conditions.

After the phase reactor, harmonic current is eliminated, thus the ac current is the fundamental part with some smaller ripple, and the ripple should be restricted within allowed range by proper choice of equivalent reactance.

4.7 VALVE REACTOR

The current through the valve reactors is a superposition of a dc current and a nearly sinusoidal ac current. The amplitude of the harmonic current can be negligible. The dc component equals to one third of the dc current whereas the ac components is half of the ac current.

Depending on the location of the reactors relative to the valve, the insulation voltage to ground may be a dc voltage, an ac voltage or a superposition of both. As there are no special requirements regarding high frequency behavior, the reactors could be standard types.

4.8 SMOOTHING REACTOR

The current flowing through the smoothing reactor is the current in dc transmission line with superposition of harmonics which are quite small. The smoothing reactor is exposed to the pole dc voltage. However, there are no polarity reversals in VSC-HVDC.

4.9 RADIO FREQUENCY INTERFERENCE FILTER

The RFI filters are connected between the phase reactor and the transformer. They are predominantly subjected to fundamental frequency stresses, and no special considerations are required with regard to stresses under steady-state operation.

4.10 COMMON MODE BLOCKING REACTOR

The steady state stresses decisive for the design of a common mode blocking reactor are

- Direct Current
- Direct voltage
- Harmonic voltages across the Reactor
- Harmonic Currents

The common mode blocking reactor is exposed to the dc current with the dc side harmonic currents loaded.

An important factor regarding steady state stresses is that the common mode blocking reactor is exposed to both pole to ground and pole to pole dc voltage. However in VSC-HVDC there is no polarity reversal.

The longitudinal voltage stress of the common mode blocking reactor corresponds to the dc side common mode harmonic voltage.

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5. STRESSES AT FAULT AND DISTURBANCES

The chapter focuses on equipment stresses in system fault conditions and abnormal operating conditions. Fault mechanisms are illustrated, and then equipment electrical and thermal stresses under fault conditions and post-protection conditions are analyzed to provide some guidance for the selection of appropriate test methods.

5.1 AC SYSTEM FAULTS

5.1.1 General

As the interface transformer does not have an earthed neutral on both sides, it blocks the ac side zero sequence current from impacting the converter equipment and vice versa. Therefore, overvoltage on healthy phases at single phase-to-earth faults in a network with high zero sequence impedance will not be transferred to the valve side. Neither will the valve side dc voltage in a configuration as shown in Figure 5.23 stress the ac side of the interface transformer.

The valve control will prevent the valves from being exposed to excessive currents at any ac side fault. In addition, the valves will be blocked if the valve voltage or current is too high for proper operation.

At faults in a network leading to low ac voltage in one or more phases, the converter can not continue to operate during the fault through rapid reduction of the converter ac output voltage in order to obtain a current level within the converter's capability. In this process, the commutation in the faulty phase(s) may be temporarily blocked to protect the converter from over-current. Thus, at fault in the inverter network, the inverter may be temporarily blocked, which depending on the duration could result in temporary dc side overvoltages, as described in Section 5.3.6.

One essential characteristic of HVDC converters is that the converters shall work properly for all realistic ac side conditions, including faults, unbalances and phase shifts. If the conditions are outside the design parameters, the converters shall in all cases be safely taken out of service, temporarily or permanently by blocking the converters and/or tripping of the ac side breaker. It is a very essential task during the development and design stages to verify this characteristic.

The ac side faults impact the VSC converter in the same way, regardless of applied topology.

5.1.2 Excessive Fundamental Voltage Variations

Loss of load (load rejection) or loss of a shunt reactor may lead to fundamental frequency overvoltage. In the same way, loss of lines, shunt capacitors, generators or static Var equipment may lead to fundamental frequency undervoltage, unless it is compensated by reactive power support. One important feature of the VSC-HVDC converters is their capability to consume or generate reactive power to support the ac network voltage. As the converter controls the converter filter bus voltage, the voltage variations of that bus will be less than the variation of the network. The tap changer will help to control the voltage of the converter filter bus within its limits.

If the voltage variations are outside the design parameters for the converter it will be blocked and finally its ac breaker will be tripped. Anyhow, the control will prevent the converter from being overloaded.

5.1.3 AC Voltage Phase Unbalance

The ac networks are never perfectly symmetrical. There is always a small amount of negative sequence voltage present. The continuous negative sequence voltage is often 0.5-1.0 per cent of the positive sequence voltage during normal conditions. During abnormal network conditions the asymmetry is often 1-2 percent. This is a figure to be specified by the end user.

In some VSC topologies the negative sequence voltage will result in a second harmonic voltage on the dc side which will cause a small second harmonic current on the dc side and a corresponding positive sequence third harmonic current on the converter ac side.

During unbalanced ac systems faults such as single phase-to-earth and phase-to-phase faults, the negative sequence voltage will be much higher, in the order of 30-50 percent of the normal positive voltage. Especially if there is a resonance between the filters and the ac network for the third harmonic, it will impose stresses on arresters and filter components. Severe ac side faults will result in blocking of the valves during the faults and the valves are protected by the valve side arresters. Consequently, the valves are not exposed to excessive stresses.

In order to properly coordinate the converter protections with the ac system protections, it is important that the end user should specify the negative sequence voltage amplitude versus duration taking into consideration the characteristics of the ac system protections. The converter equipment is rated for the specified unbalance conditions and the converter is provided with protections that will take the converter out of operation if the specified conditions are exceeded.

Besides, the converter protection should not trip in the event of undervoltage within the specified ac network fault clearance time.

In topologies with valves acting like controllable voltage sources, the unbalance current may cause the valve bridge current unbalance, both dc and ac components. In these systems the control system must be designed to suppress circulating current between phases and voltage unbalance between the valve bridges. For specified fault scenarios, the converter must not be blocked and tripped, in order to support the ac system. That is, the converter should have certain fault ride-through capability.

VSC topologies with valves acting like voltage sources are robust to unbalanced ac networks due to the individual voltage and energy flow control in each phase. However, grid code requirements can have an influence on the converter design, such as number of VSC valve levels.

5.1.4 AC Voltage Phase Shift

All events causing ac voltage variations will generally also cause ac voltage phase shifts. The worst case is the fault cases discussed in Section 5.1.3, as unsymmetrical faults may cause large unsymmetrical phase shifts. The VSC converter control is designed for dealing with the combination of voltage variations and phase shifts during both symmetrical and unsymmetrical faults.

All events resulting in a change of the active power flow result in symmetrical ac voltage phase shifts. Thus, the load rejection cases discussed in section 5.1.2 will in most cases result in both ac voltage variations and

phase shift. Even sudden loss of generation may result in ac voltage variation and ac voltage phase shift. Depending on the event and the ac network conditions, the voltage variation or the ac voltage phase shift may be most pronounced.

AC voltage phase shifts, combined with minor voltage variations, will initially cause a change in the converter active power flow, which will be quickly corrected by the active power control.

5.1.5 Lightning Overvoltage

A direct lightning strike may have amplitude of 100-200 kA with a rise time of a few µs, which is a magnitude higher than what an ordinary arrester can take. Therefore, all electrical substation installations are protected against a direct lightning strike by lightning protection systems such as lightning masts or shield wires. However, all outdoor installations are exposed to secondary lightning strikes with much lower current magnitudes. The arresters in the converter have to be designed and located with consideration this possibility of a secondary lightning strike on any outdoor bus or an incoming surge from a lightning strike to a line close to the station.

An additional secondary effect of a direct lightning strike is the local potential rise of the earthing grid, connected to the bottom of the lightning mast exposed to a lightning strike. Even if not connected with wires, the earth mat will be connected by the lightning current channels if located nearby the lightning mast. That local potential rise of the earth mat will introduce surge current in cables and cable screens that might disturb the control equipment. This is an important part of the EMI design of the converter and the substation.

With a proper design of the substation lightning protection system, the worst lightning strikes are the ones entering the substation via the incoming ac or dc lines. Considering the limited voltage withstanding capability of the line insulation, the amplitude of the lightning strike current is limited to 5-20 kA, depending on the voltage level. However, the steepness is high and so is the voltage rise. As a result, an arrester will only protect equipment located close to it. The maximum voltage surge amplitude increases with the distance from the arrester, the so called distance effect. Correspondingly, the arresters shall be located close to the equipment they are supposed to protect, such as the interface transformer. Lightning strikes from incoming ac lines will not impose any significant stress on the valve side of the interface transformer. Anyhow, the converter ac filter bus is protected by arresters.

The VSC valves are properly located and well protected by capacitors and reactors on both the ac and the dc side. Therefore, stresses due to external lightning are of no concern for IGBTs and FWDs regardless of topology. For all topologies the significant fast transient stresses are due to valve commutations.

5.1.6 Switching Overvoltage

The normal event related to switching overvoltage is the connection of an open ended line or connection of equipment. However, the worst switching overvoltage event for a converter installation is the clearance of an ac side fault. And the worst condition is the clearance of a solid three phase-to-earth fault when the post-fault ac network is weak. The reasons are:

- At the fault clearance the converter will be blocked, which result in a load rejection overvoltage.
- The transformers may be saturated as the fault clearance event may be in opposite phase to the

voltage break down at the fault, i.e. the recovery voltage will not be synchronized with transformer remanence. The saturated transformer will inject low order current harmonics into the system.

- The charging of the discharged filter capacitors (if any) via the inductive network will result in voltage overshoots.

- Resonance between capacitors and the network may worsen the overvoltage.

This case is decisive for the arresters located on the ac side of the converter, both in regard to energy dissipation and coordination current. It may be decisive also for some of the arresters on the dc side of the interface transformer, especially the one on the filter bus.

The duration of the combination of switching and resonance overvoltage is one to three cycles. The ac network will provide damping for the overshoots. At the restart of the converter immediately after the fault clearance, the load rejection overvoltage is eliminated. Beside, operation of the VSC converters stabilises the voltage waveform.

As the dc line is charged and the phase reactors are located between the converter filter bus and the valves, ， the valves are not exposed to any significant stresses at ac network fault clearance. The valves are in any case protected by the arresters. The valve reactor plays the same role as the phase reactor.

5.1.7 Resonance Overvoltage Due to Transformer Energization

In the beginning of the seventies severe overvoltage was reported at transformer energization in a converter station located in a remote generation area with very small amount of local load [5-3], [5-4]. The equivalent inductance of the saturated transformer varies with the saturated level. Consequently, as the saturation event remains in order of seconds, the circuit is sooner or later tuned to exact resonance with the converter filters for the current harmonics from the saturated transformer. As only generators with step-up transformers constituted the ac network, its q-value was very high. The consequence was overstress of ac bus arresters.

No such high overvoltage has been reported from meshed networks with connected loads.

The remedial action at that time was to provide the transformer breakers with high resistive pre-insertion resistors. Synchronized closing is an alternative solution.

It is recommended that breakers for large transformers located electrically close to installation of large capacitor banks, like the HVDC ac filters, be provided with pre-insertion resistors or synchronized closing. Even if the arrestors are likely to survive a transformer energization without those measures applied, the voltage distortion will be very significant.

5.1.8 Post-fault Recovery

The primary and urgent objective of the VSC converter at post-fault recover is to support the ac voltage control, and bring the ac voltage within the specified limits. Although very important, to restore the power transmission is a secondary objective but not as urgent as the ac system voltage stabilisation.

Besides, ac network faults almost always mean loss of a transmission line. Consequently, the post fault power

transmission may be restricted to a lower value. Even if it is possible to restore the power transmission to the pre-fault level, the restoration should be smooth enough for the ac network voltage controllers to adapt to the new situation.

Utilization of frequency damping control will prevent the post-fault restoration of the power transmission from worsening the phase angle swings in the ac network, which are primarily caused by the ac network fault.

5.1.9 Summary of Equipment Stresses at AC Side Faults

The lightning transients will determine the number and location of the arresters, especially the arresters at the ac side of the interface transformer.

Switching and resonance overvoltage at fault clearance will determine the coordination current and energy dissipation requirements for the arresters, mainly on the ac side of the interface transformer. However, the converters side arresters have to be checked as well.

The converter controls its own currents in the valves and phase reactor. Thus, the ac side faults do not impose any significant stresses on the valves or phase reactors. (The converted dc side capacitance will not be discharged during the ac side faults. Hence there will be no large recharge currents through the diodes.) Blocking an inverter connected to the end of a line will raise the voltage on the line and cause overvoltage but the arresters clip the voltage.

Breakers for large transformers located electrically close to large capacitor banks should be provided with pre-insertion resistors or synchronized closing to avoid severe distortion at transformer energization.

5.2 Internal Faults in the VSC Substation

5.2.1 Internal AC Bus Fault

Converter station internal structures including converters and phase reactors etc. are in most cases installed under well defined conditions, which makes the probability of internal ac bus fault relatively low.

Internal ac bus faults are usually caused by insulation failure somewhere between transformer secondary winding and converter valves or failure of devices connected to the ac bus (e.g. ac filter). The faults in the ac bus between transformer and converter shall be considered as permanent because of the severity and the low fault probability, which demands the converter to be blocked and trip the ac circuit breakers.

Consequences of an internal ac bus fault mainly depend on:

- Type and location of the fault which define the fault severity and characteristic
- The main circuit arrangement defining the fault current paths with its impedances
- Transformer winding configuration and grounding type.

In both topologies of VSC-HVDC a high-impedance connection of the ac bus to ground is typical. However, an internal ac bus fault results in overvoltages and possibly overcurrents as well. The associated

over-voltages are limited by ac and dc arresters.

5.2.1.1 The filter bus

At a single phase-to-ground fault on the converter ac filter bus causes the voltage of the healthy phases to rise to the phase-to-phase voltage level. As a first approximation, that will lift the voltage of both poles to a level of 1.73 times the normal voltage due to peak rectifications via the FWDs. Figure 5.1 indicates the two charging paths.

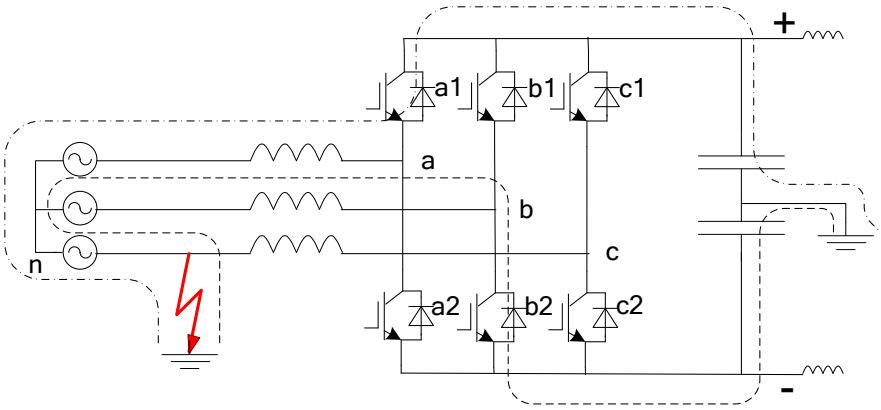

Figure 5.1 Charging paths at a single phase to earth fault

The complete converter including the valves, the dc transmission line and the converter in the other station will then be exposed to overvoltage. Arresters will limit the overvoltages resulting in significant arrester stresses. The faulty converter will be quickly blocked by the overvoltage and earth fault protections. However, the overvoltage and arrester currents are driven from the ac side via the interface transformer until the converter ac breaker is tripped.

The other station will also be blocked by its overvoltage protection.

Since the fault is a single phase-to-ground fault, there will be no short circuit currents. Furthermore, as the fault is located on the network side of the phase reactors, the current derivative at turned on of the IGBTs in the faulty phase will be limited. Thus, there will be no significant IGBT current stress.

Both converter topologies will suffer overvoltages in about the same way but no severe overcurrent at single-phase-to ground faults on the network side of the phase and valve reactors respectively. The overcurrents can be limited by the reactors. In this case the converter can be blocked with nominal turn-off currents.

If a solid grounding methodology is adopted, a single phase to earth fault will result in short circuit currents. However, the overvoltages will be less.

For other fault types, e.g. phase-to-phase fault, the overcurrent stress should be considered but there should be no obvious overvoltage.

5.2.1.2 The converter bus

A fault short circuit of the converter bus to ground is much severer because of the direct discharging of the VSC dc capacitors via the IGBTs. The discharging path is illustrated in Figure 5.2 and Figure 5.3.

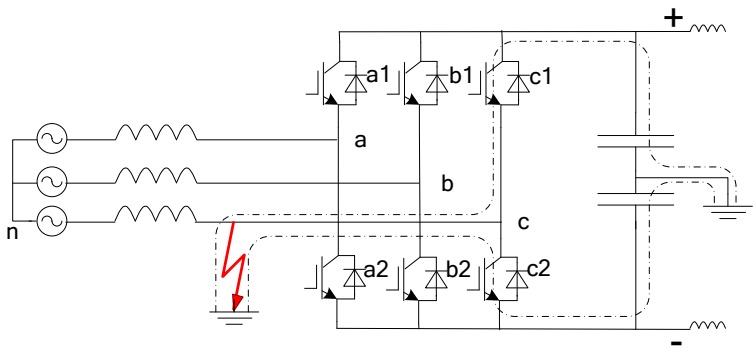

Figure 5.2 Discharge path through the IGBT single-phase to ground fault

The rise of the overcurrent in the faulty phase is very high and is determined by the stray inductance of the discharge path. Without action the current may quickly rise above the switch-off capability of the IGBTs. One possibility to cope with such internal faults is to use the self-limiting effect of IGBTs in case of a short circuit and turn off the short circuit current. The self-limiting effect is combined with very fast acting valve short circuit protection.

The overvoltage mechanism for this fault will be the same as that for a single-phase to ground fault on the ac filter bus as discussed above.

Although the discharge current path is not exactly the same in the topologies used for VSC-HVDC, the principles and measures for dealing with internal faults are very similar.

Under the very rare circumstance of a phase-to-phase short circuit, there will be no overvoltage. However, the interface transformer and the phase/valve reactors will be exposed to short circuit current. The current path is indicated in Figure 5.3.

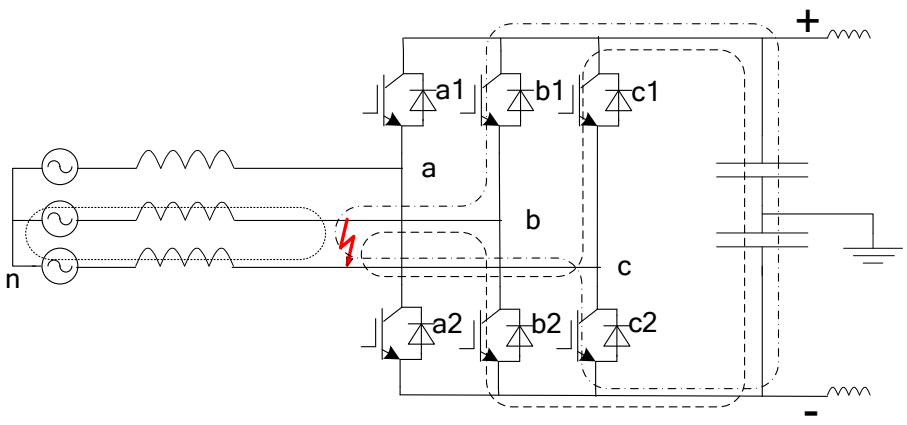

Figure 5.3 Discharge paths at a phase to phase fault

The possibility for fast capacitive discharge of the converter or valve capacitors is similar to the described case with single-phase to ground fault. The discharger loops are indicated in the right part of Figure 5.3. The measures for preventing too large IGBT currents are the same as described above for single-phase to ground faults.

5.2.1.3 Topologies with valves acting like controlled voltage sources

In the topologies with valves acting like controlled voltage sources, a high-impedance connection of the ac bus to ground is typical; there is no further solid grounding within the dc circuit. However, an internal ac bus fault also results in overcurrents. In many cases， the overcurrents can be limited by valve reactors. Then the converter can be blocked at nominal turn-off currents and the station can be tripped.

However, there are also fault scenarios where the valve reactors do not limit the rise of fault current. Such a failure is shown in Figure 5.4. In that case, the upper valve of the phase with fault represents a voltage source. The dc cable with positive voltage represents a capacitor with a different voltage level. This results in fault current, not flowing through a valve reactor. Two measures can handle that failure mode:

DC reactors as shown in the following figure to limit the fault current and the rate of rise in order to turn off the fault current within the SOA of the IGBTs. Alternatively the valve reactors can be placed on the dc terminals side of each valve.

Turn off the fault current by the IGBTs, which is in the first microseconds limited by the limitation function of the IGBTs in case of short circuit.

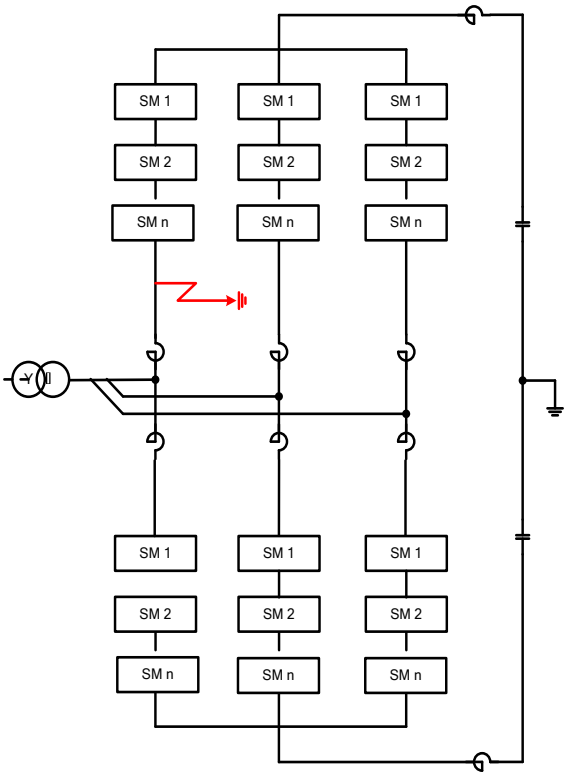

Figure 5.4 Valve reactor valve side grounding fault

Typically, at a single phase-to-ground fault on the internal ac bus, the voltage of the healthy phases will rise to phase-to-phase voltage level. The associated over-voltages are limited by ac and dc arresters.

5.2.2 DC Bus Fault

A converter pole bus-to-ground fault as shown in Figure 5.5 can be a result of an insulation failure on the connection between the dc terminal of a valve and the dc link connection. Since that fault is severe for the whole system, the converter has to be blocked and the system has to be tripped immediately after detection of the fault.

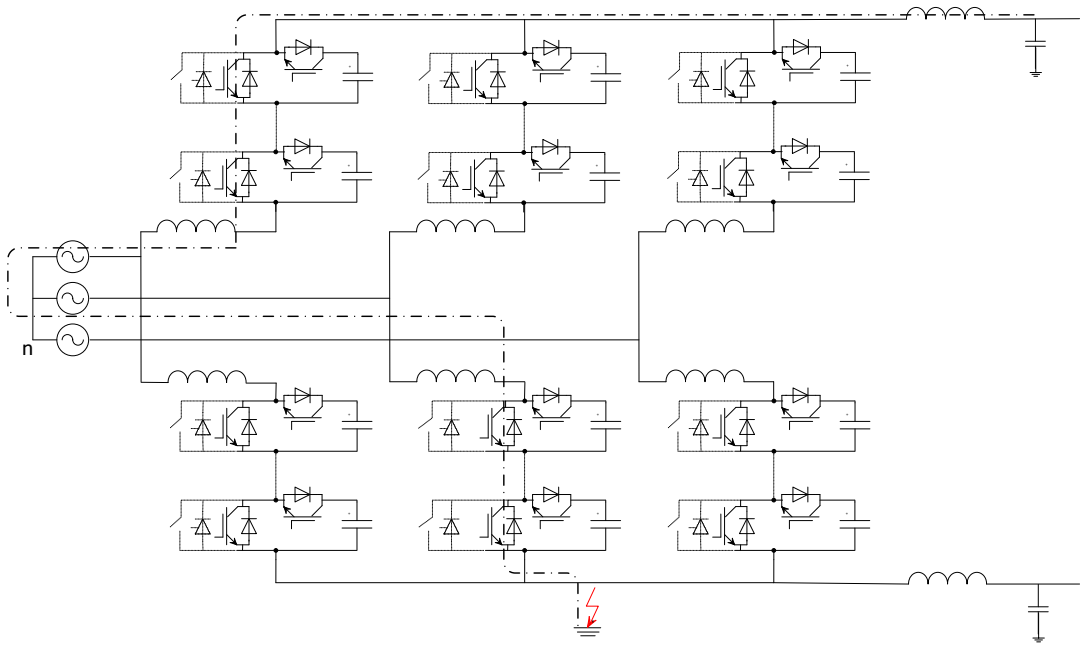

Figure 5.5 DC bus fault at a symmetric monopole configuration at a topology with the valves acting like controlled voltage sources.

The transient valve voltages and valve currents depend on the grounding philosophy of the scheme. Two examples with different stresses are discussed below.

5.2.2.1 Symmetric monopole configuration

In case of a symmetric monopole configuration ground fault on one pole will lift the other pole to about twice the dc voltage. The overvoltage will be limited by the arresters on the pole bus and on the converter filter bus. The path for charging the healthy pole via the FWDs is indicated in Figure 5.6 .for a topology where the valves act like controllable voltage sources. Figure 5.6 shows the corresponding path for the topology where the valves act as controllable switches. For this configuration, the converter capacitor of the faulty pole is discharged through the pole to ground fault. That discharge path is indicated as a dashed line in Figure 5.6.

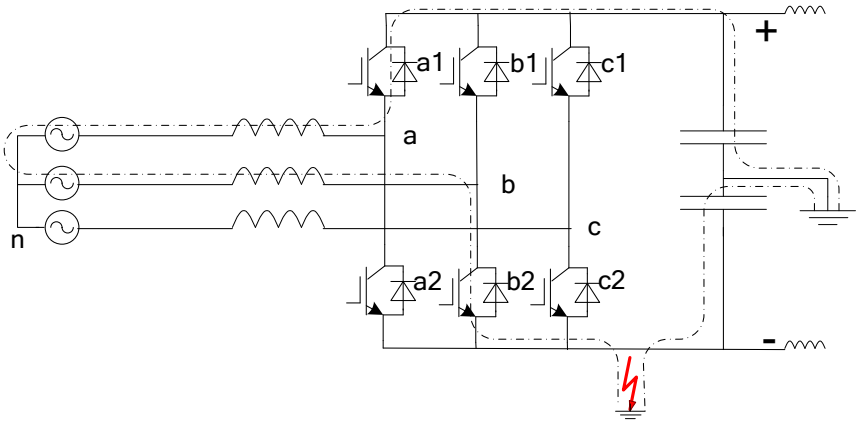

Figure 5.6 DC bus fault at a symmetric monopole configuration at a topology with the valves acting as controlled switches

For both topologies the healthy pole bus and the ac phases will be exposed to overvoltage limited by the arresters. The FWDs will be exposed to the charging currents only. Furthermore, there will be no overvoltage across the valves. However, the valve insulation to earth will also be stressed by the overvoltage. The valve side of the interface transformer will be temporarily exposed to dc voltage.

Due to the overvoltage on the healthy pole, the converters of both stations have to be quickly blocked and the converters ac breakers have to be tripped.

5.2.2.2 Asymmetric monopolar system with grounded dc neutral

In case of an asymmetric monopole concept, i.e. one dc terminal is grounded or held to a medium voltage potential, a high voltage dc bus fault has a similar effect as a short circuit between the two dc terminals. The fault current paths for the two topologies are shown in Figure 5.7 and Figure 5.8.

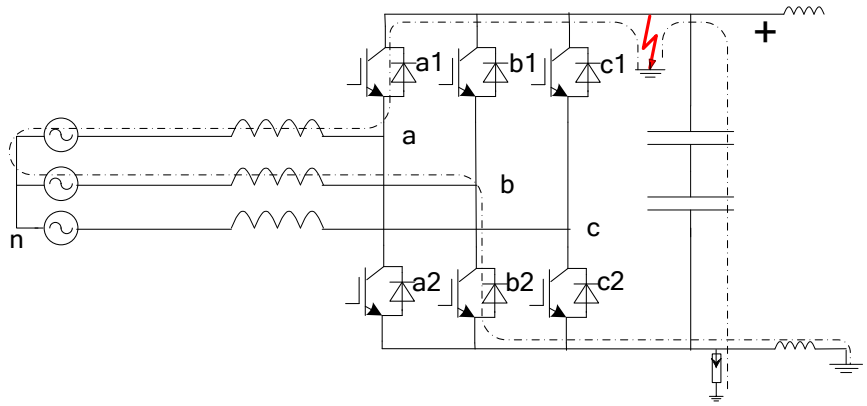

Figure 5.7 DC bus fault at an asymmetric monopolar configuration at a topology with the valves acting as controlled switches

In the topology where the valves act as controllable switches the FWDs will be exposed to short circuit current fed from the ac side until the converter ac breaker is tripped. One of the paths for the short circuit

current is shown in Figure 5.7. The converter capacitors will be discharged through the fault and the arrester protects the neutral bus of the converter, as indicated in Figure 5.7. The inductance of the electrode line will limit the discharge through the electrode. The IGBTs will not be exposed to any abnormal current stress in this configuration.

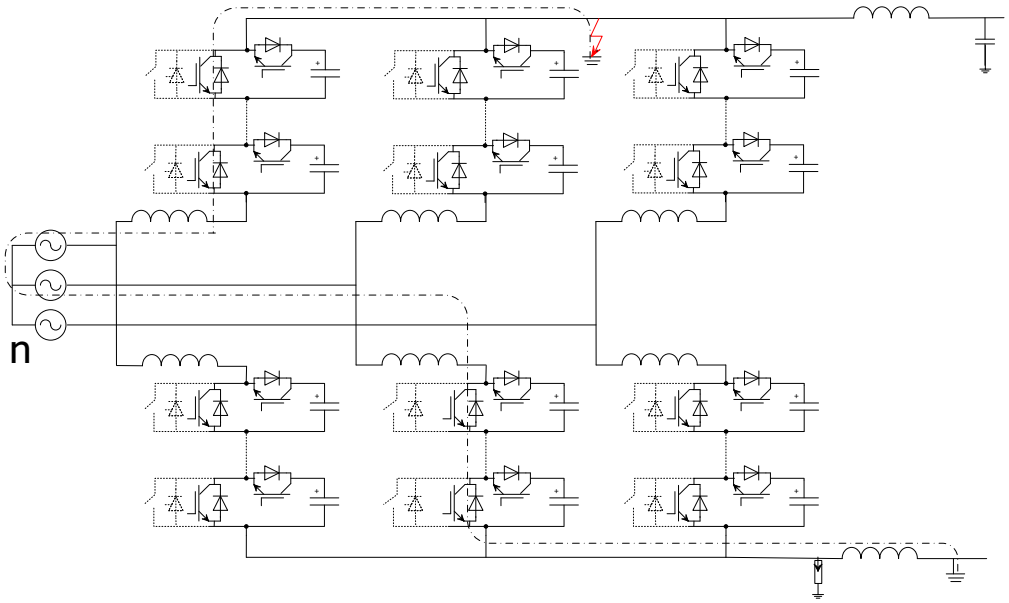

Figure 5.8 DC bus fault at an asymmetric monopolar configuration at a topology with the valves acting like controlled voltage sources

In the topology where the valves act like controllable voltage sources, the FWDs will be also exposed to short circuit current fed by the ac side until the converter ac breaker is tripped. One of the short circuit current paths is shown in Figure 5.8. If the FWDs cannot withstand the current stresses until the converter ac breaker is tripped, they may be by-passed by protecting thyristors, as indicated in Figure 5.8. To prevent the valve capacitors from being discharged in this topology, the IGBTs have to be immediately blocked. However, the derivative of the discharge current is limited by the valve reactor and the IGBTs will have no severe stresses.

5.2.3 Thus, for both topologies, the converter's ac circuit breaker has to be immediately tripped to avoid overstressing the FWDs. Depending on the current capability of the FWDs, additional protecting devices such as by-pass thyristors may be needed. In addition, the remote converter station has to be tripped. The remote converter will see the fault as a dc transmission line fault, which is further discussed in Section 5.3.VSC Valve Failure

For VSC valves, in addition to the number of series-connected VSC valve levels that have to sustain the converter voltage rating, each single valve in a VSC transmission scheme must include a few redundant VSC valve levels to enable continued operation in case of failure of an individual component shown in Figure 5.9. (In case of topologies with valves acting like controlled voltage sources, redundant submodules are needed).

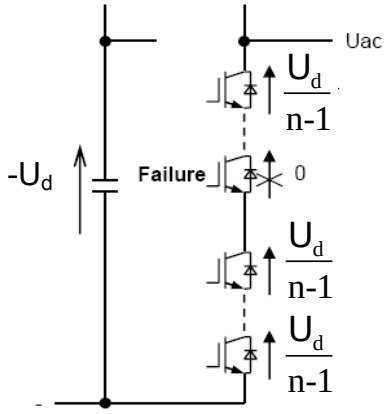

Figure 5.9 Short circuit mode failure of single power device in series connected VSC unit

Therefore, a faulty IGBT or FWD (or submodule) must not result in an open circuit of the respective VSC valve level, as the valve must continue operating with the remaining healthy VSC valve levels. Instead, the faulty valve level must enter into a short-circuit failure mode and be capable of conducting current until it can be removed and replaced, e.g., during a scheduled maintenance period.

There are two possibilities to realize that requirement:

a) Capability of the semiconductor device itself.

b) Bypass Switch which is closed in case of a faulty VSC valve level.

In case a) the capability of short-circuit failure mode of the IGBT (SCFM) operation is very critical for series-connected IGBTs without bypass path, and must be verified by appropriate tests under conditions that are relevant for a particular application. A specially developed package is used for IGBTs for VSC transmission and other similar high-voltage applications, in which the semiconductor devices must have the capability of riding through short circuits. These are press pack designs rather than the module design used for industrial and traction, low-voltage applications. Standard IGBT modules do not have the required SCFM behavior, as they normally use bond wires that open the circuit upon failure.

In case b) high speed and high reliable bypass switches can be used to make standard IGBTs also suitable in HVDC applications. To ensure reliable conducting capability, based on the circuit configuration, the VSC valve level may be equipped with a short-circuit path of its output, which will be closed automatically when a failure happens inside the VSC valve level circuit as shown in Figure 5.10. That gives the redundancy to the series connected VSC valve levels.

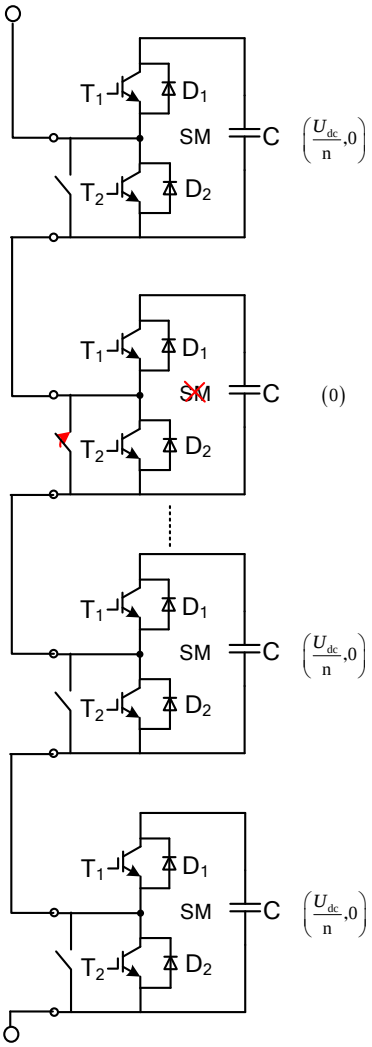

Figure 5.10 Bypass switch attached to ac output of VSC valve level

IGBT device which contains multi-chip, wire-bonding that will melt as a result of the fault currents will be destroyed by the fault currents and the chip will fail. Open-mode of wire-bonding causes internal flash over which damages the IGBT package and/or other materials outside the IGBT packages. It is therefore necessary to take measures to avoid cascading failures of neighboring VSC valve levels, and to detect the Open-mode failure before the severe damage occurs.

5.2.3.1 Short circuit mode failure

Short circuit mode failure may be caused by the failure of IGBT (or FWD) device, VSC valve level, or phase unit. Cause of the failure may be occasional random failure of the IGBT device itself, misfiring of control circuit, break down of a structural component of VSC valve, flash over outside the VSC valve, and so on.

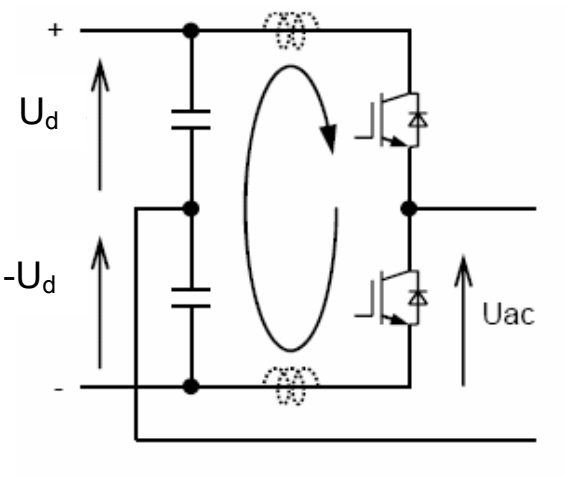

Figure 5.11 Description of VSC Valve failure

If the phase unit consists of one VSC valve level, short circuit failure occurs as follows. After the failure of conducting IGBT device or VSC valve level, and when the opposite side phase turns on, or, when the non conducting IGBT device fails and opposite side is conducting current, both upper and lower phase circuit will be in the conducting state resulting in a short circuit failure. Both terminals of the VSC dc capacitors will be short circuited by the failed phase unit as shown in Figure 5.11.

To minimize the switching losses in IGBTs and diodes, the dc circuit including dc capacitor and dc bus, is designed to minimize the loop inductance, which means a high di/dt for the short circuit discharging current.

Even for the series connected IGBT Phase unit, if the fault firing signal is provided to each devices, the series connected redundancy will not show its proper function. Fault firing gate signal such as unintended turn on, leads to full phase short circuit mode as show in Figure 5.12. Unintended turn off gate signal leads to full phase turn off.

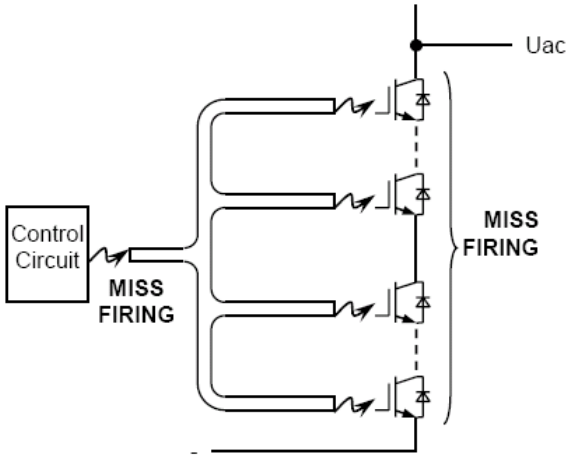

Figure 5.12 Fault-firing from control circuit cases full arm fault firing leads to full arm short circuit

Break down of or external flashover across one phase circuit also leads the short circuit mode failure immediately, see Figure 5.13.

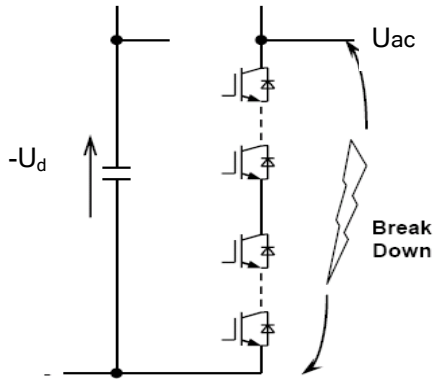

Figure 5.13 Break over between dc terminal and ac terminal along the VSC phase unit also leads to full arm short circuit

For the VSC circuit with each component contained inside the valve, insulation materials must be designed to have sufficient voltage withstanding capability to avoid the break down or flash over under normal and transient operation condition. They must be verified to have those sufficient capabilities by the dielectric tests and/or operational tests.

When the full-arm short circuit failure happens, short circuit current will be supplied from VSC dc capacitor and from ac system as shown in Figure 5.14.

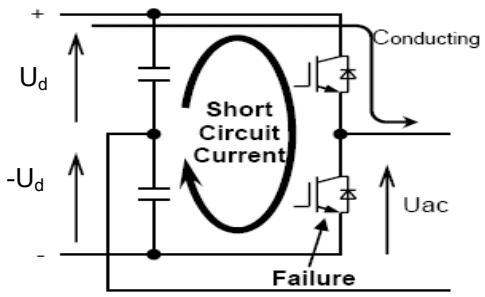

Figure 5.14 Full arm short circuit leads VSC dc capacitor discharge

Since the loop inductance throughout VSC dc capacitor and phase unit is usually very small, the short circuit current increases very rapidly. Over-current protection of IGBT Device itself is an important function to turn off the dc short circuit current without any discrete protecting device such as high speed fuses.

In case of the topologies with valves acting like controlled voltage sources, the capacitance of a dc cable would also result in a fault current through the IGBTs. Here, the valve reactors can be designed to limit the rise of fault current and to realize the capability to switch off all IGBTs within their SOA. For the lower voltage applications, it is a common practice to use the arm fuses as the protection method. It is not common to apply the fuses in high voltage system such as in HVDC converters.

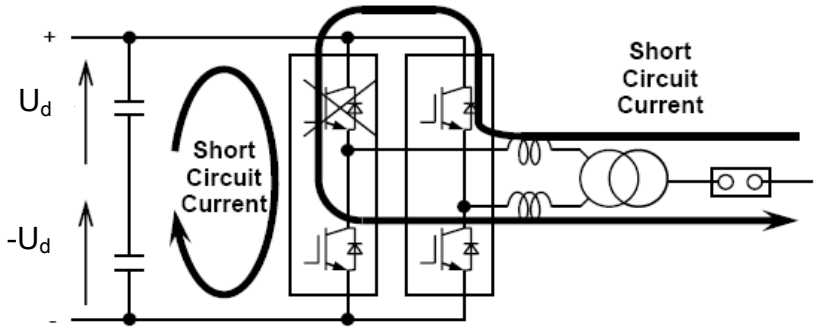

Figure 5.15 AC short circuit current and dc short circuit current

Some IGBT devices incorporate the over-current protection function in combination with gate drive unit. Sensing voltage or sensing current directly/indirectly, IGBT and gate drive unit combined circuit detects the over current and controls the gate voltage, suppresses the IGBT conducting current down to certain level small enough for the IGBT to turn off, then gives the IGBT off signal and turns off the short circuit current as shown in Figure 5.16.

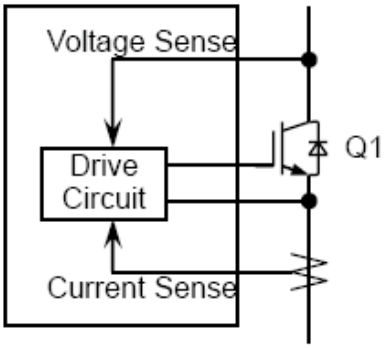

Figure 5.16 Short circuit protection circuit for each power electric device

A fault of an IGBT or an FWD in the topologies with valves acting like controlled voltage sources could lead to a rapid discharge of the associated submodule dc capacitor. For example, in case of an IGBT fault during turn off usually leads to a damage of the opposite FWD of the half bridge of the submodule. Thus the submodule dc capacitor will be discharged and the discharge current is limited by the loop inductance of the submodule. As the loop inductance is in the order of some μH, the resulting discharge current is in the range of some hundred kA. Neither an interruption of converter operation nor any effect on adjacent submodules or other equipment is acceptable under such circumstance

A complete valve failure in the topologies with valves acting like controlled voltage sources would also lead to a discharge current as shown in Figure 5.17. The capacitors represent the capacitance of a dc cable. In comparison to other topologies, the inductances in the short circuit loop are in the order of mH.

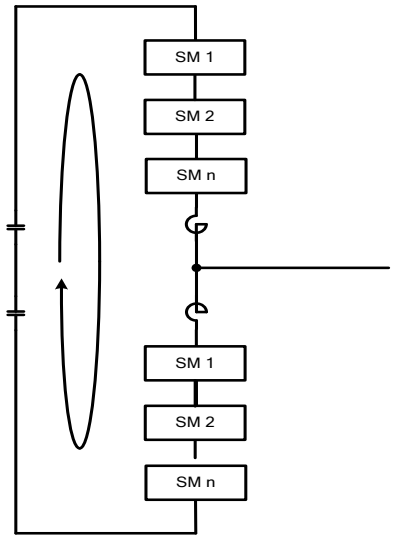

Figure 5.17 Description of VSC Valve failure in the Topologies with valves acting like controlled voltage sources

5.2.3.2 Open mode failure

In the a system with series connected IGBTs, open mode failure of an IGBT will lead to a short circuit failure mode as described in section 5.2.3.1. This assumes that one IGBT or VSC valve level including FWD fails in open mode. In that case, the total voltage of the phase unit will applied across both terminals of the failed IGBT or VSC valve level, which normally exceeds the voltage withstanding level of IGBT or VSC valve level and leads to over voltage failure.

The condition when the IGBT or VSC valve level fails in open mode is shown in Figure 5.18. To ensure reliable conducting capability, the insulation coordination on the IGBT level is such that the IGBT and/or the FWD is shorted due to overvoltage but there should be no external flashover outside the IGBT/FWD component. IGBT/FWD in VSC-HVDC with series connected IGBTs are designed to withstand the conducting current also when short circuited. Thus the IGBT/FWD itself serves as the overvoltage protection for the open circuit failure mode. That provides redundancy in the series connected VSC valve levels.

The protective function of the IGBT/FWD component must be checked during the test as it is supposed to work in appropriate timing against the open mode failure. The VSC valve level must be capable of withstanding the voltage which will appear in the transient until the IGBT/FWD is shorted due to overvoltage. This capability must be checked in the test where no breakdown outside the IGBT/FWD or any cascading failure should occur.

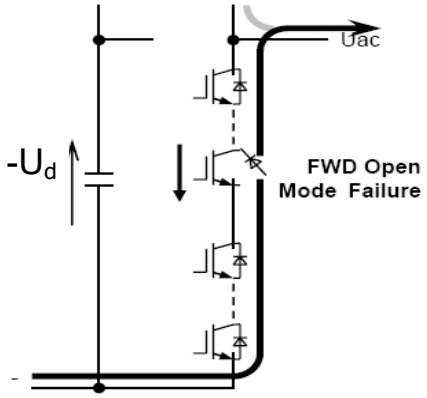

Figure 5.18 Open Mode Failure of FWD

If the gate turn on signal to a single IGBT level unit or the off-signal is given to an IGBT in the conduction interval, it results in an open mode failure on IGBT level, as described above

If the gate signal from a control unit to a complete valve fails or the off-signal is given to the conducting phase unit and off-signal is provided to all the VSC Valve Levels connected in series, the conducting current will be commutated to the FWD of opposite phase, without any over voltage, because the FWD of opposite phase keeps the path of the current. Thus no over voltage will appear in the VSC valve with unintended turn off, although total function is not properly maintained.

Note that under open mode failure, the fault phase can only be conducted by FWD, which leads to one direction of ac current only being conducted by the FWD of the healthy arm. This asymmetric switching action can cause dc offset in ac system. The offset is asymmetric in three ac phase which can cause the saturation of the transformer and dc harmonic if appropriate protection is not activated. Consequently, the VSC converters are provided with protective supervision for immediately blocking and tripping of the converter in case of an open mode failure of a complete valve.

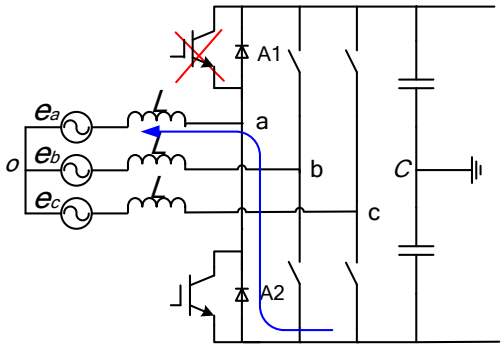

Figure 5.19 Open Mode Failure of IGBT

When using semiconductors without short-circuit failure mode capability, high speed bypass switches should be provided at the VSC valve level or the submodule as applicable.

5.2.3.3 Snubber circuit failure

Snubber circuit is designed to absorb the voltage of the IGBT device when it is turned off to suppress the switching stress.

There are several types of snubber circuits, which are designed as per the rating of the equipment and the number of series connected devices.

Individual snubber circuit will be applied to every IGBT device. The energy stored into the snubber circuit must be adequately drained before the next switching action. The simplest way is to dispose of the energy in the resister, which causes the thermal stress to snubber resister.

An individual snubber circuit contains a snubber resister connected in series with a snubber capacitor. The snubber resister sometimes is connected in parallel with a snubber diode, which forms the lower inductance path to charge the snubber capacitor.

For the clamping snubber circuit, the snubber resister is connected in parallel with a clamping diode, or is connected from the snubber capacitor to the VSC dc capacitor terminal, which discharges the clamping capacitor voltage down to dc bus voltage, within the adequate period of the switching actions of the IGBT.

When the snubber circuit fails, usually, serious damage occurs in the IGBT devices. In series connection applications, a voltage grading circuit such as a high impedance resister is often combined with the snubber circuit.

If the failure of the snubber circuit affects the grading circuit, it also affects the voltage sharing and balancing of each IGBT and sometimes results in IGBT/FWD overvoltage failure. Thus, the snubber circuit failure results in a short circuit failure mode on IGBT level, as treated in Section 5.2.3.1.

In topologies with valves acting like controllable voltage sources, the discharge of a submodule dc capacitor is limited to one VSC valve level. Snubber circuits are usually not necessary as the commutation occurs within one submodule with the possibility of low-inductive stray inductance. In case of a fault in one submodule, the resulting fault currents are in the range of several hundred kA. The VSC valve levels in the surrounding area of the failed submodule must not be influenced in their operation. Therefore special care has to be taken in the design regarding the mechanical stresses and the EMC behavior.

5.2.3.4 Free wheeling diode failure

FWD failure occurs mostly in the same structure or in the same module of IGBT device. Failure of FWD normally will be treated as an IGBT failure.

5.2.4 Interface Transformer Failures

The converter will be provided with a normal set of protections for system transformers such a differential protections and gas relays. In case of a transformer failure the converter will be blocked and the ac breaker will be tripped. Except for a dc side phase to earth fault, a transformer failure will not impact any other equipment. For a phase-to-earth fault, please see Section 5.2.1.

5.2.5 Phase Reactor and Valve Reactor Failure

The reactors used in VSC-HVDC are dry type air core reactors. Therefore, the only relevant failures for phase and valve reactors are flashovers to ground or flashovers across the reactor, which may be partial. In fact most of the reactor failures start as a turn-to-turn failure which usually develops to a complete reactor flashover, resulting in tripping and blocking the converter.

No existing VSC-HVDC scheme uses parallel reactors, thus it is not possible to apply unbalance protection for detection of changed reactance of the reactor. A flashover to ground failure will result in a valve side ac bus ground fault discussed in Section 5.2.1.

A partial flashover of a valve reactor in the topology where the valves act like controllable voltage sources will have marginal impact on the operation, see Figure 5.20.

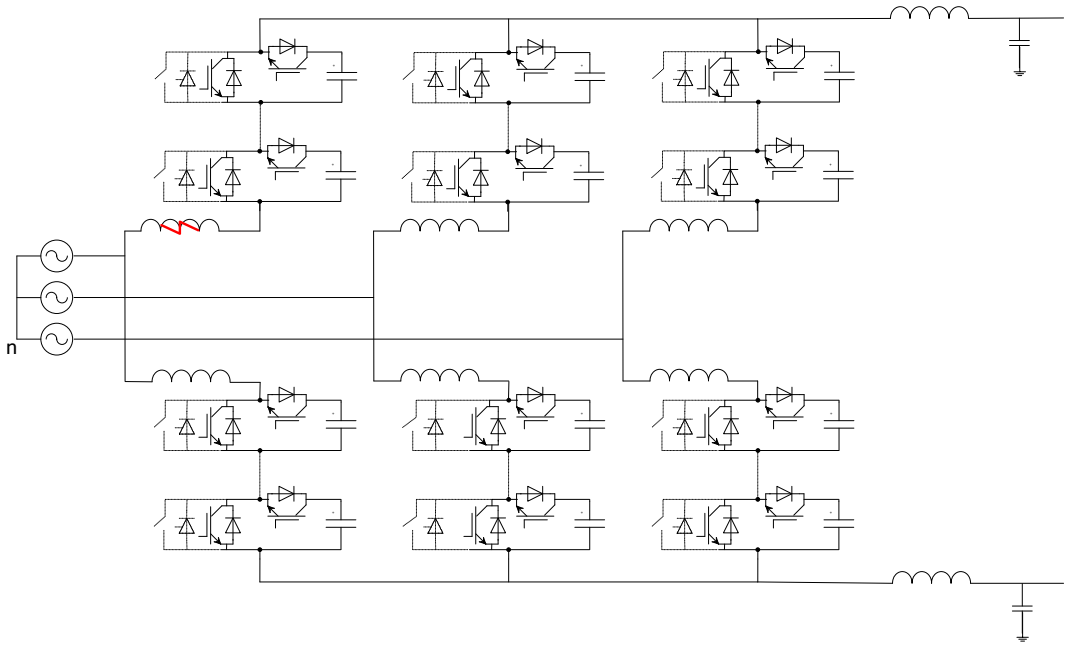

Figure 5.20 Phase reactor failure

The series connected reactors will limit the current derivatives at the valve switching. However, as the reactor fault develops there will be some abnormal converter current harmonics which might be detectable.

In the topology where the valves act as controllable switches, a partial reactor flashover will have significant impact on the operation, see Figure 5.21. The series connected reactors in the other phases will limit the current derivative and the current ripple at commutation.

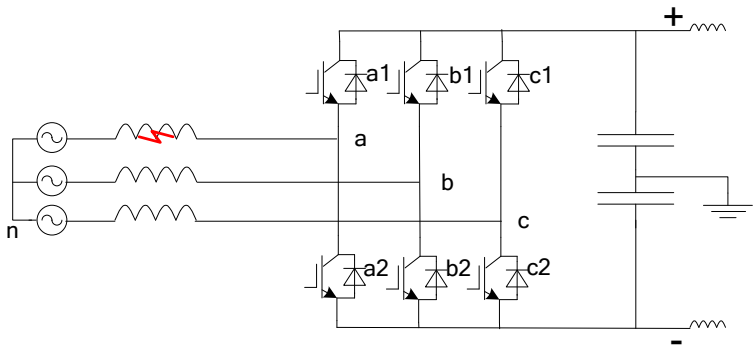

Figure 5.21 Phase reactor failure

However, as the fault develops, the amplitude of the ripple current and the ac side current harmonics will increase. That may be detected at high loading of the ac filters or high current amplitude of the converter ac side current.

For either topology, an electrical protection will not detect a reactor turn-to-turn flashover in an initial stage. However, if the phase or valve reactors are located indoor, an arc detector and/or a smoke detector will detect a turn-to-turn flashover in an early stage. Anyhow, a complete or temporary flashover of a phase or valve reactor will not impose any severe stresses on other equipment.

5.2.6 VSC DC Capacitor and Submodule DC Capacitor Failure

The dc capacitor can be subjected to transient overvoltage due to external faults and the capacitor must be able to withstand its temporary overvoltage stress as defined by the arrester protective scheme of the converter.

The capacitor bank must be able to withstand the discharge current that will occur at a ground fault in or close to the bank at a pre-charge level corresponding to its temporary overvoltage stress.

A failure of a submodule dc capacitor is limited to the respective valve level and is therefore included in the redundancy of VSC valve levels. Failures of the capacitor usually lead to abnormal voltage waveforms and a subsequent bypass of the respective submodule. In addition a deviation of the capacitance of the submodule dc capacitor can be monitored online with the measurement of the submodule voltages and valve currents. A submodule dc capacitor with suspected capacitance degradation can then be replaced during maintenance.

5.2.7 PLC-reactors, HF-filters etc

Failure of PLC-reactors, HF-filters etc. is very rare and a failure will only result in a degraded harmonic performance, but no significant stresses on other equipment. As this equipment is often installed indoor, the fire or smoke detectors will detect the failure as soon as it starts to cause smoke. In any case, this equipment is simple and has a robust design and therefore the failure rate should be very low.

5.2.8 AC and DC Filter Failures

The ac and dc filters will be provided with their own protection as in a HVDC scheme with line commutated

converters. The ac filter capacitor banks can be expected to be equipped with unbalance protections and similarly ac and dc filter reactors and resistor can be expected to be provided with thermal overload protections. The protection will detect internal faults in ac and dc filters and clear the faults. In case there are no redundant filters, the converter will be blocked and the ac breaker tripped. In case of a redundant ac filter, the ac breaker of the faulty filter will be tripped.

Operation without ac and dc filters will worsen the harmonic performance by not impose any significantly increased stresses on other equipment.

5.2.9 Smoothing Reactor Failures

The smoothing reactor for a VSC converter is in most cases a quite small dry type reactor more similar to a large PLC reactor than a smoothing reactor for a HVDC scheme with a line commutated converter.

For earth faults, please see section 5.3.2.

As the reactor has a robust design and the steady state stresses are low, the likelihood for a failure should be very low. Anyhow, the most likely internal failure is a turn-to-turn failure caused by transient overvoltage which may, if not detected, reduce the effective inductance. The consequence is a worsened RFI and dc side harmonic performance.

In case of an indoor installation the fault will be detected by the fire alarm, or smoke detectors. In case of an outdoor installation it may be detected during a visual inspection, or perhaps as a pole to earth fault.

5.3 DC TRANSMISSION LINE FAULT

5.3.1 General

The stresses on valves and other equipment during dc line faults and other faults resulting in abnormal dc line voltage depend very much on the actual system configuration. The converter in any case acts as a stiff voltage source. Thus, in case of a stiff connection, a fault results in a short circuit current event and in case of a high impedance connection, the same fault results in an overvoltage event.

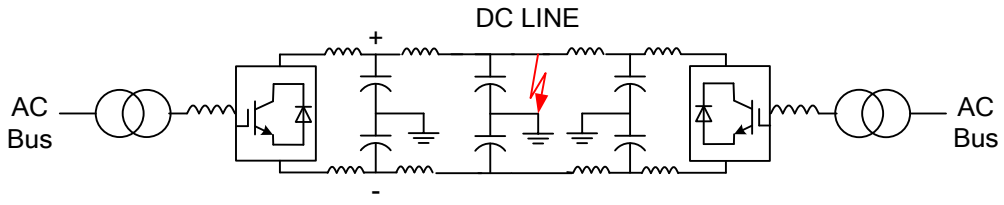

Figure 5.22 Balanced VSC-HVDC transmission

In case of a pole-to-earth fault in a balanced VSC-HVDC transmission as shown in Figure 5.22 the voltage of the other pole will rise up to about 2 pu. In the case as shown in Figure 5.22, with a pole-to-earth fault on the positive pole, the negative pole will be exposed to overvoltage that will stress the arresters on the negative pole, but there will be no high fault current, except for the capacitive discharge currents.

However, in case one side of the converter is connected to earth, as shown in Figure 5.23, an earth fault on

the positive pole will not result in any overvoltage, but the ac networks on both ends will feed short circuit currents into the dc side via the diodes until the ac side is interrupted.

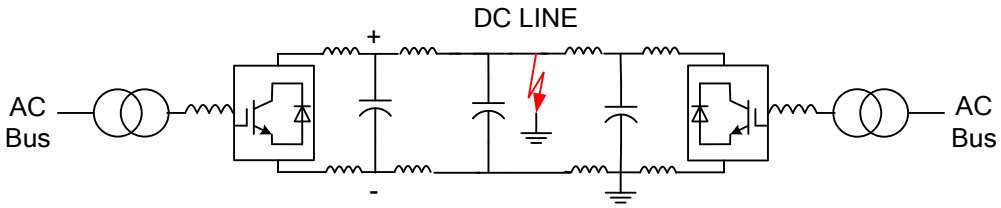

Figure 5.23 VSC-HVDC transmission with one side earthed

As there are many possible ways to arrange VSC-HVDC transmission, not all alternatives can be discussed here. Instead the description below reflects some typical schemes.

5.3.2 DC cable fault

The typical characteristic for a dc cable fault is that it is a permanent fault. Thus the converters at both ends of the cable will be immediately and permanently blocked and the ac side breakers tripped upon a detection of a cable fault.

Figure 5.22 shows a common configuration for cable transmission. In this type of system, a pole cable fault will not result in any significant stress on the converter valves but will stress the pole arresters on the healthy poles. The dc side capacitors will be discharged through the fault resulting in a surge current of short duration.

In case the transmission is asymmetrical and one side is earthed, a pole to earth fault will not result in any overvoltage but a short circuit current will flow through the FWDs and reach a magnitude determined by the ac side impedance and the dc side fault impedance, until the ac breakers are tripped.

As a cable fault is permanent there is plenty of time to allow for equipment cool down until the operation of the system can be resumed.

For topologies with valves acting like controlled voltage sources, because of the high resistive grounding connection, the single pole to ground fault only leads to a potential sudden change with no current stress, the dc pole-to-pole fault causes the submodule dc capacitor to discharge, however, the current rate of rise is suppressed by the valve reactor, which gives enough time for the protection to block the converter. Similar to the topology with valves acting as controllable switches, after blocking, the diode will suffer the overcurrent fed by ac system, but in topologies with valves acting like controlled voltage sources, the diodes are protected by the parallel thyristor to ensure the reliability of the valves.

5.3.3 DC overhead line fault

The important characteristic for a dc overhead line fault is that it in most cases the fault is a temporary fault calling for a restart of the transmission after clearing the fault. Furthermore, the configuration as shown Figure 5.23 is considered as the most typical configuration for an overhead line. Thus, a dc side fault will result in a temporary short circuit current in the converter, until cleared by the ac side breakers at both ends of the HVDC link. Seen from the ac side the fault will result in voltage drops, as for any three phase fault in

an ac system.

However, on the dc side the dc current will continue to flow, even when the ac breaker is open, due to the dc side inductances. The diodes in the VSC valves will act like free wheel diodes for the dc current. The decay time depends on the dc side losses, including the arc voltage of at the point of failure. (For all temporary faults there will be an arc.)

For fast fault clearing and isolation of the dc side HVDC breakers can be used.

The valves, in particular the diodes, must be designed for the overcurrent at the fault clearing taken into consideration that the converter shall be energized from the ac side again when the faulty dc side is isolated, taken into account fault clearing sequence timing.

In case of the topologies with valves acting like controlled voltage sources, the rise of the valve fault current is limited by the valve reactors. After blocking the IGBTs within microseconds, the submodule dc capacitors are not discharged. Till the circuit breaker is opened, a fault current is driven by the ac system through the freewheeling diodes D1 of the submodules.

5.3.4 DC line lightning overvoltage（dc overhead line only）

For overhead line transmission, a typical configuration shown in Figure 5.23 is a common arrangement at present. For asymmetric monopolar system, dc bus overvoltage is introduced by lightning strikes on dc overhead lines, which is known as fast-front overvoltage. However, the majority of the lightning energy is absorbed by the VSC dc capacitors, causing the amplitude and rate of change of the overvoltage to be suppressed: the larger the dc capacitance, the smaller the overvoltage.

Valves and dc pole are usually equipped with pre-defined surge arresters for the limitation of destructive overvoltage. The overvoltage suppression equipment shall be rated for this duty, taking into account the specific devices used, i.e., surge arresters.

5.3.5 DC overvoltage due to VSC control faults

Hypothetically, certain control failures could result in dc side overvoltage. However, due to the valve and circuit capacitance, the voltage rise would be quite slow, compared to the voltage rise in the case described in section 5.2.1 above. The protection will block the valves in case the voltage rise to unacceptable levels.

5.3.6 DC overvoltage due to blocking of remote converter

Blocking of the rectifier will not result in any overvoltage as the inverter will transfer the dc side energy to its ac-side until there is an undervoltage situation. The control and the diode rectification will limit the voltage drop.

However, blocking of the inverter will result in overvoltage. The overvoltage will be determined by the stored magnetic energy in the dc side inductances, the power is fed in by the rectifier until it senses the overvoltage and the power infeed is stopped by the control. The energy stored in the inductances amount of energy will be transferred to stored energy in the dc capacitances. Thus, the overvoltage is to a large extent determined by the relationship between the dc side inductance and dc side capacitance, combined with the dc

current at the time the fault is interrupted. Hence the worst case is a long overhead line combined with high dc current. When the voltage is above the acceptable operating voltage, the valves will be blocked.

The overvoltage associated with the blocking of a remote inverter terminal is not a problem for the equipment rating, but a concern for the possibility to impede quick restoration of the operation after the disturbance. The most likely reason for blocking of the inverter is a temporary disturbance (earth fault) in the inverter ac network. Even in case of a permanent inverter blocking it is favorable to quickly restart the rectifier for voltage control of the rectifier ac network.

In many situations, the overvoltage at blocking of a remote inverter will not result in overvoltage above the normal operating level. However, if the voltage resulted from blocking of an inverter rise too high, it is possible to add voltage limiting devices.

5.4 REFERENCES

[5-1] Lianxiang Tang, Boon-Teck Ooi, *"Managing Zero Sequence in Voltage Source Converter*," Industry Applications Conference, 2002. 37th IAS Annual Meeting

[5-2] Lianxiang Tang, Boon-Teck Ooi, "***Converter non-integral harmonics from ac network resonating with dc network***," IEEE 36th Industrial Application Society Annual Conference, Chicago, 2001.

[5-3] John P. Bowles, *"Overvoltages in HVDC transmission systems caused by transformer magnetizing inrush currents*" IEEE Transactions on Power Apparatus and Systems, Vol. PAS-93, March/April 1974, pp. 487-495

[5-4] D. Povh, W. Schultz, "***Analysis of overvoltages caused by transformer magnetizing inrush currents***", IEEE Transactions on Power Apparatus and Systems, Vol. PAS-97, July/Aug. 1978, pp. 1355-1365.

6. SPECIFIC COMPONENT STRESSES RELEVANT TO TESTING

6.1 GENERAL

Chapter 4 and 5 give the detailed description of component stresses of the VSC transmission system under steady-state and fault conditions respectively. Based on this, chapter 6 will focus on the further analysis of those stresses, in order to develop test philosophies.

The aim of tests is to verify that fully tested components fulfill the design requirements and have the capability to operate reliably under both normal and fault conditions. To accomplish this we ideally have to reproduce all possible stresses under the real working conditions. In practice some representative tests are defined, through which we can be reasonably assured that the tested components should satisfy all anticipated operational conditions.

This chapter is intended to cover all stresses of every component one by one, identify the critical stresses, and more detailed analysis of the test requirements in order to provide the foundation for the definition of test methods described in chapter 8.

6.2 VALVE

6.2.1 Steady-state

6.2.1.1 Stresses relevant to operational tests

The steady-state valve voltage and current waveforms are shown in Figure 4.1. The HF (high frequency) characteristic implies that the switching frequency is a significant factor influencing valve stresses. The valve currents are HF impulses enveloped by sine waveform which contains harmonics determined by the phase reactance, while the voltage waveforms are HF square wave with the same amplitude but varying widths.

It shall be noted that, due to the recovery process of FWD (free-wheeling diode), the valve current will include an overshoot during valve turn-on, as shown in Figure 4.3. The overshoot increases with an increasing valve maximum off-state voltage and rate of rise of current (di/dt) of the IGBT during turn-on. As for valve turn-off, circuit stray inductance will impose a voltage overshoot upon the valve as a result of the high di/dt, see Figure 4.3. The amplitude of the overshoot is associated with circuit stray inductance and di/dt.

When C-R type snubber circuit is connected across the IGBT, the resistor experiences mechanical stress caused by high di/dt due to the IGBT switching, as well as heat dissipation. The capacitor also dissipates dielectric loss which is proportional to the switching frequency.

In the topologies with valves acting like controlled voltage sources the commutation processes and the related effects are limited to the individual submodules. The switching frequency is in the order of one hundred to two hundred Hz, the voltage steps in the range of a few kV.

6.2.1.2 Stresses relevant to dielectric tests

As explained in Section 4.2, the valve off-state dc voltage is equal to dc bipolar voltage. Besides, the valve voltage includes overshoot generated by circuit stray inductor in the presence of valve turn-off di/dt. The amplitude of the overshoot, depending on circuit stray inductance, di/dt as well as snubber circuit design, is normally 20%-30% of the valve's nominal voltage.

The valve support connected to the valve's ac terminal is subjected to the repetitive switching overshoot, while that connected to the valve's dc terminal is subjected to the single pole to ground dc voltage, as shown in Figure 4.12(b).

Because VSC valves may operate at high frequency up to several kHz, the overshoot also may appear at each switching. Therefore strictly speaking, dielectric tests should be performed using the same frequency to verify the withstand ability against the repetitive switching overshoot. However it is generally known that V-n (flash-over voltage versus number of repetitive application) characteristics in the air is almost flat from dc to 10 kHz as shown in Figure 6.1. For the VSC application, the switching frequency is usually less than several kHz. Then we can verify the voltage withstand ability of VSC valve by using power frequency, and avoid the high frequency testing.

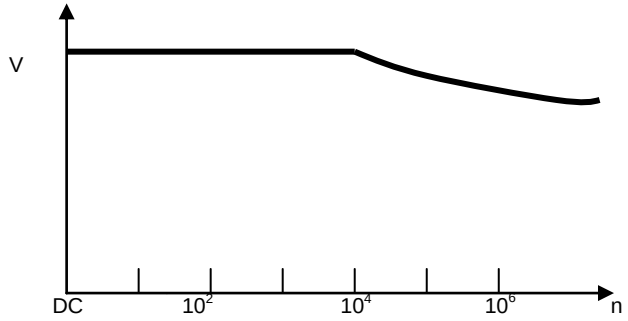

Figure 6.1 V-n characteristics in the air

During the operation, no harmful partial discharge should be allowed, and then the level of the partial discharge test between valve terminals, Utac2, should include a test safety factor in addition to the maximum switching over voltage, Umax as shown in Figure 6.2.

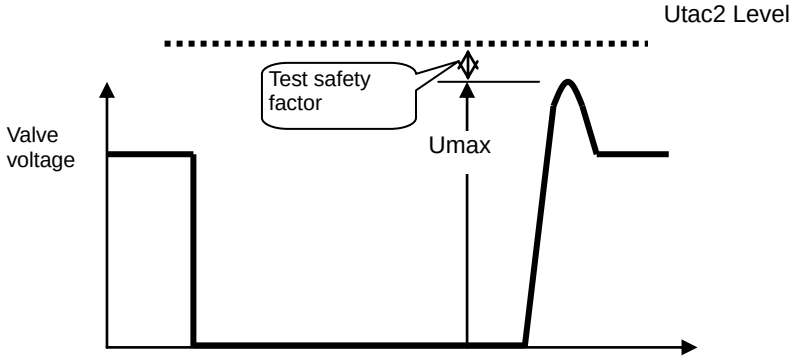

Figure 6.2 Valve voltage and test voltage

6.2.2 Transient Stresses

6.2.2.1 Stresses relevant to operational tests

Generally, the valve voltage during operating state is exposed to the dc bus voltage. However, after blocking due to a severe overcurrent, the transient overvoltage capability of the valve is also required, which demands definition of relevant test conditions.

Typically, valve flashover or valve mis-fire will render VSC dc capacitor to fast discharge through the IGBTs, introducing IGBT overcurrent which depends on the stray inductance and resistance of the discharging loop. Similar stresses can be seen during converter ac terminal faults, but the overvoltage stress is more critical for the valve due to the overvoltage on the healthy phases. This should be considered in the IGBT overcurrent turn-off test.

For topologies with valves acting like controlled voltage sources, the corresponding fault scenarios are submodule short-circuit failure or valve flashover. Valve reactor ground fault on the valve side should also be considered.

In the event of dc pole-to-pole fault, the ac current is close to the three-phase short-circuit current which is determined by the ac short circuit current and the impedance of the fault current circuit. The protection strategy demands blocking of the converter and tripping of the ac circuit breaker. Although the duration of the FWD overcurrent is relatively long, overvoltage is avoided. The stress shall be reflected in the short-circuit current test.

6.2.2.2 Stresses relevant to dielectric tests

The dielectric test should contain the ac, dc support test and valve terminal ac-dc voltage test.

For the internal ac bus fault scenarios, the overvoltage on healthy phases under asymmetric faults should be considered in the valve support ac voltage test. Due to the over voltage on the healthy phases under specified faults, it may force the FWD to continue conducting which charges the VSC dc capacitor significantly above its nominal voltage. The stresses should be considered in the valve support dc voltage test. Thus the combination of ac and dc voltage should also be considered in the ac and dc test.

Due to dc single-pole-to-ground fault, the dc bus of the healthy pole will be charged to approximately twice the nominal value, depending on the arrester design. The stress should be considered in the valve support dc voltage test. A dc offset of the ac terminal to ground voltage will also be induced. These voltage stresses shall be reflected in the valve support ac voltage test or dc voltage test by means of an equivalent test method.

6.3 INTERFACE TRANSFORMER

There are many alternative concepts for VSC-HVDC schemes and from case to case it has to be evaluated if the transformer is exposed to any specific stress above the normal stresses for an ordinary ac transformer. In most cases relevant parts of guides and standards for ordinary HVDC transformers can be directly applied.

6.3.1 Steady-state

In topologies where the valves act as controlled switches the operation stresses on the interface transformers depend very much on the actual configuration. If the ac filters are located on the valve side of the transformer and there is no dc voltage present on the transformer, the stresses and test requirement will be the same as for an ordinary ac transformer. If one side of the circuit is earthed, as per Figure 5.23 the relevant part of the dc requirement and test for a conventional HVDC transformer has to be applied. If the ac side filters are located on the network side of the interface transformer, the relevant section for harmonic current loading has to be applied. And if the transformers are directly exposed to valve switching transients these stresses have to be relevantly considered.

Under normal operation, both the voltage and current of the valve side transformer windings are close to power frequency ac waves. Regarding interface transformers for symmetric monopole VSC-HVDC with the ac filters located on the valve side of the interface transformer, no specific stress different from conventional ac transformers will be present. Test of transformer should follow IEC 60076. However, regarding interface transformers for asymmetric monopolar VSC-HVDC the valve side dc voltage must be considered. Furthermore, when the ac filters are located on the ac system side of the interface transformer, the harmonic content of the transformer current must be considered. See IEEE Std C57.129-2007 “IEEE Standard for General Requirements and Test Code for Oil-Immersed HVDC Converter Transformers” for more information.

In topologies where the valve acts like a controlled voltage source, the multi-level voltage on the valve side approaches a sinusoid wave and the current through the interface transformer is also sine-wave shaped, so the normal ac test requirements can be used for the interface transformer, provided that the dc side voltage is balanced to ground.

6.3.2 Transient

The transient stresses to be considered for the transformer tests should contain all the critical stress conditions related to faults for each winding. Typically, the stresses that appear on the ac system side are similar to those for conventional HVDC transformers. This includes lightning overvoltage caused by lightning strikes or switching overvoltage caused by fault clearing and etc. These stresses should be considered in the applicable test specifications.

However, there are some unique transient stresses for VSC-HVDC transformers that should be considered: Transformer secondary side will be exposed to a few cycles of a transient overvoltage during valve side phase-to-ground faults. The stress can be defined as switching impulse voltages whose amplitude is going to be limited by the arresters.

DC offset will be introduced on the transformer converter side in the event of a dc pole-to-ground fault. The dc overvoltage is clamped by the filter capacitor (if any) even after tripping of the ac circuit breaker. This voltage stress will decay with time due to discharge of the filter.

6.4 VSC DC CAPACITORS

6.4.1 Steady-state

The dc capacitors should be tested with a direct voltage equal to $k\left(U_d + \sqrt{2}\sum U_h\right)$ where k is a suitable test factor (>1), the capacitor should also be demonstrated to have thermal stability.

6.4.2 Transient

The capacitor should be able to withstand temporary overvoltage stress and discharge or similar fault current.

The converter arrester scheme will ensure that the maximum temporary overvoltage is limited and the dc capacitors should be tested with a direct voltage corresponding to the protective level of the arrester.

Critical fault conditions for the temporary overvoltage stresses are:

Over voltage under internal ac bus single phase to ground fault will charge the VSC dc capacitor to a high level, as presented in 6.2.2.2, dc pole to ground fault which will force the healthy pole dc voltage to the protective level of the arrester.

The most severe (critical) dc capacitor fault current will occur if the bank is discharged at a ground fault close by the capacitor bank when pre-charged to the arrester protective level. The discharge current for individual units has to be corrected by the number of parallel units/strings the bank is built up with.

6.5 SUBMODULE DC CAPACITOR

In topologies where the valve acts like a controlled voltage source, the submodule dc capacitors are exposed to a line frequency current and the resulting relative voltage ripple is higher.

Overcurrent stress

The most severe overcurrent fault scenario is a discharge of the submodule dc capacitor through the IGBT half bridge of the associated submodule circuit. This failure can occur in case of a short circuit of the IGBTs. The resulting current is mainly determined by the capacitance of the submodule dc capacitor and the stray inductance in the fault circuit and is typically in the order of several hundred kA. The capacitor should sustain such a fault without damage. The converter has to be operated without any interruption in case of such a fault. Therefore any effect on the adjacent submodules should be avoided.

In case of other fault scenarios, the IGBTs of the converter can be turned off and a discharge of the capacitors can be avoided.

Overvoltage stress caused by blocking of the inverter

The overvoltage introduced by blocking of the inverter depends on the control mode employed at the rectifier. If dc voltage control is adopted when the inverter is blocked, then the dc side will only present a temporary overvoltage depending on the control response and on the length and inductance of the dc cable/line. However, if active power control is used, then the dc side overvoltage will keep growing till activation of

protection.

The overvoltage should be considered in voltage test to reflect the situation shown in internal ac bus, ac system temporary overvoltage etc.

For additional information, see IEC61071.

6.6 PHASE REACTOR

The phase reactor has to accommodate the difference in voltage between the ac system and the converter terminals.

Phase reactors are usually of air-core dry-type design.

For the design criteria of reactor, the following points have to be taken into account:

Stresses due to fundamental (50 Hz or 60 Hz) current

Stresses due to harmonics in the lower and middle frequency range

Dielectric stresses due to harmonics in the middle and upper frequency range

Dielectric stresses due to normal operating voltage and transient voltages occurring during fault scenarios

6.6.1 Steady-state

The phase reactor of two and three level converters has to accommodate the difference in voltage between the ac system and the converter terminals. The latter is a string of high and fast rising pulses, as shown in Figure 4.12 (b), which needs special attention in the design of the air core reactor. The insulation system of the reactor winding must withstand this type of repetitive fast rising pulse voltage. Suitable design tests on voltage endurance must be carried out to verify the adequacy of the insulation system to provide sufficient life time for this kind of voltage stress.

Due to the steep front of the pulses the voltage distribution along the winding tends to be non-linear resulting in a higher turn voltage than in case of a linear distribution; particularly at the winding end connected to the converter. Shielding electrodes mounted to the winding ends may be used to mitigate the non-linearity in order to alleviate the voltage stress.

Under normal operation, the current flowing through a phase reactor is an ac current superimposed by HF harmonic currents. The characteristics of the harmonic currents depend on the converter topology and the modulation method. The phase reactor itself can contribute to wave smoothing and therefore harmonic amplitude can be limited by properly choosing the reactance. The thermal performance of the reactor should be tested with fundamental 50 Hz or 60 Hz current. The temperature rise of the winding caused by the harmonics is considered by testing the reactor by injection of a thermally equivalent current so chosen that all the losses caused by the fundamental and all harmonic currents are properly represented.

6.6.2 Transient

Typically, the transformer is arranged for blocking the ac side zero sequence current from impacting the converter equipment. Thus, the most severe overvoltage imposed on the phase reactor ac side should be the overvoltage caused by internal ac filter bus and dc pole to ground faults which are similar to the interface transformer valve side as described in Section 6.3.2. The phase reactor valve side voltage amplitude is determined by the dc pole to ground voltage Thus the relevant overvoltage on phase reactor valve side is the same as the overvoltage for the dc capacitors, see Section 6.4.2.

For current stress, the fault scenarios should be considered are as follows:

- The internal ac bus fault;
- DC pole-to-pole fault.

6.7 VALVE REACTOR

As mentioned above, the content of current harmonics flowing through the valve reactor is relatively low in the topologies with valves acting like controlled voltage sources. Thus standard air core reactors can be utilized.

The insulation system of the reactor winding must withstand the surge currents and voltage pulse stresses in case of insulation failures within the substation or on the dc line.

Transient stresses similar to those referred to Section 6.6.2 should also be considered for valve reactor.

6.8 SMOOTHING REACTOR

6.8.1 Steady-state

Under normal operation, the current flowing through smoothing reactor is the dc current superimposed by the dc side harmonics as explained in Section 4.8. The harmonics shall be considered in the reactor temperature rise test. The turn-to-turn voltage stress due to harmonics is quite low.

The influence on the temperature rise of the winding by the harmonics has to be considered by testing the smoothing reactor with a thermally equivalent dc current which includes the dc current losses as well as the losses introduced by all of the harmonics. The voltage stress between the reactor terminals due to the harmonics is quite low and may be simulated by an ac voltage test between the terminals. The insulation to ground is provided by the support insulators.

6.8.2 Transient

For smoothing reactors in series with a dc line, the relevant terminal to ground overvoltage stresses are similar to those that appear on the VSC dc capacitor. Converter ac bus ground faults will expose the support insulators of the smoothing reactor to temporary dc overvoltage in accordance with section 5.2.1.

Other fault cases to be considered area:

- Converter pole bus ground faults in accordance with section 5.2.2;
- DC line faults in accordance with sections 5.3.3 and 5.3.4.

These stresses shall be reflected in terminal to earth voltage test.

In the event of a dc line fault (either a dc cable fault as explained in section 5.3.2, or a dc overhead line fault as illustrated in section 5.3.3), the smoothing reactor will be exposed to surge current, which the reactor must withstand. This can also impose a steep front surge on the line side of the reactor causing turn to turn failure of the reactor.

For overhead line system, another scenario should also be considered. As explained in Section 5.3.4, for the smoothing reactors used for overhead lines, lightning strikes will induce overvoltages on smoothing reactors which shall be reflected in lightning impulse voltage test of smoothing reactor. Since the lightning strike may have a reverse polarity as compared to the dc line-to ground voltage, the voltage across the terminals of the smoothing reactor may be the sum of both dc and lightning voltage, this case might be worse than a ground fault at the reactor terminal.

6.9 Radio Frequency Interference Filter

The RFI filters are exposed for the same current and voltage stresses as the valve side winding of the interface transformer, see Section 6.3.

6.10 Common Mode Blocking Reactor

The common-mode blocking reactor and smoothing reactor are usually connected in series with the dc line, and therefore the steady-state and transient stresses of common-mode blocking reactor are similar to those of the smoothing reactor.

6.10.1 Steady-state

During steady-state operation, the current flowing through the common-mode blocking reactor is dc side harmonics currents superimposed by on the dc side current. Besides, the reactor is exposed to the common mode voltage harmonics.

Furthermore, common mode blocking reactor is exposed to the pole-pole the dc voltage.

6.10.2 Transient

The transient stresses on the common-mode blocking reactor are similar to those of the smoothing reactor, discussed in section 6.8.2. Furthermore, during internal pole to ground faults, both converter faults and dc line faults, the transient common mode voltage will be significantly higher than the steady state stresses, unless limited by surge arresters.

7. COMPONENT LOSSES

This part focuses on the determination of losses in the main components of a VSC system, for the purpose of defining thermal rating conditions of the main circuit components including cooling equipment. Furthermore a similar procedure could be used to determine guarantee losses under normal operation of the converter station. The common practice for the determination of losses for Classic HVDC according to IEC 61803 should, whenever possible, be followed.

With regard to loss calculations used for thermal rating of the main circuit components the maximum continuous operating conditions should be used. Operating conditions for thermal rating should state the maximum ambient conditions as well as the worst case conditions for power frequency voltages and currents as well as harmonic voltages and currents. When short term overload operation is decisive for the thermal rating, corresponding operating conditions should be used.

Regarding calculation of the guaranteed losses during normal operation, common practice is to use an average ambient dry bulb temperature of 20°C. Operating conditions should, if nothing else is specifically stated, be assuming to nominal grid voltage, at rated active power transfer and at unity power factor with respect to the grid interface point. But it should be noticed that losses be worse for some filter equipment under partial loading.

7.1 VSC VALVE LOSSES

A station consists of a number of valves, where a valve is built up of a number of VSC valve levels. The losses are calculated for each level and then added to obtain a total sum for all levels in the valves in the station.

VSC valve losses consist of contributions from following parts:

- IGBTs
- Diodes (FWD)
- Voltage divider/ Snubbers
- Gate drive unit / Auxiliary power
- Submodule dc capacitor, if any
- Bypass switch, if any

7.1.1 IGBT and Diode

7.1.1.1 IGBT and diode loss calculation

IGBT and diode losses (semiconductor devices) consist of on-state, turn-on and turn-off losses. For the diode

the turn-on loss is negligible as it immediately starts to conduct in forward direction. The turn-off loss due to diode recovery, however, is not negligible.

The on-state loss is calculated by using the average and rms current value in each component together with the threshold voltage drop and slope resistance according to the following formula:

$$P_{on-state} = U_{to} I_{av} + R_t I_{rms}^2$$

The turn-on loss is calculated by defining the instantaneous turn-on energy at each turn-on switching (function of voltage, current, temperature and the characteristics of the device at turn-on) and then add all turn-on energies together for all switching in a fundamental frequency cycle time or if switching is not synchronized to the fundamental sufficient time, to get average losses divided by the corresponding time as shown below.

$P_{turn-on} = (1/T) \cdot \sum (E_{turn-on})$; where T is the time interval.

The same calculation is done for turn-off losses but here the instantaneous turn-off energy is used.

$P_{turn-off} = (1/T) \cdot \sum (E_{turn-off})$; where T is the time interval.

The different switching intervals, with instantaneous current and voltage, are defined by the parameters in the converter for a steady state fundamental frequency cycle. (converter type, PWM control pattern, operational mode(active- reactive power), dc voltage, ac (phase reactor) current, modulation index, phase reactor size, ac-bus voltage)

There are also some losses due to leakage current during the off state that should be considered.

This gives the total semiconductor losses as shown below.

$P_{IGBT} = P_{on-stateI} + P_{turn-onI} + P_{turn-offI} + P_{off-state}$

$P_{diode} = P_{on-stateD} + P_{turn-offD} + P_{off-state}$ ($P_{turn-on}$ is negligible in the diode)

7.1.1.2 IGBT and diode loss design details

Due to the different power factor from an inverter to a rectifier operation, in most cases inverter operation is thermally decisive for the IGBT part, and rectifier operation is thermally decisive for the diode part. The reason is that the highest on-state loss for the IGBT appears in inverter operation and the highest on-state loss for the diode appears in rectifier operation.

High power dissipation at IGBT turn-on and turn-off is due to the fact that the device is subjected to high current and high voltage simultaneously during a substantial part of the switching process. In order to reduce the associated losses, the device should switch as fast as possible, that is, as high voltage and current derivatives as possible. The drawbacks with high di/dt are that the inevitable stray inductance in the commutating circuit will produce a voltage (u=L*di/dt) and cause higher RFI. This voltage will be in

addition to the dc voltage across the IGBT and must be taken into account in the VSC valve design. It is highly desirable to keep the stray inductances in the commutation circuit as low as possible. This is a major consideration in the layout of the converter circuit.

The design of the VSC valve involves an overall optimization between losses, di/dt and voltage across the component for all VSC schemes.

The IGBT turn on energy and turn off energy are defined as 1 pulse energy dissipation at a certain voltage (Vce), temperature and IGBT conducting current (Ic). E-on and E-off is shown in Figure 7.1. Assuming the same voltage and temperature during a fundamental period, E-on and E-off vary with current waveform. Summing up those energies at every switching operation, for 1-cycle of fundamental waveform and divide by the period time (T), the average losses are calculated as shown in Figure 7.2.

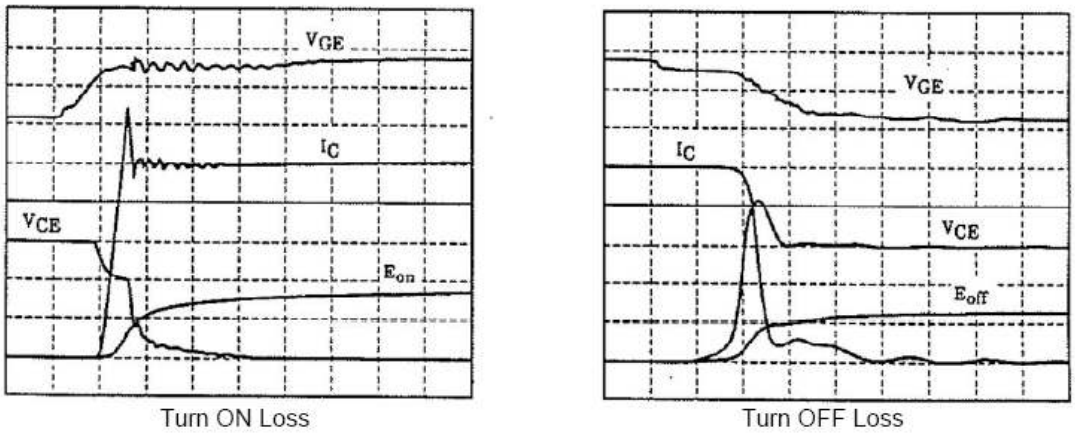

Figure 7.1 Typical waveform of Turn ON energy and Turn OFF energy of IGBT

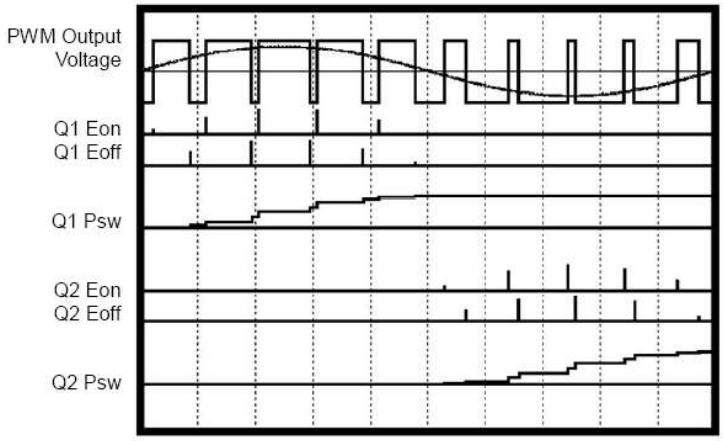

Figure 7.2 Calculation of switching loss with sinusoidal waveform current

Switching and conduction losses vary as a function of the junction temperature. Usually a higher junction temperature leads to larger switching and conduction losses. To have representative losses the valve shall be brought to thermal steady state condition at maximum continuous load, with the maximum coolant temperature.

Switching losses vary with the gate drive circuit switching time. In case of driving with a voltage source and a gate resistor, an example of change in switching characteristics as a function of gate resistor is shown in Figure 7.3. Changing gate resistor to higher values makes switching time longer, and switching losses larger.

(The opposite with lower value on gate resistor.)

With shorter switching time (higher du/dt and di/dt) problem with high frequency oscillations can occur. The gate driving method must be chosen carefully taking into consideration the system configuration and the requirement of the application.

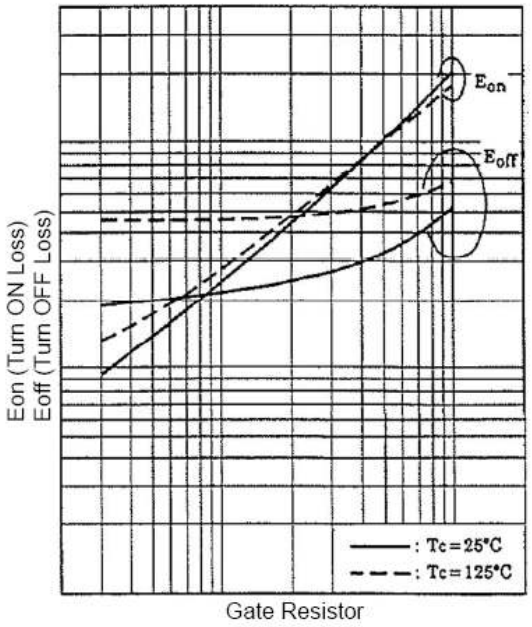

Figure 7.3 Example of IGBT turn on/off energy as a function of gate resistor and junction temperature

7.1.2 Voltage Grading Circuit/Snubber

Depending on design of the VSC valve level, different types of voltage grading circuit or snubbers can be applied (or common to several VSC valve levels).

The losses in the grading circuit with dc voltage applied are calculated as:

$P= U_d^2/R_g$

The losses in the snubbers are calculated as:

$P_{snubber}= P_{on\text{-}stateI} + P_{turn\text{-}onI} + P_{turn\text{-}offI} + P_{off\text{-}state}$

In other cases the losses can vary according to design and application. In principle the losses are calculated by taking the energy flowing in the voltage grading circuit/snubber resistor plus the number of events occurring in a fundamental frequency cycle, and then divided by the cycle time.

P_{VD} = sum of all voltage grading circuit/snubber losses in a VSC valve level.

7.1.3 Gate Drive Unit / Auxiliary Power

The gate drive unit can consists of different parts of circuits for feeding electronics and driving the IGBT. It is dependent on the design and sums up from current sources, voltage sources, zenerdiodes, IC circuits and clamping circuits and is usually given as a lump sum per position.

P_{GU}= losses in feeding circuits/auxiliary power in a VSC valve level

7.1.4 Summary

Total valve losses are

$P_{valve}= (P_{IGBT} + P_{diode} + P_{VD} + P_{GU})*N_s*N_{valve}$

Where:

N_s= Total number of VSC valve level in a single valve function

N_{valve} = Total number of valves in the station

Notes:

1: If devices common to more than one VSC valve level is used the losses must be calculated separately for that device.

2: If switching (and by that the losses) vary for different VSC valve level in the chosen VSC topology, the different losses shall be calculated independently for each valve and added separately to get the total losses.

7.2 VSC DC CAPACITOR AND SUBMODULE DC CAPACITOR

With the assumption that the harmonic ripple voltage is significantly lower than the dc voltage for a VSC dc capacitor bank the losses can, in line with IEC 61803 §5.7.2, be taken as the losses of the grading resistors.

In case the ripple voltage is substantial or in the case of an Sub-module Capacitor (with high ripple) dielectric losses as well as resistive series losses should be considered.

7.3 REACTORS

The losses of a dry type reactor consist of the I^2R losses of the winding and the eddy losses induced in the winding conductors and in other metallic components of the reactor. Furthermore, the eddy losses of metallic elements in the vicinity of the reactor, for example the screening cage enclosing the phase reactor will also contribute to the total loss. Therefore the reactor should be fully assembled for the loss measurement.

Only the winding loss (total loss excluding the losses external to the winding), will heat up the conductors and its associated insulation. The highest winding temperature may be expected at the top of the winding. Allowable temperature limits of the winding depend on the selected insulation system (for example, temperature class F, 155°C) and on the loading conditions of the reactor. Since the loading profile for reactors in HVDC projects may be more stringent than for reactors in other applications it is recommended to design

the reactors with sufficient thermal allowance to avoid premature thermal aging of the insulation.

Phase reactors are usually installed indoors. Sufficient ventilation must be provided to exhaust the heated air from the reactor hall.

7.3.1 Phase Reactor

The losses for the phase reactors are in general calculated according to clause 5.6 of IEC 61803. But the total phase reactor losses should be measured including the losses in the shield.

The impedance of a dry-type air-core phase reactor remains constant with the current and therefore the harmonic losses may be measured at any current level and corrected to the rated harmonic current:

$$P_r = \left(\frac{I_r}{I_m} \right)^2 \cdot P_s$$

Where

Pr = the losses at rated current

Ir = rated current

Im = current in the reactor when losses were measured

Ps = the losses at reference temperature and measured current, Im

The total losses for one phase reactor are calculated as:

$$P_L = P_1 + \sum_{n=1}^{m} P_{r,n}$$

Where:

P1 = the losses at the fundamental current

n = harmonic order

Pr,n = calculated losses through the reactor at nth harmonic.

7.3.2 Valve Reactor

The valve reactor losses are calculated as the phase reactor losses, including shield losses if used.

7.3.3 DC reactor

When a dc side series reactor is included the corresponding losses shall be considered.

DC side reactor losses are calculated as the phase reactor losses, including shield losses if used.

7.4 FILTER

7.4.1 AC filter

Determination of losses for ac filters should follow the principles and conditions outlined by IEC 61803, i.e. for idealized conditions with respect to the ac and dc systems. The converter shall be modeled as a generator of harmonic voltages and the ac system shall be assumed to be open-circuited.

In the no-load operating mode, ac filters are usually disconnected from the ac system and, therefore generate no losses. In the case where ac filters are energized while the converter is in no-load operating mode only the fundamental frequency losses shall be considered.

7.4.2 DC Filter

Determination of losses for dc filters (if any) should follow the principles and conditions outlined by IEC 61803, i.e. for idealized conditions with respect to the system and the converter.

Dielectric losses shall be included in the no-load losses, since the dc filter typically is energized with the converter.

7.4.3 Radio Frequency Interference Filter

Determination of the losses in the high frequency filters, i.e. RFI and PLC filters, should follow the principles and conditions outlined by IEC 61803, i.e. for idealized conditions with respect to the ac and dc systems.

No-load losses in RFI filters are negligible, since the harmonic currents are zero and losses due to the leakage dc current can be neglected.

7.5 INTERFACE TRANSFORMER

The transformer losses should be calculated according to clause 5.2 of IEC 61803. The no-load losses (core losses) shall be determined according to IEC 60076-1. The operating conditions of the transformer should include decisive fundamental frequency current loading and, if applicable, depending on the harmonic filtering solution the harmonic current loading should also be included.

7.6 OTHER LOSSES

The main other sources of losses not covered in the above description are losses related to valve cooling and auxiliary power.

The valve cooling system typically consists of cooling tower fans and circulation pump motors. At no-load, when the valves are energized, losses related to the circulation pump motors should be included. For load losses the corresponding number of cooling tower fans shall be included.

The auxiliary losses are calculated for the following systems;

- Losses in other auxiliary services of a converter station, i.e. air conditioning of control system cubicles, battery chargers, auxiliary transformers etc.

- Ventilation systems of indoor equipment, for example valve halls and equipment enclosures

The losses of other equipments such as the grounding device, bus bars, measuring devices, PLC equipments etc. should be considered if used according to relevant IEC standard 61803.

7.7 REFERENCES

[7-1] IEC 61803. *Determination of power losses of in high voltage direct current (HVDC) converter stations*, February, 1999.

8. COMPONENT TESTS

8.1 VSC VALVE

8.1.1 General Requirements for Performance of Tests

The following principles should apply:

- Type test should be performed on a complete valve or on an appropriate number of valve sections, as specified according to IEC62501, to verify that the valve design meets the specified requirements. All type tests should be performed on the same valve(s) or valve section(s);
- Certain type test may be carried out either on a complete valve on a valve section;
- Material for the type tests should be selected without special adjustment;
- Individual tests may be performed in any order；

8.1.2 Valve Temperature at Testing

The voltage blocking capability of IGBTs and FWDs is temperature-dependent. Normally the voltage blocking capability is increased with the temperature increasing. It is lower at room temperature than it is at normal working junction temperature. All dielectric tests should be carried out at room temperature.

Unless specified otherwise, the operational tests should be carried out under the conditions that produce the highest component temperature that may occur in real operation.

8.1.3 Operational tests

8.1.3.1 Test object

The tests may be performed on either a valve or valve sections. The choice depends mainly upon the valve design and the test facilities available. The tests specified in this clause are valid for valve sections containing five or more series-connected VSC valve levels. If tests with fewer than five levels are proposed, additional test safety factors should be used. Under no circumstances shall the number of series-connected levels for tests be less than three.

The valve or valve sections under test shall be assembled with all auxiliary components. When required, a proportionally scaled valve arrester shall be included. The arrester shall be scaled to the number of series-connected levels under test to give a protective level which corresponds at least to the maximum characteristic of the service arrester.

The coolant shall be in a condition representative of service conditions. Flow and temperature, in particular, shall be set to the most unfavorable values appropriate to the test in question, such that the relevant component temperature(s) are equal to the values applicable in service.

In topologies with valves acting like controllable voltage sources，the test objective can be one or several

submodules (with submodule dc capacitor).

8.1.3.2 Test circuit

For a valve which acts like a controllable voltage source and contains a built-in dc storage capacitor, the dc capacitor and its connections to the semiconductor devices are an integral part of the test object. However, for a valve which acts as a switch, where the VSC dc capacitor is separate from the valve, the VSC dc capacitor needs to be correctly represented in the test circuit. In particular, the series leakage inductance of the connections between the VSC dc capacitor and the valve, and the stray capacitance across the valve section, must be correctly reproduced and scaled to the size of valve section under test.

The test circuits should give stresses equivalent to the appropriate service conditions. The test circuits vary with different tests and different types of VSC valve. For example, the back to back test circuit is applied in steady-state operation test whilst the synthetic circuit is used for transient test.

8.1.3.3 Maximum continuous operating duty test

The principal objective of this test is to verify the valve's switching capability at periodic turn-on and turn-off operation. The operation causes special stresses on the IGBTs because of the combined effect of voltage and current during the switching processes.

This test also verifies the proper operation of the grading circuits for both dynamic and static conditions.

All the parameters below need to be reproduced during tests based on the most onerous converter operating conditions.

As for VSC valves:

- Maximum turn-on current
- Maximum turn-off voltage
- Maximum du/dt
- Maximum di/dt

The test current shall be based on the maximum continuous direct current at the maximum ambient temperature.

The test current, expressed as an rms value, shall incorporate a test safety factor of 1.05.

The test voltage corresponding to the maximum continuous operating dc voltage shall be determined by the maximum continuous operating dc voltage, including ripple, which shall incorporate a test safety factor of 1.05;

The maximum continuous operating duty test can usually be combined with the maximum temperature test.

8.1.3.4 Maximum temporary overload operating duty test

If the valve is specified for temporary overload operation, it shall be subjected to the maximum temporary overload operating duty test. The valve or valve section should reach thermal stability under the maximum continuous operating duty test or equivalent from the temperature stress point of view prior to the test and the test is then started. The test duration should be equal to the specified duration of temporary overload operation multiplied by test safety factor of 1.2. Following the temporary overload operation duty test, the maximum continuous operating duty test should be performed to verify the appropriate temperature design and also to check any damage during the test.

In topologies with valves acting like controllable voltage sources，the relative testing procedure is similar to the topologies with valves acting as switches.

8.1.3.5 Minimum dc voltage test

The test is to verify the performance of the valve electronic circuits whose energy is extracted from the voltage between valve terminals.

The test voltage is the minimum dc voltage required to ensure normal operation of valve when the valve electronic circuit is ready.

To verify the correct operation of the valve electronic circuits, energize the valve or valve section and monitor the feedback signals from the valve or valve sections. Only the voltage but not the current is important for this test.

In topologies with valves acting like controllable voltage sources，the test objective mainly focuses on the submodule which contains the submodule dc capacitor. The energy should be extracted from the submodule dc capacitor which can be charged by another power unit, e.g. the dc voltage source, to testify the submodule electronic circuits can operate correctly.

The minimum dc voltage test should consider the voltage charged in the VSC without switching of IGBTs with the consideration for the specific requirements of the scheme:

a)charging from ac side,

b)charging from dc side.

The test voltage, U_{min}, is determined by the lowest dc voltage across one valve in service where proper functioning of the valve electronics is required with a test safety factor of 0.95;

8.1.3.6 Temperature rise test

The main purpose of this test is to verify that the temperature rise of the most critical heat producing components is within the specified limits and to verify that no components or material are subjected to excessive temperature under different steady-state operating conditions.

The maximum temperature test can usually be combined with the maximum continuous operating duty test.

The test should be performed on a complete valve or on valve sections, using the test procedure described in

section 8.1.3.3.

The valve should be subjected to voltages and currents that result in the same losses as in service under specified operating conditions, taking into account the test safety margins in order to determine the temperature for the most stringent thermal conditions. The test should be continued for 30 minutes after thermal equilibrium has been reached.

Several methods can be used to measure the temperature rise of critical components, including temperature sensitive stickers which show the surface temperature reached during operation.

Note: no accurate method for measurement of junction temperature of a valve in real operation is presently available. A measurement of the surface temperature might be used as an indication the junction temperatures.

8.1.3.7 IGBT overcurrent turn-off test

The test object is the same as section 8.1.3.1.

The principal objective of the test is to check the capability of the IGBTs to turn off under significant overcurrent condition and the voltage withstanding capability of the IGBTs just after the turn off.

Scenarios to be considered are:

- Short-circuit of an ac terminal to ground;
- Phase-to-phase short circuit across the ac terminals;
- Short circuit of the bridge arms in the same phase unit or valve mis-fire of the other valve in the same phase unit.

For topologies with valves acting like controllable voltage sources, the test object can be a valve or valve sections. The following scenarios should be considered:

- Short circuit of the bridge arms in one submodule or valve mis-fire of the other IGBT in the same submodule;
- Valve section flashover or valve flashover.

8.1.3.8 Short-circuit current test

The test object is the same to section 8.1.3.1

The principal objective is to check the adequacy of the devices, especially the FWDs or auxiliary components, such as thyristors protecting the FWDs, and their associated electronic circuits with regard to current stresses under specific short-circuit conditions. The mechanical strength of the valve bus bars is also checked in this test.

Stresses to be considered are as follows:

- Continuous current-carrying of the diode caused by dc pole-to-pole short-circuit fault.

The amplitude and the duration of the fault current should be determined under the conditions that lead to the most severe stress from the diode junction temperature point of view. Because of the uncertainty in the fault current value, no test safety factor is applied to the test current in this test.

Depending on the ratio of inductance and resistance in the short circuit path, reverse voltage may be applied to the diodes just after the fault current. In this case this reverse voltage including turn-off overvoltage should be reproduced during the test. Test safety factor of 1.05 should be applied to the test voltage.

8.1.4 Valve Support Dielectric Test

8.1.4.1 Test object

The test objects for the test include insulators in the valve support structure, cooling ducts, light guides and other insulating components related to the valve support structure. The test objects for the test should not necessarily include the valves; however the numbers of cooling ducts and light guides related to the VSC valve should be equal to the actual ones. If the supplier can demonstrate that the reduction of these components and does not affect the results of tests, then it may be accepted.

The purity of the cooling water should be kept at the normal operating value.

8.1.4.2 Valve support dc voltage test

The test is intended to verify the voltage withstand capability of the valve support insulation under-maximum steady-state dc voltage stress and dc temporary overvoltage stress across the valve support.

The test shall then be repeated with the voltage of both polarities.

Prior to the test, the valve support shall be short-circuited and earthed for a minimum of 2 h.

The valve support dc test voltage shall be determined in accordance with the maximum value of the dc component of the steady-state operating voltage appearing across the valve support;

NOTE: Operation conditions which shall be considered in choosing the test voltages are as follows:

- Maximum dc terminal to ground voltage under all steady-state operation conditions
- Maximum dc terminal to ground voltage induced by ac temporary overvoltages, which include conditions as follows:
    - The dc overvoltage caused by ac system faults, including the blocking of the inverter, load rejection and etc;
    - The dc pole-to-ground overvoltage caused by filter bus asymmetrical grounding fault;
    - The healthy pole overvoltage caused by dc pole to ground fault;

8.1.4.3 Valve support ac voltage test

The test is intended to verify the voltage withstand capability of the valve support insulation under-maximum steady-state ac voltage stress and ac temporary overvoltage stress including switching overvoltage across the

valve support.

The rms value of the valve support ac test voltage U_{tas} shall be determined in accordance with the peak value of the maximum repetitive operating voltage across the valve support during steady-state operation, including switching overshoot;

Operation conditions which shall be considered are as follows when choosing the test voltages:

- Maximum ac terminal to ground voltage under all steady-state operation conditions
- Maximum ac terminal to ground voltage induced by ac temporary overvoltage, which include conditions as follows:
    - The ac overvoltage caused by filter bus asymmetrical ground fault;
    - The ac overvoltage caused by ac system faults, like load rejection, the blocking of the converter and etc.

Note: The temporary overvoltage factor and safety factor should refer to IEC62501.

8.1.4.4 Valve support switching impulse voltage test

The test is to verify the voltage withstand capability of the insulation of valve support under various switching impulse stresses across the valve support. The test shall comprise three applications of positive polarity and three applications of negative polarity switching impulse voltages between the main terminals of the valve (connected together) and earth. Standard switching impulse voltage waveforms specified in IEC 60060 will be employed.

The test voltage should be determined according to the insulation co-ordination of the VSC substation which takes into account various switching impulse voltage peaks that are possible at the ac side, which mainly includes:

- Fault-clearance switching overvoltage
- System resonance overvoltage
- Transformer energization overvoltage
- Overvoltage due to internal ac bus faults
- Overvoltage due to dc bus faults

8.1.4.5 Valve support lightning impulse voltage test

The test is intended to verify the voltage withstand capability of the valve support insulation under various switching impulse stresses across the valve support. The test shall comprise three applications of positive polarity and three applications of negative polarity lightning impulse voltages between the main terminals of the valve (connected together) and earth. Standard lightning impulse voltage waveforms specified in IEC 60060 will be employed.

The test voltage should be determined according to the insulation co-ordination of the VSC substation which

takes into account the following scenario:

- Lightning impulse voltage which are possible at ac side;
- Fast transient voltage at switching of the opposite valve.

8.1.5 Dielectric Test between Valve Terminals

8.1.5.1 Test object

The test object for this test should be a complete valve or valve sections. Tests on individual valve sections are acceptable if the supplier can demonstrate that the voltage distribution between valve sections, under test conditions, is representative of the voltage distribution within a complete valve in service.

For all impulse tests, the valve electronics shall be energized unless otherwise specified.

The coolant shall be in a condition that represents service conditions except for flow rate which can be reduced. If any object external to the structure is necessary for proper representation of the stresses during tests it shall be included or simulated in the test. Earth planes shall be used, whose separation shall be determined by the proximity of other adjacent valves and earth potential surfaces.

8.1.5.2 Valve ac-dc voltage test

This test is to verify the valve voltage withstand ability and insulation reliability against the repetitive voltage stresses applied across the valve terminals. The test should demonstrate that:

- The valve will withstand the specified overvoltages;
- Partial discharges will be within a specified limit under onerous operational conditions;
- The valve electronic systems are immune to interference and function correctly.

AC and dc components of valve short-time test voltage are peak values of maximum transient ac and dc overvoltages across the valve. Besides, the limiting effect of valve arrester (if any) or pole arrester shall be taken into account to derive overvoltages in service conditions.

In this test a capacitor can be used in conjunction with an ac test voltage source to produce a composite ac – dc voltage waveform. Depending on the converter topology, the capacitor could be an integral part of the valve, or it could be a separate item (part of the test circuit, not part of the test object). Alternatively a separate dc voltage source could be used to substitute the capacitor.

For topologies with valves acting like controllable voltage sources, the capacitor may be charged before the test, and then the dc voltage and ac voltage should be applied at the dc and ac terminals respectively.

NOTE: It may be necessary to disable gate units or other auxiliary circuits in this test in order to prevent interference with partial discharge measurement, for example, from gate unit power supply circuits.

The valve test voltages have a sinusoidal waveform superimposed on a dc level.

The valve short-time test voltage shall be determined in accordance with the peak value of the maximum transient ac component over-voltage and the maximum transient dc component over-voltage across the valve.

Fault conditions which shall be considered for the short-time test voltage are as follows:

- AC terminal asymmetric faults;
- AC system load-rejection;
- Valve flashover or misfiring;
- Internal ac bus faults;
- DC bus faults.

The limiting effect of the valve arrester or pole arrester can be taken into account to derive the overvoltage in service condition. A test safety factor of 1.1 should be considered.

The valve's long-time test voltage shall be determined in accordance with the maximum steady-state phase-to-phase voltage on the ac system or the valve side of the transformer if a interface transformer is used between the ac system and converters, and the maximum value of the dc component of the steady-state operating voltage of the dc system;

The choosing of test voltage shall consider the following conditions:

- The ac component of the test voltage represents the maximum switching overvoltage including the effect of the valve arrester;

- The peak voltage for the long-time test should be higher than the maximum switching overvoltage during the normal operation. The difference of them is the test safety factor 1.1;

- The dc component of the test voltage represents the peak value of the maximum steady-state dc component of the ac system.

NOTE: The use of a capacitor instead of a dc source in the test circuit should be mutually agreed by manufacturer and purchaser as the test voltage is higher than actual value.

8.1.5.3 Valve switching impulse voltage test

For some applications, for instance, no overhead line is present in dc side and the busbar between phase reactor and valves is completely protected against direct lightning strike in ac side or in topologies, where the valve acts like a controllable voltage source with its own submodule capacitors, impulse tests in such applications can be omitted.

The impulse test will be applied only in one polarity which corresponds to the polarity of valve withstand voltage.

If the valve impulse withstanding levels are equal to or less than the valve ac-dc test level it is deemed that the valve ac-dc test can cover the impulse tests.

Standard switching impulse voltage waveforms specified in IEC 60060 will be employed.

If the valve arrester protection is used, the valve switching impulse test withstand voltage shall be determined in accordance with the switching impulse protective level of the valve arrester;

If the valve arrester protection is not used, this test is intended to verify the valve insulation when the valve is not directly protected by surge arresters, then the valve switching impulse test withstand voltage shall be determined in accordance with the switching impulse prospective voltage across valve terminals according to system insulation coordination studies;

Two situations, i.e. test with and without arrester shall be considered. The test voltages shall be:

- Valve arrester switching impulse protection level when valve is protected by a valve arrester
- Prospective switching impulse voltage subjected by the valve which is determined in the system insulation coordination study when the valve is not protected by valve arrester.

The test shall take into account the following switching overvoltage scenarios and various switching impulse voltage peaks generated at ac and dc side:

- Fault-clearance switching overvoltage
- System resonance overvoltage
- Transformer saturation overvoltage
- Switching surge caused by energization of the interface transformer

The valve shall withstand the test voltage without switching or insulation breakdown.

8.1.6 Tests for Valve Immunity to Electromagnetic Disturbance

The principal objective is to verify the immunity of the valve to electromagnetic interference (electromagnetic disturbance) arising from voltage and current transients generated within the valve and imposed on it from the outside.

The sensitive elements of the valve are generally electronic circuits used for controlling, protecting and monitoring of the VSC valve levels.

Generally, the valve immunity to electromagnetic disturbance can be checked by monitoring the valve during other type tests. It is industry experience that electromagnetic fields with a high rate of change and with high amplitude represent the greatest risk for producing EMI. For this reason, the maximum continuous operating duty test (8.1.3.3), the valve switching impulse voltage test (8.1.5.3) and the IGBT overcurrent turn-off test (8.1.3.7) are the most important.

The tests should demonstrate that:

- out-of-sequence or spurious switching of IGBT does not occur;
- the electronic protection circuits installed in the valve operate as intended;
- false indication of VSC valve level faults or erroneous signals sent to the converter control and protection systems by the valve base electronics, arising from receipt of false data from the valve

monitoring circuits, does not occur.

8.2 INTERFACE TRANSFORMER

Test of the interface transformer depends on its function and stresses in the respective VSC scheme.

In case of a symmetric monopole configuration, in which the interface transformer is not exposed to any dc voltage offset during operation, the interface transformer can be considered to be an ac power transformer. In such case the test procedure is similar to conventional transformers, as per IEC 60076.

In case of an asymmetrical monopole configuration, the interface transformer will be exposed to a dc voltage offset during operation. Under such circumstances, the interface transformer is like a HVDC converter transformer, whose test value, test procedure and acceptance criteria shall follow IEC 61378, part 2, but the routine tests exclude polarity reversal including partial discharge measurement.

Depending on the overall converter configuration and operating principles the voltage and current in the interface transformer may contain significant harmonic components. These harmonic components shall be considered in determining the equivalent test parameters for the transformers, particularly with respect to the heat run (temperature rise) test and noise level test, as described in IEC 61378, part 2.

In addition, ac voltage withstand test of the interface transformer shall consider the following scenarios:

- Voltage distortion under asymmetric fault of converter internal ac bus;
- AC temporary overvoltage caused by ac system faults, load rejection and etc;
- DC offset of transformer ac terminal generated by dc single-pole-to-ground fault.

The test procedure and acceptance criteria of the ac voltage withstand test can be referred to IEC 61378, part 2.

8.3 VSC DC CAPACITOR

There is no standard applicable for dry type self-healing VSC dc capacitors with a high operating voltage. IEC 61071 (2007) is the most applicable but it is limited to operating voltage up to 10 kV in practice. The limit was acknowledged in a previous revision, IEC 61071-1 (1991), but not in present revision IEC 61071 (2007). However, design and test factors are not adopted for a higher voltage why the limit still must be considered applicable.

In view of this the following test procedure has demonstrated to be proficient for dry type self healing dc capacitors used as energy storage in VSC transmissions.

Routine Tests

(1) **Capacitance measurement and tan δ measurement**

As per IEC 61071 Clause 5.3.

The measurement shall be carried out at a voltage not less than $\frac{1}{2\sqrt{2}} u_r \frac{1}{S}$, where

- u_r is the specified ripple voltage, peak to peak value, across the capacitor bank
- S is the number of series connected capacitor units in the bank.

(2) Voltage test between terminals

As per IEC 61071, clause 5.5.2, with the following modification:

The terminal-to-terminal test voltage shall be a dc voltage of $1.2 \times SIPL \frac{1}{S}$ and the duration shall be 10 s. Where

- SIPL is the switching impulse protective voltage level of the arrester.

The capacitance shall be measured before and after the test and the values corrected to the same dielectric temperature.

(3) AC voltage test between terminals and case

As per IEC 61071 Clause 5.6.1. (Only applicable for capacitors with metallic container and with terminals insulated from container.)

(4) Measurements of grading resistor

The resistance of the grading resistor shall be measured according to IEC 61071, clause 5.7.

The resistance of the grading resistor(s) shall be verified by measuring the voltage decay of a capacitor unit.

Expected time at which the voltage decay should be measured is in the range of R*C seconds, where C is the unit capacitance and R the grading resistor resistance.

The terminal voltage following the R*C function shall not deviate more than 1%.

(5) Sealing test

As per IEC 61071, clause 5.8. The capacitor units shall be visually inspected

Type Tests

(1) Thermal Stability Test

As per IEC 61071 Clause 5.10.

(2) Surge discharge test

As per IEC 61071 Clause 5.9.

The surge current of a single unit shall be the discharge current of a single unit shall be $\hat{I}_{test} > 1.4 \frac{SIWL}{\sqrt{\frac{L}{C}}} \frac{1}{n}$, where

SIWL is specified switching impulse protective voltage withstand level of the arrester across the capacitor bank,

L is fault inductance,

C is specified capacitance/ bank,

n is number of parallel connected capacitor units or strings/ bank.

(3) AC voltage test between terminals and case

As per IEC 61071 Clause 5.6.2. (Only applicable for capacitors with metallic container and with terminals insulated from container.)

(4) Voltage test between terminals

As per IEC 61071, clause 5.5.3, with the following modification:

Test voltage selected as $1.3 \times SIPL \frac{1}{S}$. Where

- SIPL is the switching impulse protective voltage level of the arrester.

The capacitance shall be measured before and after the test and the values corrected to the same dielectric temperature.

The test shall be performed on at minimum 6 units. Failure of one single unit is permitted. Self-healing breakdown is permitted, but no puncture or flashover.

8.4 SUBMODULE DC CAPACITOR

In topologies with valves acting like controllable voltage sources, the capacitors are assigned to the submodules.

The tests shall be performed according to IEC 61071as described in the chapter before.

Special testing demands include:

1) DC voltage test

- Rated voltage under steady state;
- The overvoltage caused by balance control failure;
- Overvoltage caused by internal ac bus asymmetric fault.

2) AC current test

- The rated current under steady state;
- Unbalance current under internal ac bus fault.

3) Life time test

Special accelerated life time tests shall be performed in order to verify the specified life time in the real application, taking ambient conditions, especially the temperature profile of the real application into account.

8.5 REACTOR

Basically the test program of international standards such as IEC 60076-6 "Reactors" or ANSI C57.16 "Series Reactors" is applicable for testing the reactors for VSC-HVDC converters.

IEC 60076-6 comprises several categories of reactor application. Section 8 of 60076-6 "Current limiting reactors and neutral earthing reactors" is applicable to phase and valve reactors and, as the description implies, section 12 "Smoothing reactors", is applicable to smoothing reactors.

8.5.1 Phase Reactor

Two level or three level VSC converters may be tested in accordance with Section 8 of IEC 60076-6. However, a few additions and modifications are required to reflect the stresses by the specific nature of the converter voltage.

Since the reactor reflects the in-service conditions only when it is mounted in the electromagnetic cage, the type tests have to be done on the reactor equipped with the shield and, for ease of testing, the routine tests may be done without shield.

Routine tests (performed excluding cage):

- Measurement of winding resistance
- Measurement of impedance
- Measurement of loss
- Lightning impulse voltage test

- Test of the tightness of the liquid cooling circuit for reactors with directly liquid cooled winding (if any)

Type tests (performed including cage):

Measurement of loss, at fundamental frequency and all relevant harmonic frequencies

Since an air-core reactor is a linear device with regard to the current magnitude, the losses may be measured at any current level and corrected to the rated harmonic current. As the eddy losses vary with frequency the losses have to be measured at the fundamental and all harmonic frequencies of the current spectrum.

Temperature rise test at loss equivalent ac current;

The loss equivalent current is derived from the loss measurement (without cage) at fundamental frequency and harmonic frequencies using the formula:

$$I_t^2 \cdot R_t = I_F^2 \cdot R_F + \sum_{n=2}^{m} \left(I_{Hn}^2 \cdot R_{Hn} \right)$$

Where,

I_t = equivalent test current (50 Hz)

I_F = maximum continuous fundamental current

I_{Hn} = maximum continuous n^{th} harmonic current

R_t = winding resistance at test current frequency corrected to maximum operating temperature

R_F = winding resistance at fundamental frequency corrected to maximum operating temperature

R_{Hn} = winding resistance at n^{th} harmonic, corrected to maximum operating temperature.

m = highest specified harmonic

Separate source ac withstand voltage test on the reactor mounted on support insulators

The test is to verify the voltage withstand capabilities of phase reactor terminals. The test shall be performed at 50 Hz or 60 Hz. The voltage shall be applied between both winding terminals connected together and earth. The duration of the test is 1 min. Test voltage peak applied between phase reactor terminals and valve support is 1.5 times higher than the maximum operation voltage. The valve side of phase reactor is subjected to HF square/step wave which can be substituted by power frequency ac voltage with equal amplitude.

Measurement of the capacitance to earth and of the self resonant frequency of the reactor mounted on support insulators and installed in the cage; from these measurements the capacitance along the winding may be

derived.

Special tests that may be applicable for the reactors are as follows:

- Switching impulse voltage test

  The test is to verify short-time large-amplitude voltage withstand capability of phase reactor. Test voltage is determined by the following stresses:

  - overvoltage caused by internal ac bus asymmetric fault
  - overvoltage caused by dc single-pole-to-ground fault

- Short-time current withstand test

  - overcurrent caused by internal ac bus fault
  - overcurrent caused by dc pole-to-pole fault

- measurement of acoustic sound level

- measurement of high frequency impedance

The above tests can be carried out according to section 8 and section of IEC 60076-6.

8.5.2 Valve Reactor

Valve reactors for multilevel VSC converters provide a virtually sinusoidal wave shape at the ac terminals and do not require tests other than those covered by the test program for standard series reactors as per IEC 60076-6 "Reactors". The special tests described in clause 8.5.1 are also applicable for the valve reactors with exception of measurement of high frequency impedance.

8.5.3 Smoothing Reactor

Section 12 "Smoothing reactors" of IEC 60076-6 is fully applicable to smoothing reactor for VSC- HVDC systems. Furthermore, the standard ANSI 1277 to be revised in 2009 will contain an informative annex addressing the specifics for smoothing reactor used in VSC-HVDC schemes.

8.5.4 Common Mode Blocking Reactor

Conventional tests of common-mode blocking reactor are as per IEC 60076-1, where dc resistance measurement of reactor winding is as per Section 58.5 of IEC 60289, while external dc voltage withstand test is in accordance with IEC60076-3.

8.6 RADIO FREQUENCY INTERFERENCE FILTER

The equipments of RFI filters for VSC system are covered by international standards.

Depending on the capacitor design, RFI capacitors on the ac side are tested in accordance with different IEC standards:

- IEC 60358 “Coupling capacitors and capacitor dividers” for capacitors of porcelain design
- IEC 60871-1 “Shunt capacitors for ac power systems having a rated voltage above 1000V. Part 1: General”, for capacitors of bank design including capacitor cans

For dc applications, if applicable, the same standards are referred to with the exception that the rated voltage has to be corrected with regard to the dc voltage stresses.

Line reactors are tested in accordance with IEC 60353 “Line traps for ac power systems”

8.7 REFERENCES

[8-1] IEC 60060, *High-voltage test techniques*.

[8-2] IEC 60060-1:1989, *High-voltage test techniques – Part 1: General definitions and test requirements*.

[8-3] IEC 60060-2:1994, *High-voltage test techniques – Part 2: Measuring systems*.

[8-4] IEC 60071-1:2006, *Insulation co-ordination – Part 1: Definitions, principles and rules*.

[8-5] IEC 62501, *Electrical testing of voltage sourced converter (VSC) valves for high-voltage direct current (HVDC) power transmission*.

[8-6] IEC 61378-2:2001, *Converter transformers - Part 2: Transformers for HVDC applications*.

[8-7] IEC 61071:2007, *Capacitors for power electronics*.

[8-8] IEC 61071-1-1991, *Power electronic capacitors - Part 1: General*.

[8-9] IEC TR 61071-2-1994, *Power electronic capacitors - Part 2: Requirements for disconnecting test on fuses, destruction test, self-healing test and endurance test*.

[8-10] IEC 60076-6-2007, *Power transformers - Part 6: Reactors*.

[8-11] IEC 60076-1-2000, *Power Transformers-Part 1: General Edition 2.1*; Edition 2:1993 Consolidated with AMD 1:1999.

[8-12] IEC 60076-3-2000, *Power Transformers Part 3: Insulation Levels, Dielectric Tests and External Clearances in Air Second Edition*; Corrigendum 11-2000.

[8-13] IEC 60358-1990, *Coupling capacitors and capacitor dividers*.

[8-14] IEC 60871-1-2005, *Shunt capacitors for ac power systems having a rated voltage above 1000 V-Part 1: General*.

9. CONCLUSIONS

By the end of 2008, the total in-service rating of VSC transmission schemes has reached 1660MW, and it is expected to exceed 2400MW in early 2010. The Nord E.ON1 project, being constructed in Germany, will reach a dc power level of 400MW at ±150kVdc. The rating power of Transbay Cable project in USA is 400MW at ±200kVdc. VSC technology has provided a competitive alternative to the present power transmission for the new energy generation, the urban power supply and the for ac system interconnection.

Because of the increasing application of VSC transmission, the manufacture, subsystem assembly and tests of related components need to be understood by a wider user community. Among them, in particular information about the specification, testing of VSC- HVDC components and subsystems and operation of such systems is needed.

The key subsystem of the VSC transmission system is the converter. VSC transmission converter can be divided into two types of topology. One can be described as VSC valve acting as a controllable switch, such as two-level, three-level, and multi-level converters and so on. Pulse width modulation, such as SPWM and OPWM is commonly employed for this topology. The other type is the VSC valve acting like a controllable voltage source. In this topology a desired valve voltage is the sum of the submodule voltages and is achieved by means of individual and appropriate control of the VSC valve levels.

In the VSC transmission system the following components and subsystems need to be tested:

- VSC valve;
- Interface transformer;
- Phase reactor/ Valve reactor;
- VSC dc capacitor/submodule dc capacitor;
- Smoothing Reactor;
- Common mode blocking reactor(if any);
- Other components (if any).

Steady-state stresses on components are mainly influenced by operating mode, topology, modulation strategy, the equivalent reactance of the ac system and by the characteristics of the dc transmission system (i.e. over-head lines or cables).

For topologies where VSC valve acts as a controlled switch, the interface transformer is loaded sine wave current and voltage with high frequency harmonic which need to be filtered. The valve is exposed to the VSC dc capacitor voltage and the ac bus current at the same time during the switching process. In this case, the dc voltage ripple is dependent on the dc capacitance while the ac current ripple is determined by the phase reactance. The phase reactor is subjected to high frequency voltage harmonics as well.

For topologies where VSC valve acts like a controlled voltage source, the voltage and current at valve side of the interface transformer are approximately sine waves. The valve withstands step voltage and half ac bus current plus one third dc current. Since the capacitors are distributed within submodules and are carrying line frequency currents, the resulted voltage ripple is higher.

During ac system faults and post-fault recovery, line frequency overvoltage, line frequency undervoltage and phase angle swing appear. In this case, the converter is able to limit the increase of the current flowing through the valve and the phase/valve reactor, thus there are no serious stresses on each component. In case of asymmetric faults, negative sequence voltage arises up to 30% to 50% of the normal voltage, which may

result in valve blocking, then the arrester is activated in order to protect valves from overvoltage. For lightning overvoltage, switching overvoltage following fault clearing and resonant overvoltage which are transmitted to valves and phase/valve reactors via the incoming ac bus, the corresponding arresters will be activated to mitigate overvoltage stresses.

During internal faults in a VSC substation the VSC valve is exposed to greater overvoltage and overcurrent than in case of ac system faults. Type and location of the fault, transformer winding type and grounding arrangement of the VSC substation determine the fault severity and characteristic. Among the component failure faults, the valve short circuit mode failure and open mode failure are the worst cases. Valve short circuit mode failure results in overcurrent due to discharge of the VSC dc capacitor, while valve open mode failure will lead to overvoltage of fault IGBT or VSC by adding the whole dc voltage on them.

In symmetric monopole systems, the healthy pole voltage increases in the event of ground fault of the other pole. Filter bus arrester and dc bus arrester can limit this overvoltage. However, when it comes to a bipolar short circuit fault, the FWD is subject to high overcurrent derived from ac system before the tripping the ac breakers even if the converter is blocked. In asymmetric monopolar system, the pole to earth fault is similar to that in a symmetric monopole system. When the lightning strikes, there is no obvious overvoltage on the VSC valve due to the protection provided by the arrester.

The calculation of component losses is illustrated in detail in this document. Component losses related to the testing mainly include valve losses (which include IGBT turn-on, turn-off and on-state loss, FWD loss, snubber circuit loss, gate driver unit loss and submodule dc capacitor loss in case of topologies with valves acting like controlled voltage sources), and VSC dc capacitor loss, reactor losses (including phase reactor loss, valve reactor loss and dc reactor loss), filter loss and interface transformer loss etc.

The test of the valve includes dielectric test and operational test. The dielectric test involves ac voltage test, dc voltage test, lightning and switching impulse test between valve terminals; ac voltage test, dc voltage test, lightning and switching impulse test for the valve support. The operational test consists of maximum continuous operating duty test, maximum temporary overload operating duty test, minimum dc voltage test, temperature rise test, IGBT overcurrent turn-off test, short-circuit current test and tests for valve insensitivity to electromagnetic disturbance.

For other components, special tests need to be considered for VSC-HVDC applications are listed in this document. For routine tests please refer to relevant standards.

The choice of test parameters is not investigated in this document; please refer to the standards such as IEC62501 etc. Simple advices can be found for test circuits in this document.

VSC-HVDC technologies are still evolving, and therefore test methods and guidelines must anticipate technology improvement and enrichment of engineering applications. The working group recommends having amending of the document within one year.

The working group also recommends that the reliability and availability performance for VSC transmission schemes should be collected and reported on by the Advisory Group B4-AG-04.

10. APPENDIX: TYPICAL VOLTAGE AND CURRENT WAVEFORMS

10.1 INTRODUCTION

This appendix is intended to give an impression of real voltage and current waveforms of different VSC topologies during continuous operation of the VSC valve.

10.2 TWO-LEVEL VSC TOPOLOGY (VSC VALVE OF 'SWITCH' TYPE)

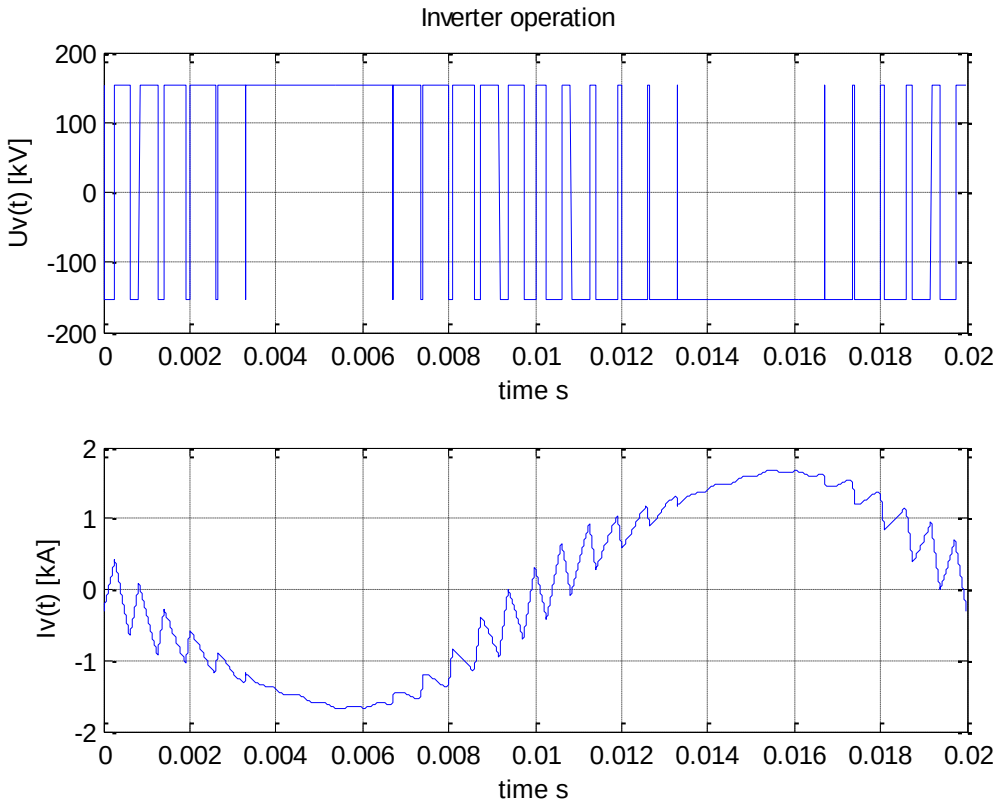

Figure 10.1 Voltage and current on the valve side of the phase reactor in inverter operation

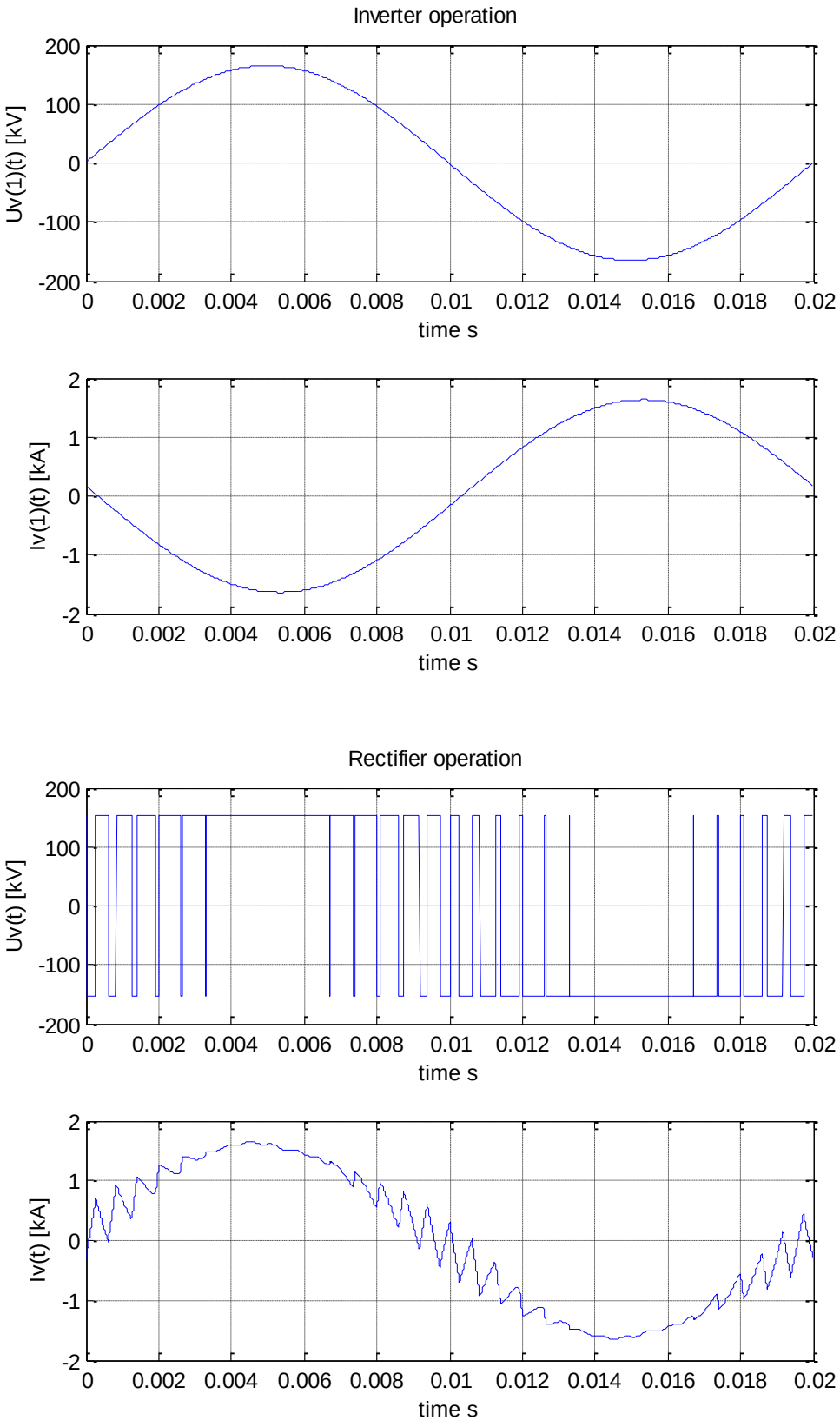

Figure 10.2 Voltage and current on the valve side of the phase reactor in rectifier operation

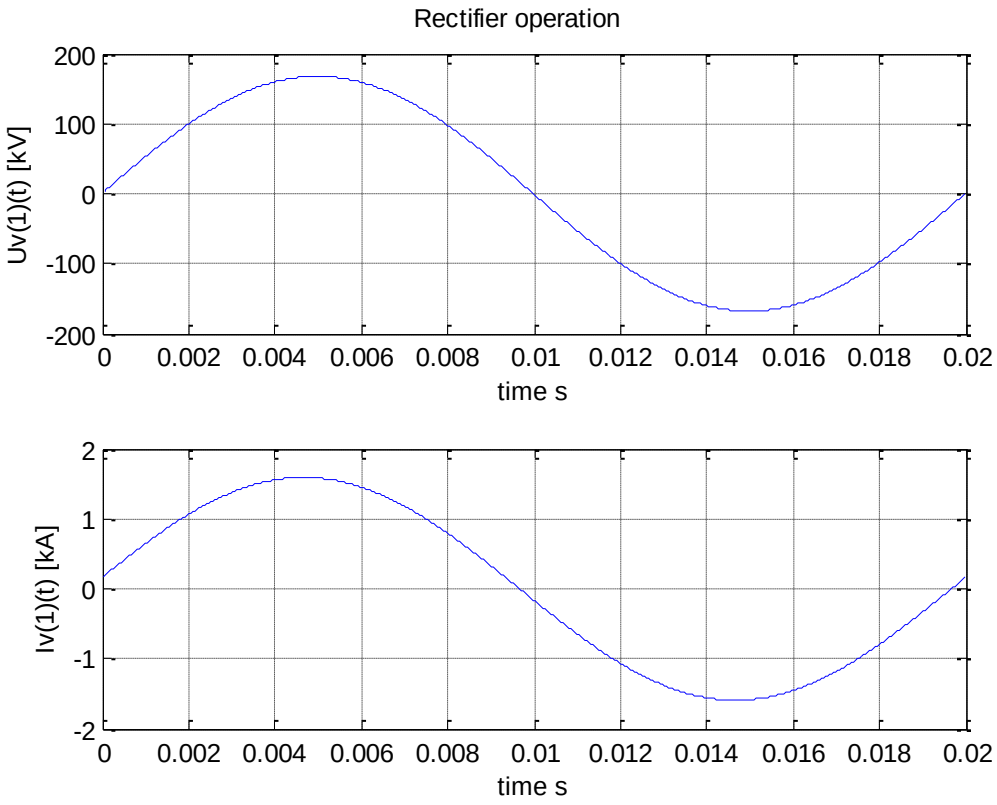

Figure 10.3 Voltage and current on the transformer side of the phase reactor in inverter operation

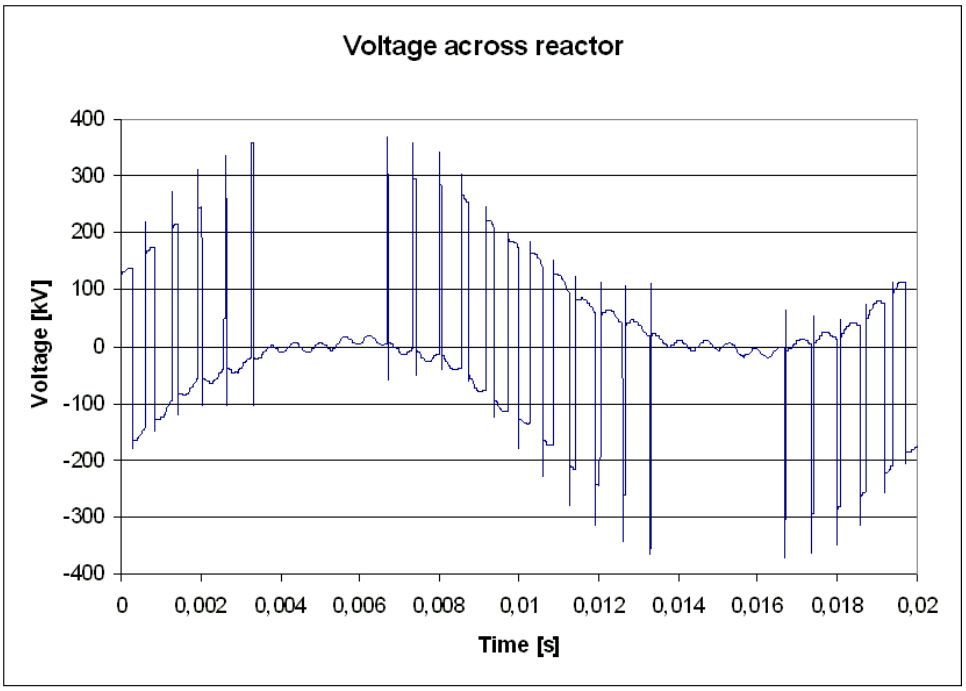

Figure 10.4 Voltage across the phase reactor

In this section some typical waveforms related to a two level converter is presented for operation in rectifier

and inverter mode, respectively. The waveforms are obtained from site measurements from the Estlink project with converters rated for 368MVA with a dc link voltage of +/- 150kV. The rated filter bus voltage and phase reactor current is 195kV and 1090A, respectively. The switching pattern is based on OPWM with a switching frequency of 1150Hz.

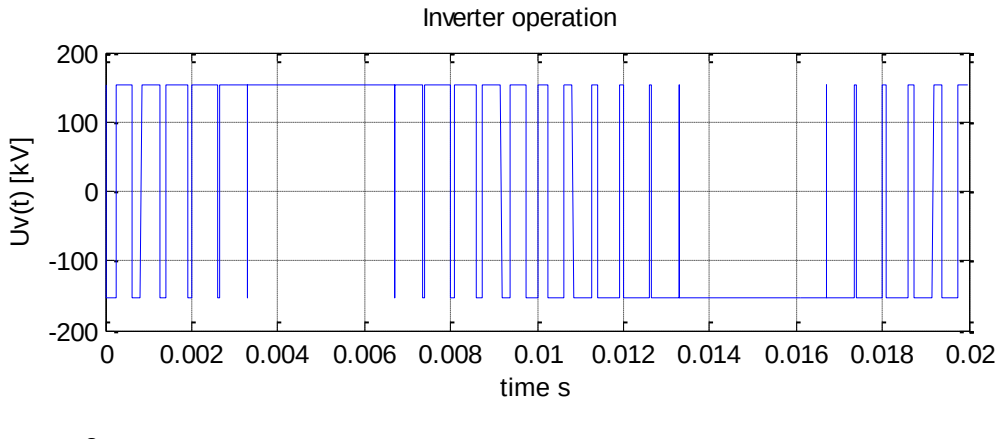

Figure 10.5 Voltage on the valve side of the phase reactor in inverter operation (simulated waveform)

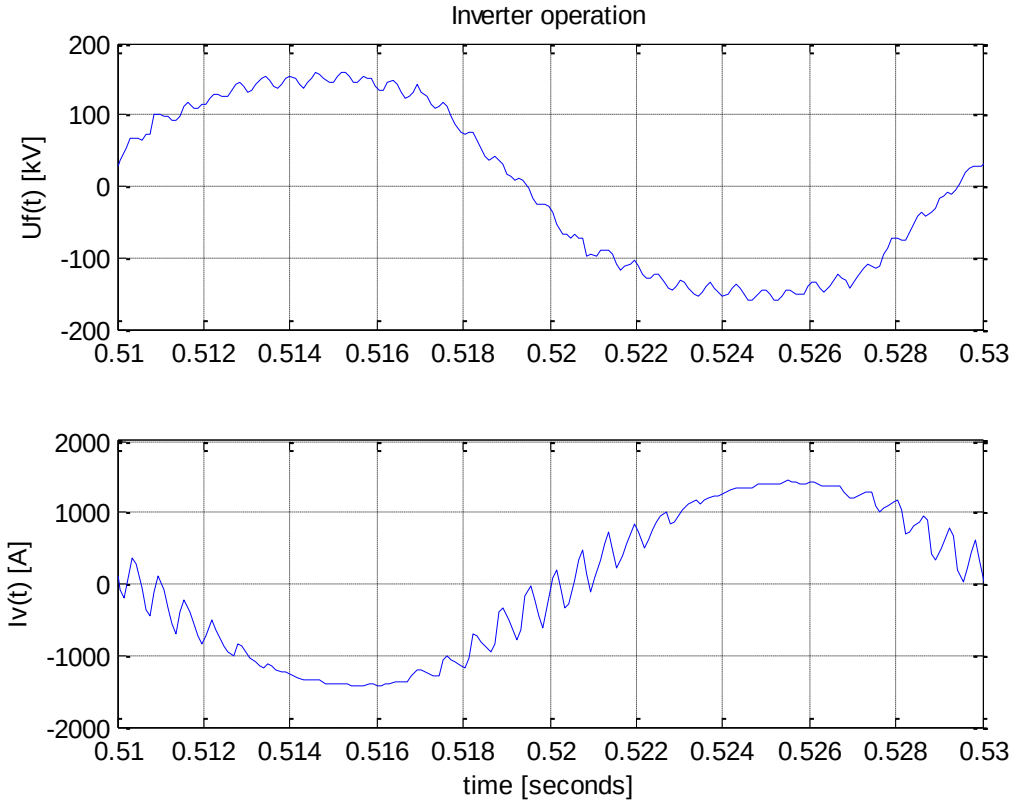

Figure 10.6 Filter bus voltage and phase reactor current in inverter operation

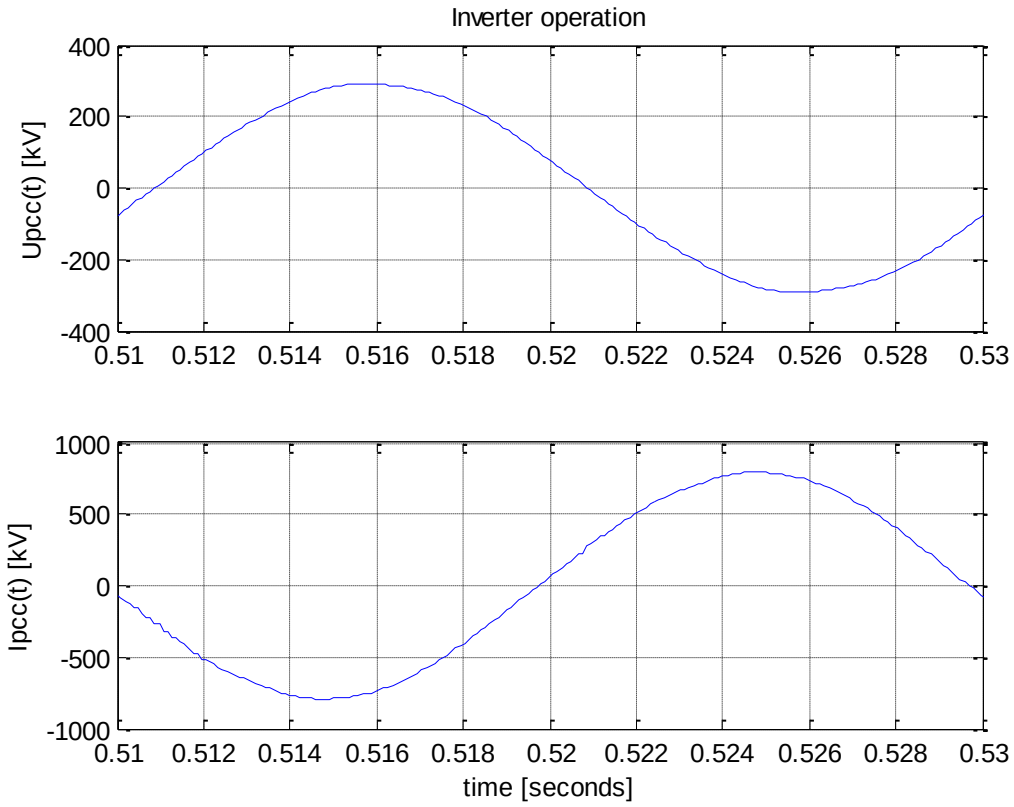

Figure 10.7 Voltage and current on the grid side of the transformer in inverter operation

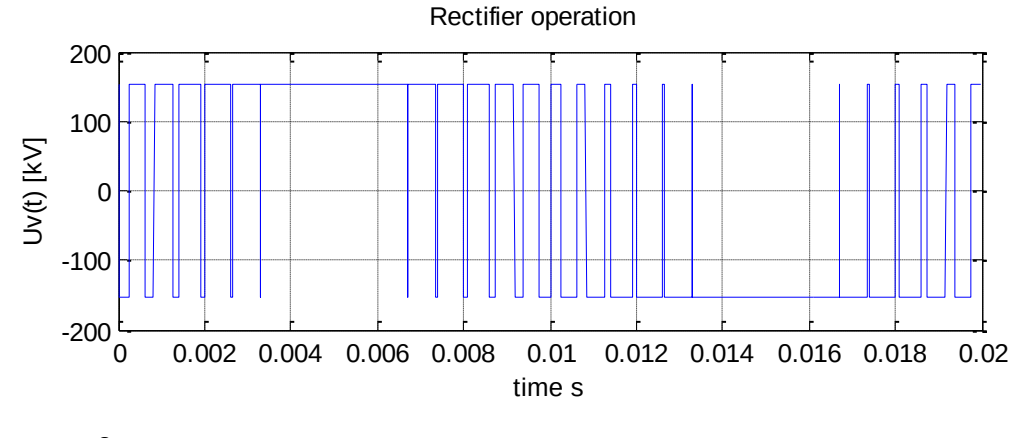

Figure 10.8 Voltage on the valve side of the phase reactor in rectifier operation (simulated waveform)

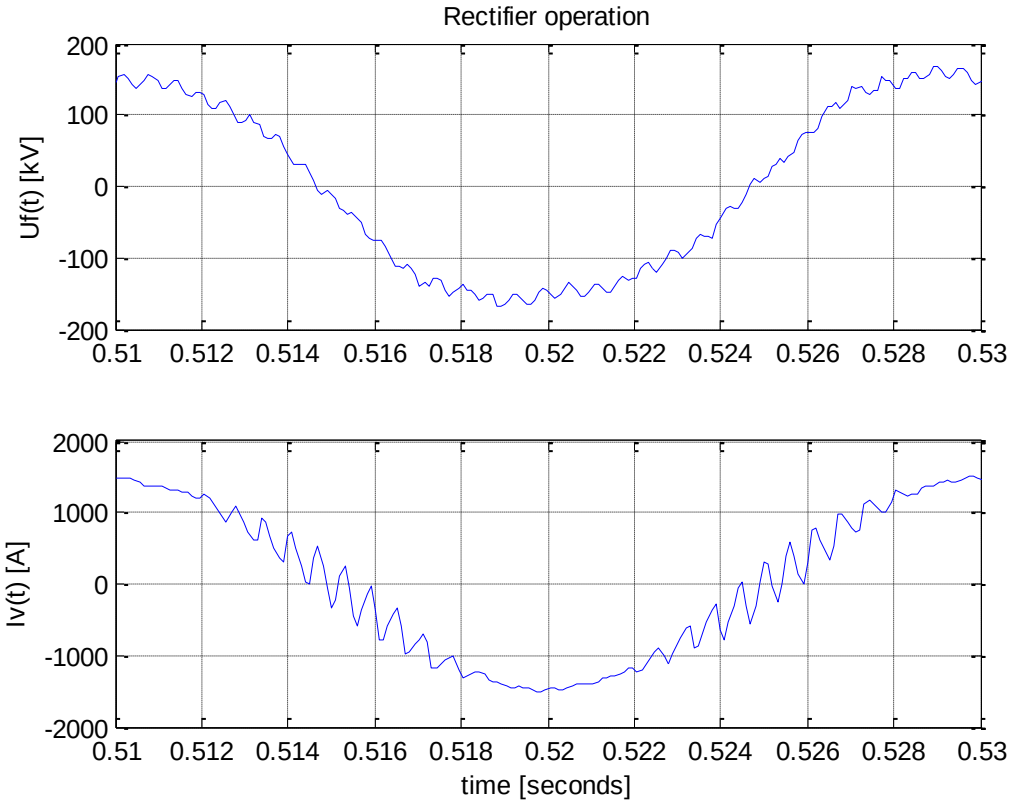

Figure 10.9 Filter bus voltage and phase reactor current in rectifier operation

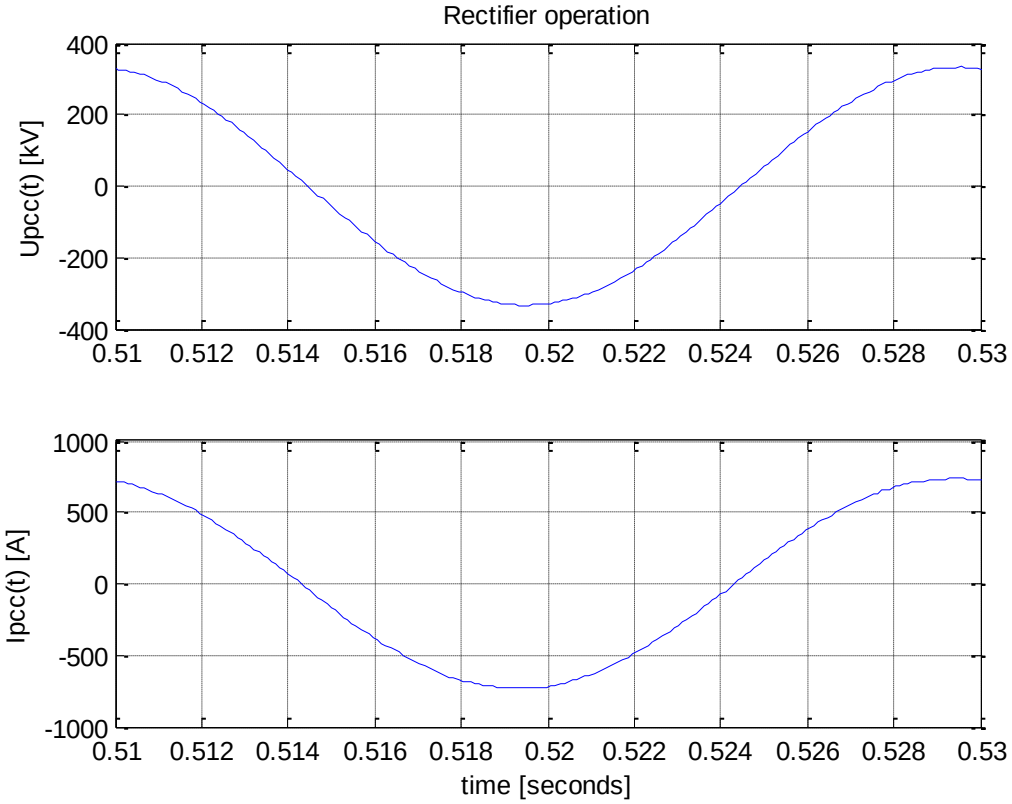

Figure 10.10 Voltage and current on the grid side of the transformer in inverter operation

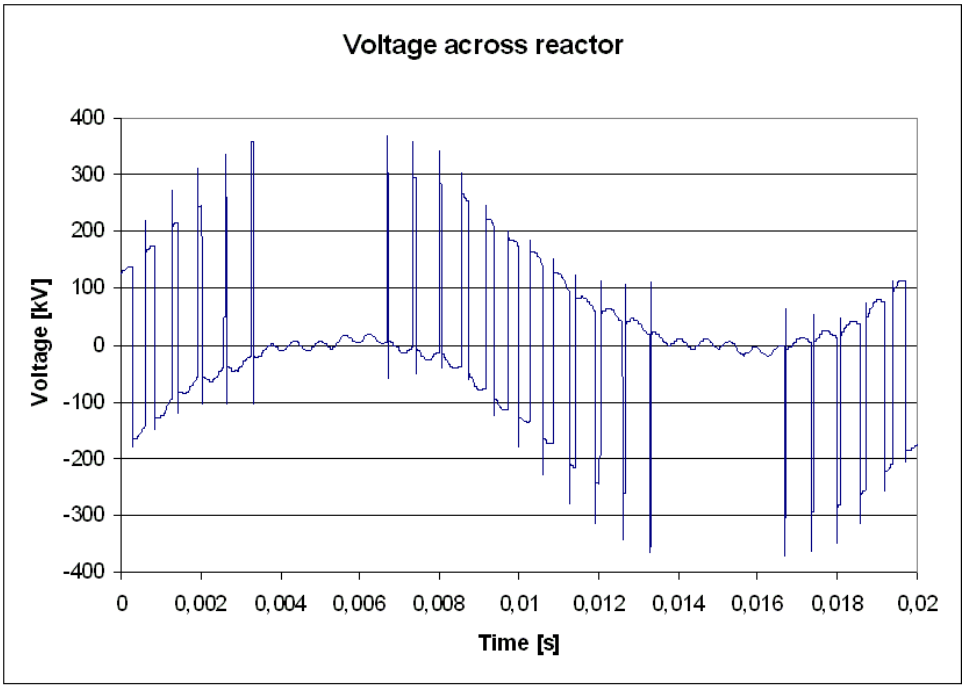

Figure 10.11 Voltage across the phase reactor (simulated waveform)

10.3 Modular Multi-Level VSC Topology (VSC Valves of 'Controllable Voltage Source' Type)

The presented voltage and current waveforms were recorded during operational type tests of the first commercial VSC project based on topologies with valves acting like controlled voltage sources, named Transbay Cable. These tests were performed on a back to back configuration of two converters, each with 12 levels per valve. The switching frequency of the individual submodule was about 300Hz and was approximately two times higher compared to service conditions.

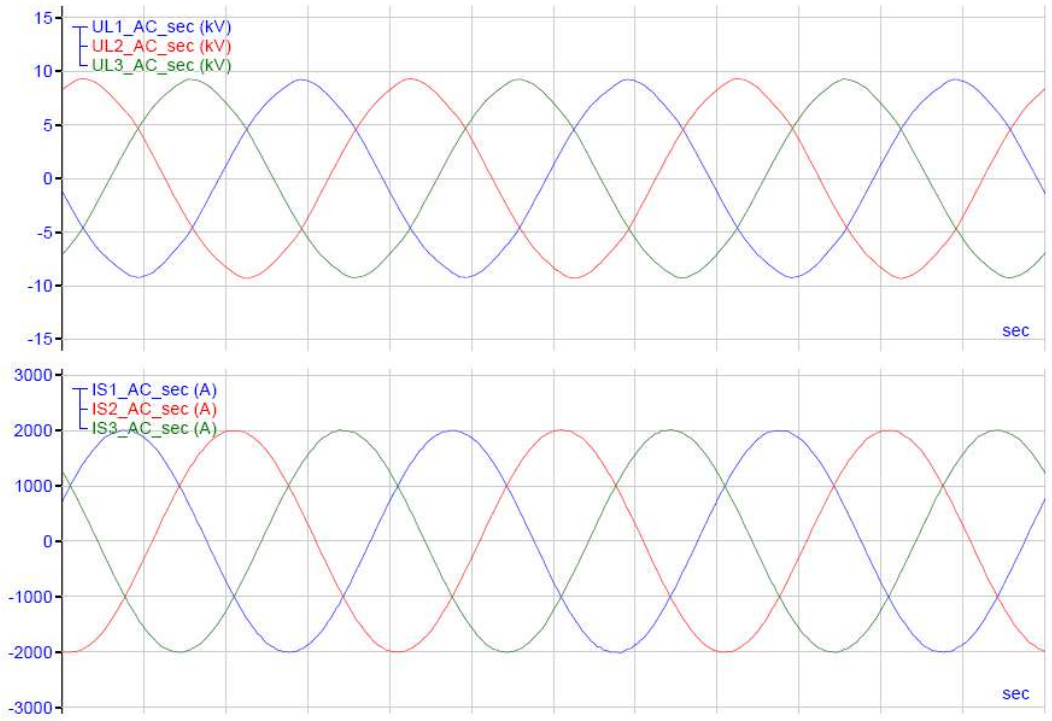

Figure 10.12: Converter ac waveforms for rectifier operation, P = 26MW, Q = 6MVAR (leading current); top: converter ac voltages to ground, bottom: secondary transformer currents

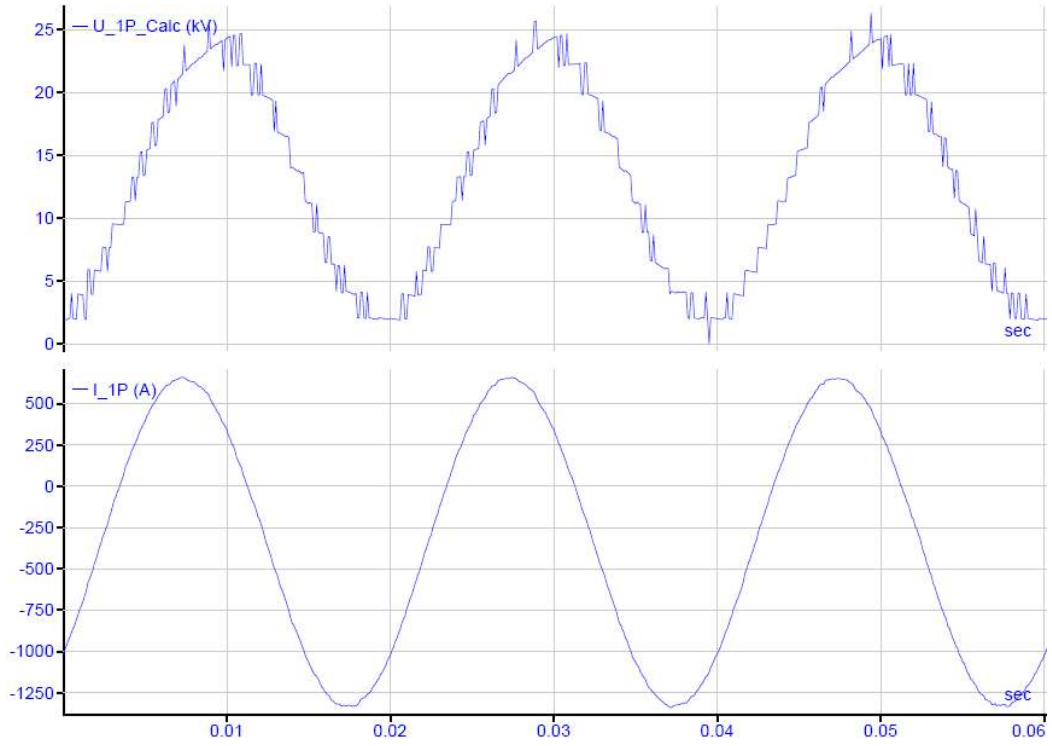

Figure 10.13: Converter valve waveforms for rectifier operation, P = 26MW, Q = 6MVAR (capacitive, leading current); top: sum of submodule output voltages of one valve; bottom: valve current

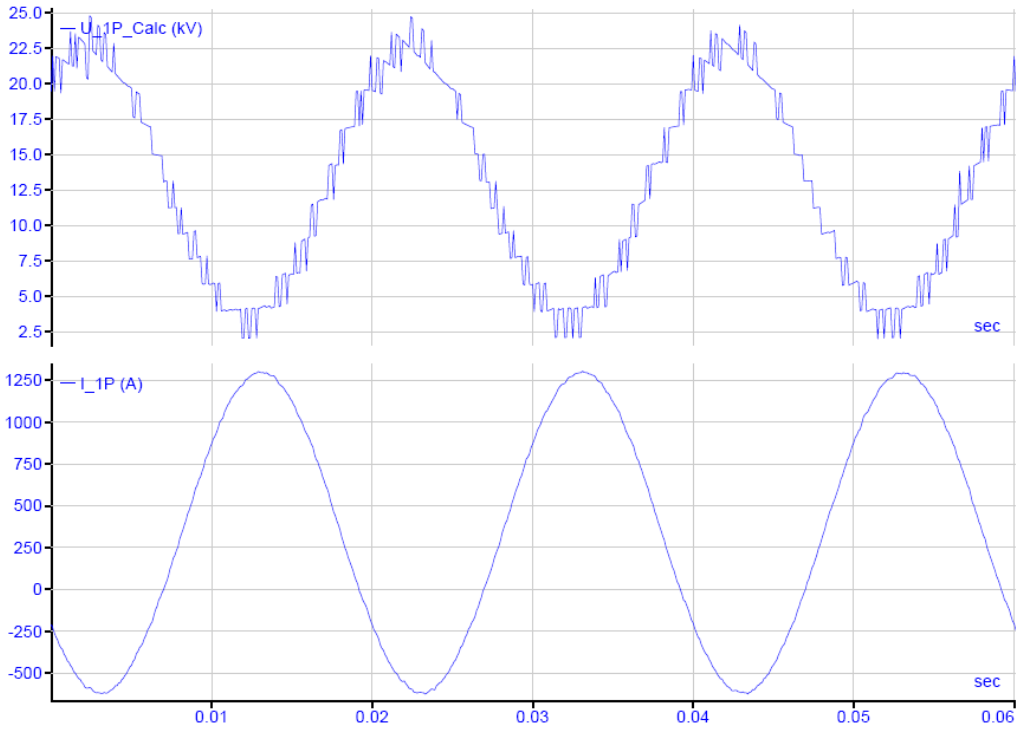

Figure 10.14: Converter valve waveforms for inverter operation, P = 26MW, Q = 6MVAR (inductive, lagging current); top: sum of submodule output voltages of one valve; bottom: valve current